

Audio and Video-in configuration module

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1 Introduction

The configuration module performs the startup configuration for both audio and video decoder chips. It is needed if you are using the [audio controller](#) or the [video-in controller](#).

This document will describe the interface and parameters of the configuration module.

You can download the source code (in Verilog) [here](#).

2 Module interface

2.1 Port Descriptions

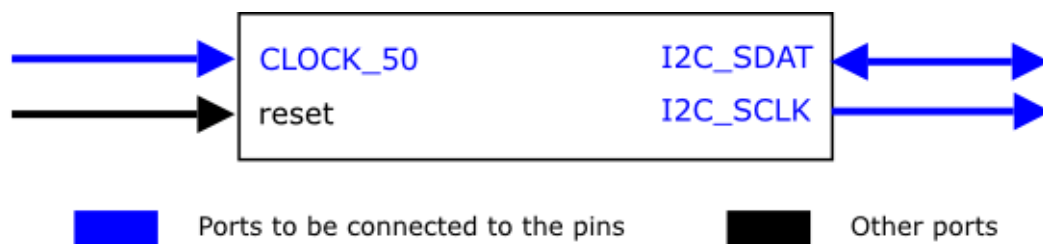


Figure 1: Module interface

The module interface is illustrated in [Figure 1](#), with inputs shown on the left, outputs and bidirectional lines on the right. Ports are used as follows:

- `CLOCK_50` - system clock input, must be 50MHz for the timing control to work properly.
- `reset` - the active-high reset.
- `I2C_SDAT` and `I2C_SCLK` - off-chip lines to be connected to the correspondingly named pins, as defined in [this file](#).

2.2 Module parameters

- `USE_MIC_INPUT` - Select the audio source: 0 to select Line-in, 1 to select Microphone.

2.3 Interface description

The module is completely self contained and only needs to be instantiated in your circuit for the configuration to be performed. The configuration is performed automatically every time the module is reset.

3 Module operation

The configuration module performs the configuration for both the audio and video chips using the same data bus. The default parameters are hard coded into the module, and described in the [audio controller](#) and the [video-in controller](#) documentation. The default parameters will be acceptable for most users, and therefore the understanding or modification of the configuration module is not required.