A Stochastic Model to Predict the Routability of Field-Programmable Gate Arrays

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Abstract

Field-Programmable Gate Arrays (FPGAs) have recently emerged as an attractive means of implementing logic circuits as a customized VLSI chip. FPGAs have gained rapid commercial acceptance because their user-programmability offers instant manufacturing turnaround and low costs. However, FPGAs are still relatively new and require architectural research before the best designs can be discovered. One area of particular importance is the design of an FPGA's *routing architecture*, which houses the user-programmable switches and wires that are used to interconnect the FPGA's logic resources. Because the routing switches consume significant chip area and introduce propagation delays, the design of the routing architecture greatly influences both the area utilization and speed-performance of an FPGA. FPGA routing architectures have already been studied using experimental techniques in [1] [2] and [3]. This paper describes a stochastic model that facilitates exploration of a wide range of FPGA routing architectures using a theoretical approach.

In the stochastic model an FPGA is represented as an N x N array of logic blocks, separated by both horizontal and vertical routing channels, similar to a Xilinx [4] [5] [6] FPGA. Each routing channel comprises a number of tracks and each track consists of a set of short wire segments. Routing switches are available to connect the pins of the logic blocks to the wire segments, and to connect one wire segment to another. The number of routing switches and their distribution over the wire segments are parameters of the stochastic model. A circuit to be routed is represented by additional parameters that specify the total number of connections, and each connection's length and trajectory.

The stochastic model gives an analytic expression for the *routability* of the circuit in the FPGA, which is defined as the percentage of the circuit's connections that can be accommodated by the FPGA's routing architecture. Practically speaking, routability can be viewed as the likelihood that a circuit can be successfully routed in a given FPGA. The routability predictions from the model are validated by comparing them with the results of a previously published experimental study on FPGA routability.

1 Introduction

Field-Programmable Gate Arrays (FPGAs) have become increasingly popular over the past few years because, with their user-programmability and high logic capacity, they offer inexpensive customized VLSI implementations of circuits and instant manufacturing turnaround. However, FPGAs are still relatively new and have not yet approached their full potential, where they hold the promise of replacing much of the market now held by Mask-Programmable Gate Arrays (MPGAs). MPGAs are both faster and more dense than FPGAs because interconnections between logic modules in an FPGA involve (large, slow) user-programmable switches, whereas connections in an MPGA are hardwired. Although this density and speed-performance gap is an inherent consequence of user-programmability, the differences between the two technologies can be narrowed through architectural improvements in FPGAs. Specifically, these improvements should focus on FPGA *routing architectures*, since this is where the user-programmable switches reside.

The stochastic model presented in this paper is parameterized to allow the study of a wide range of FPGA routing architectures and the theory could be extended to handle even more possibilities. Thus, the main purpose of the model is as a research vehicle for studying the effects that various parameters of an FPGA's routing architecture have on the routability of circuits. Theoretical studies of this sort are attractive because they are more easily carried out than experimental ones due to the long time required to develop new CAD tools for experimentation. The stochastic model as described in this paper is not intended for use as a tool for predicting whether a given circuit will be routable in a commercial FPGA product. Commercial products invariably comprise unique features that are not represented in a general model. The stochastic theory can be extended to model specific parts, but this would entail some modifications to the probability expressions that are presented in this paper.

The characterization of FPGAs in the stochastic model is the same as that used in earlier papers on FPGA architecture [1] [2] [7] and computer-aided design (CAD) algorithms [8] [9]. As illustrated in Figure 1, the FPGA consists of a square array of logic blocks with N blocks per side, and both horizontal and vertical routing channels. In terms of commercially available devices, the structure depicted in the figure is most similar to that found in Xilinx FPGAs [4] [5] [6], but it is more general. The FPGA in Figure 1 has two pins on each side of a logic block (L) and three tracks per channel. The grid shown in the figure is referenced throughout this paper as a means of describing connections to be routed. No assumptions are necessary about the internal details of the logic blocks, except that each block has some number of pins that are connected to the channels by routing switches. The channels comprise two kinds of blocks, called Switch (S) and Connection (C) blocks, described below. The S blocks hold routing switches that can connect one wire segment to another, and the C blocks house the switches that connect the wire segments to the logic block pins.

The general nature of the S block is illustrated in Figure 2a. Its *flexibility* is set by the parameter F_s, which defines the number of other wire segments that a wire segment entering an S block can connect to. For the example shown in the figure, the wire segment at

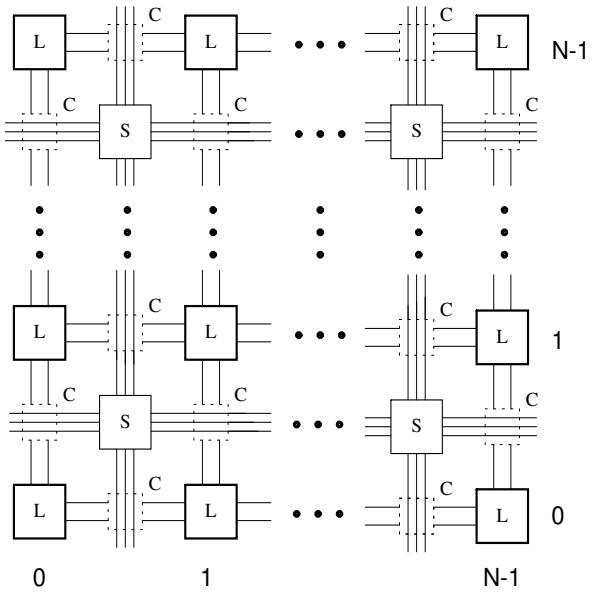

Figure 1 - *An N x N FPGA.*

the top left of the S block can connect to six others and so F_s is 6 (routing switches are shown as dashed lines in this figure). Although not shown in the figure, it is assumed that all wire segments entering an S block have the same connectivity. It is also assumed that a routing switch is always involved when passing straight through an S block, meaning that the tracks consist of short wire segments that span a single logic block. The implications of relaxing this assumption are discussed in Section 3.1.

Figure 2b illustrates a C block. The tracks pass uninterrupted through the C block and can be connected to the logic block pins via the set of switches. The flexibility of a C block, F_c, is defined as the number of wire segments in the C block that each logic block pin can connect to. For the example shown in the figure each pin can be connected to 2 vertical tracks, and so F_c is 2 (in the C block, a routing switch is drawn as an x). It is

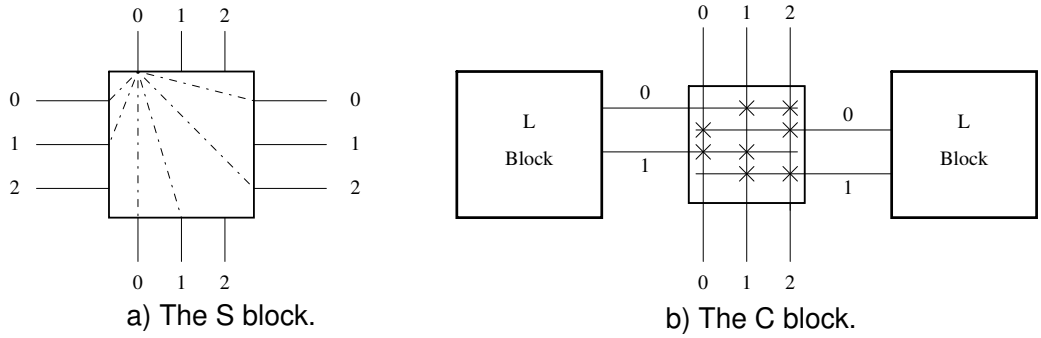

Figure 2 - *Definitions of S and C Block Flexibilities.*

assumed that all pins can connect to the same number of tracks and that the specific tracks

that can be connected to each pin are randomly chosen. The implications of this latter assumption are discussed in Section 4.3.

A wide range of routing architectures can be represented by changing the number of tracks per channel and the contents of the C and S blocks. In a routing architecture that has an abundance of switches, circuits will be easily routed. From the point of view of designing a good routing architecture, however, the number of switches should be limited because each switch consumes chip area and has significant capacitance and resistance [10]. This leads to routing architectures in which the number of routing switches is limited, which in turn produces routing problems that are not easily solved. As an example, the following section illustrates the effect on a routing problem when the C blocks allow each logic block pin to connect to only a subset of the wire segments in a channel. The example also serves as the motivation for designing the stochastic model that can account for the side effects that the routing of one connection may have on others.

1.1 Example of a Routing Problem

Figure 3 shows three views of the same section of an FPGA routing channel, and three connections that must be routed in that channel. Each view gives the routing options for one of connections A, B, and C. In the figure, a routing switch is shown as an x, a wire segment as a dotted line, and a possible route as a solid line. As indicated in the figure, it is assumed that each logic block pin can connect to only two of the three tracks in the channel ($F_c = 2$). Now, assume that connection A is completed first. If the wire segment numbered 3 is chosen for A, then one of connections B and C cannot be routed because they both rely on the same single remaining option, namely the wire segment numbered 1. The correct solution is for the router to choose the wire segment numbered 2 for connection A, in which case both B and C are also routable.

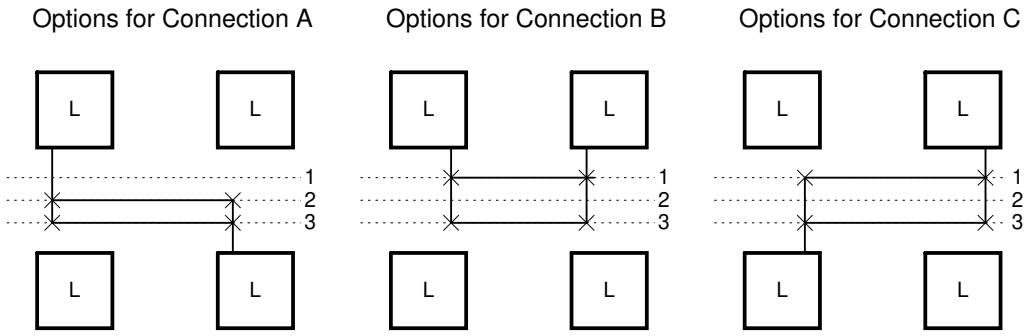

Figure 3 - *An Example Routing Problem.*

This example shows that even when there are only three connections to be routed, it is possible for a routing decision made for one connection to unnecessarily block another. This example shows connections within a single horizontal channel, but the problems are compounded when connections have segments that are in both horizontal and vertical channels. For these reasons, it is important for the stochastic model to consider the side-effects that the routing of one connection may have on others.

This paper is organized as follows. Section 2 provides an overview of the stochastic model and summarizes the main results, Section 3 describes previous research that is used to predict channel densities. Section 4 derives analytic expressions for calculating the probability that a connection can be successfully routed. The theoretical predictions of routability are given in Section 5 and Section 6 provides concluding remarks.

2 Overview of the Stochastic Model and Summary of Results

In the stochastic model, it is assumed that a circuit with a total of C_T two-point connections is to be routed in an FPGA with N x N logic blocks. The length of each connection is drawn from a probability distribution, P_L. It will later be necessary to choose a specific distribution for P_L. In Section 4.4, it is assumed that P_L is geometric, with mean length $\overline{R}$. This assumption is taken from earlier work on the stochastic modelling of two-dimensional arrays of connected cells [11] [12], and has the following physical interpretation in an FPGA: at each C block along the path of a connection, the connection will terminate (at a logic block) with probability $1/\overline{R}$ and will continue (to the next C block) with probability $1 - 1/\overline{R}$.

The C_T connections are individually referred to as $C_1, C_2, \ldots, C_{C_T}$ and the statistical event that each connection is successfully routed is called $R_{C_1}, R_{C_2}, \ldots, R_{C_{C_T}}$. The key to the stochastic model is the calculation of the probabilities of $R_{C_1}, R_{C_2}, \ldots, R_{C_{C_T}}$. Routability is defined as the percentage of the connections in a circuit that can be successfully routed. In terms of $R_{C_1}, R_{C_2}, \ldots, R_{C_{C_T}}$,this corresponds to the ratio of the expected number of successfully routed connections to the total number of connections, C_T. Thus, routability is the average probability of completing a connection and can be calculated in the stochastic model according to

$$Routability = \frac{1}{C_T} \sum_{i=1}^{C_T} P(R_{C_i}),$$

where $P(R_{C_i})$ is the probability of successfully routing C_i.

2.1 Parameters of the Model

The main result presented in this paper is the solution of the above expression for routability. It will be shown that routability is a function of several parameters that define the properties of the FPGA and the circuit to be routed. These parameters are listed below, with an indication of how each one can be obtained for a given FPGA and circuit:

- N is the number of logic blocks per side in the $N \times N$ FPGA.
- W is the number of wiring tracks per channel in the FPGA.
- C_T is the total number of two-point connections in the circuit.
- $\overline{R}$ is the average length of a connection, measured in manhattan distance between logic blocks. A typical value for $\overline{R}$ is 3, which can be measured by looking at real FPGA circuits. We note that previous theoretical work has been done in estimating average connection length for chips that consist of two-dimensional arrays of connected cells [12].
- $P(Z_1)$ is the probability that a connection will pass straight though a channel, as opposed to turning, each time it reaches the intersection of a horizontal and vertical channel. A typical value for $P(Z_1)$ is 0.75.
- F_c and F_s define the flexibilities of the FPGA's C and S blocks.
- α_1 and α_2 represent the topology of the routing switches in the FPGA's S blocks. These two parameters define the fanout that is available to a connection when it passes through an S block. α_1 represents fanout when a connection passes straight through an S block, and α_2 corresponds to the case where a connections turns.

Using these parameters, the expression for routability is solved by calculating the probability that each of the C_T connections in the circuit can be successfully routed in the given FPGA. For each connection, this involves finding the probability that a number of statistical events occur, corresponding to each step that the connection needs to make through the FPGA's routing channels. Section 4 describes this process in detail, giving expressions for the probabilities involved. Section 5 shows the routability results produced by the model and compares them to the results of a previously published experimental study on routability.

2.2 Model of Global Routing and Detailed Routing

The routing of FPGAs is modelled assuming that the classical two-stage approach of global routing followed by detailed routing is used [13]. It is assumed that once a global router assigns routing channels for a connection, a detailed router would restrict itself to those channels. This corresponds to the normal case for two-stage routing where a global router produces a set of restricted routing problems for the detailed router. While it is probable that a detailed router would see some improvements if allowed to explore other global routes for difficult connections, the effects of this optimization would be small, as discussed in [9].

In order to use a key research result by El Gamal [12] to predict the densities of the routing channels in an FPGA, the following assumption is made concerning the way in

which a global routing algorithm would assign the two-point connections in a circuit to the routing channels. It is assumed that each connection is assigned a single path through the routing channels in such a way that the number of connections per routing channel is Poisson distributed. In Section 3, we justify this assumption empirically and illustrate its use.

In the stochastic model, the detailed routing of an FPGA is represented as a random process. Given the assumption that a connection is assigned a single path through the routing channels, the probability of successfully performing the detailed routing of the connection is calculated. The probability expressions account for the number of tracks per routing channel, the flexibilities of the C and S blocks, and the side-effects that the routing of one connection has on others.

Recall that Section 1.1 showed that a key issue in the detailed routing of FPGAs is how the routing of one connection may affect other connections. To compute the value of each $P(R_{C_i})$, it is necessary for the stochastic model to account for these effects. To accomplish this, the model accounts for the impact that each successfully routed connection would have on the densities of the FPGA's routing channels. By this mechanism, the probability of completing each successive connection is influenced because there are more connections in a channel to compete with. The next section shows how El Gamal's results can be used to calculate channel densities and following this, the probability expressions for $P(R_{C_i})$ are derived.

3 Previous Research for Predicting Channel Densities

In [12], a stochastic model is developed to predict the wiring requirements of Master Slice integrated circuits that have a two-dimensional array of identical cells, with horizontal and vertical routing channels between the rows and columns of cells. The model divides the channels into segments that span the length or width of one cell and it is assumed that all interconnections start at one cell and travel a minimum distance through the channel segments to another cell. It is further assumed that the number of connections per cell can be drawn independently from a Poisson distribution with parameter λ, where λ is defined as the quotient of the total number of connections in a circuit divided by the total number of cells in the array. The average connection length, in number of cells traversed, is called $\overline{R}$. That paper also makes assumptions about the trajectories of connections, but they are not necessary for the results quoted here.

El Gamal shows that under the above assumptions, in an array that has N x N routing channels, the densities of the channel segments will be Poisson distributed, with the average density given by $(\lambda\overline{R})/2$. This result provides a convenient method of predicting channel densities and holds as long as $\overline{R} < \infty$, independent of N.

3.1 Predicting Channel Densities in FPGAs

Although the results in [12] were developed for Master Slice circuits, they can also be applied to the FPGAs considered here, since both types of devices are based on a two-dimensional array of identical cells. The definitions of the routing channels differ, but these differences can be ignored since the tracks consist of short segments that span only one cell in both cases.

Having made these assumptions, it is convenient to predict channel densities in FPGAs using El Gamal's result. The accuracy of the predictions can be checked by comparing the ideal Poisson distribution with mean $(\lambda\overline{R})/2$ to the distribution of channel densities in real FPGA circuits. Such comparisons were conducted for the example circuits that were used in the experimental study described in [2]. A typical result is shown in Figure 4, which gives one curve for the ideal Poisson distribution and another curve for the measured distribution of channel densities. As the figure shows, the actual densities are very close to the Poisson predictions.

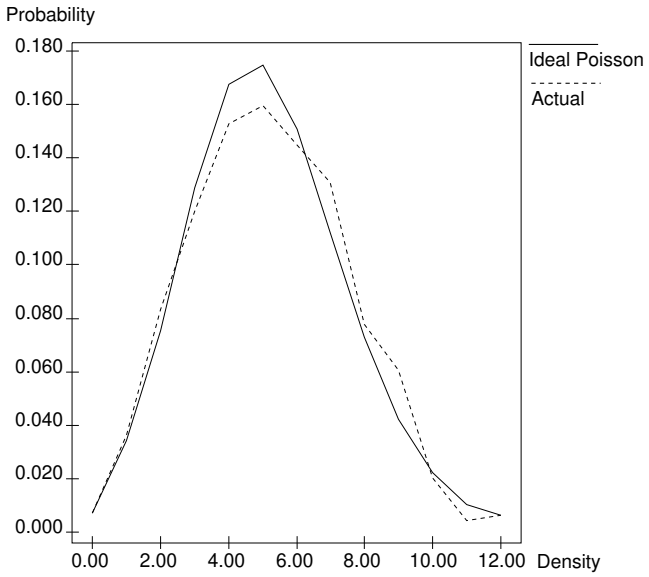

Figure 4 - *Predicted versus Actual Channel Densities.*

It is interesting to discuss a physical interpretation of the Poisson distribution in this context. Assume that an FPGA has W tracks in each routing channel and consider a specific point along the channel. For each of the W tracks at that point, define p_i as the probability of the statistical event that the track would be occupied after some circuit had been routed in the FPGA. If $W = 1$, there will be a probability, p_1, that the track will be occupied by some connection. If $W = 2$, then there will be a probability, p_2, that each of the two tracks will be occupied by some connection, and $p_2 < p_1$. Extending this to the general case, if $W = n$, then each track will be occupied with probability p_n, and

$p_n < p_{n-1} < \ldots < p_2 < p_1$. Furthermore, as $n \to \infty$, $p_n \to 0$. Since p_n is small in the limiting case, the event that a track is used is a rare event and the number of these events (density) can be approximated by the Poisson distribution. This discussion follows the standard procedure that can be found in most probability texts (such as [14]) for showing the applicability of the Poisson process as an approximation of the number of occurrences of some event that occurs rarely in the limiting case.

In FPGAs in which the tracks consist of wire segments that span multiple logic blocks (without travelling through any switches, as in the FPGA described in [6]), El Gamal's result may not be an accurate approximation of channel densities. In such cases, a different method of calculating densities would be needed. For this reason, the probability expressions that are developed in the following section are derived in a general way that does not hinge upon any particular distribution for the channel densities. However, assuming a Poisson distribution allows some expressions to be simplified, an example of which is given in Section 4.1.

4 The Probability of Successfully Routing a Connection

This section derives analytic expressions for calculating the probability of successfully performing the detailed routing of a single connection in an FPGA, accounting for the effects of other connections that have been previously routed. As an example of a connection, consider Figure 5. The figure shows a connection, C_i, that starts at logic block (x_1, y_1) and travels through routing channels to logic block (x_2, y_2). The length of C_i is defined in terms of the number of logic blocks traversed (to be consistent with [12]), as $LC_i = |x_2 - x_1| + |y_2 - y_1|$. Also, the number of S blocks that C_i passes through is given by $LC_i - 1$. To define the probability, $P(R_{C_i})$, of successfully routing C_i, it is assumed that C_i passes through n S blocks, meaning that $LC_i = n + 1$. The statistical event that corresponds to this assumption is written L_{n+1}.

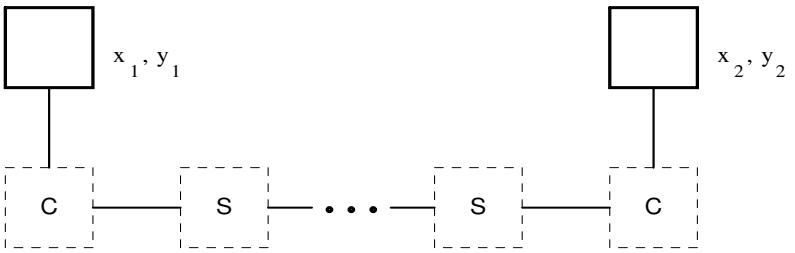

Figure 5 - *A Typical Connection.*

The following statistical events are useful for calculating $P(R_{C_i})$:

- X_1 - the event that the logic block pin associated with C_i at (x_1, y_1) can connect to at least one track at the first C block. Note that there are, by definition, F_c tracks that can connect to the logic block pin, but any number of those tracks may already be used by other connections that have been previously 'routed'.

- $S_1, S_2, \ldots, S_n$ - the events that C_i can successfully reach at least one track on the outgoing side of the first, second, up to the n^{th} S block.

- X_2 - the event that at least one of the tracks that are available to C_i at the last C block can be connected to the appropriate logic block pin at (x_2, y_2).

- R_{C_i} - the event that C_i can be successfully routed.

Since C_i is successfully routed only if all of the events $X_1, S_1, S_2, \ldots, S_n, X_2$ occur, then

$$R_{C_i} | L_{n+1} = X_1 \cap S_1 \cap S_2 \cap \ldots \cap S_n \cap X_2$$

and the probability of successfully routing C_i is given by

$$\begin{aligned} P(R_{C_i} | L_{n+1}) &= P(X_1 \cap S_1 \cap S_2 \cap \ldots \cap S_n \cap X_2) \\ &= P(X_1)P(S_1 | X_1)P(S_2 | S_1 \cap X_1)\ldots P(S_n | S_{n-1} \cap \ldots \cap S_1 \cap X_1) \cdot \\ &\quad P(X_2 | S_n \cap \ldots \cap S_1 \cap X_1) \end{aligned} \quad 1$$

Since the events $X_1, S_1, S_2, \ldots, S_n, X_2$ are not independent, it is necessary to determine expressions for each of the terms in Equation 1. This is accomplished in the following sections by using combinatorial analysis that accounts for the flexibilities of the C and S blocks (F_c and F_s), the number of tracks per routing channel (W), and the densities of the routing channels. As discussed in Section 3, channel density is approximated by the Poisson distribution with parameter $(\lambda\overline{R})/2$, where λ is the number of connections per logic block and $\overline{R}$ is the average connection length. Appropriate values for λ and $\overline{R}$ are discussed in Section 5.

4.1 The Logic Block to C Block Event

The event X_1 can be depicted as shown in Figure 6. The figure gives a routing channel with W tracks and a logic block pin that can connect to F_c of the tracks, via routing switches (shown by an x). The figure also shows a set of D tracks, drawn as dashed lines, that are already occupied by previously routed connections. In the figure, $W = 10$, $F_c = 5$, and $D = 5$. The event X_1 can then be viewed as a random process in which the switches are randomly placed on F_c of the W tracks, and the logic block pin can connect

to any of the F_c tracks that are not within the set of D used tracks. To derive an expression for $P(X_1)$, it is convenient to define the event *NONE* as the opposite of X_1 — i.e. $P(X_1) = 1 - P(NONE)$. The event *NONE* occurs when all F_c tracks are within the set of D used tracks. As a first step to evaluating $P(NONE)$, assume that $D = d$ and define the corresponding event D_d. Assuming that the F_c switches can appear on any of the W tracks, the probability of *NONE* conditional on D_d is the ratio of the number of ways in which all F_c of the switches can lie within the d occupied tracks to the number of ways in which the F_c switches can appear on any of the W tracks. By combinatorial analysis, this can be expressed as

$$P(NONE|\, D_d) = \frac{{}_dC_{F_c}}{{}_WC_{F_c}} \qquad 2$$

where ${}_dC_{F_c}$ means the combinations of d things taken F_c at a time. As a check, note that $P(NONE|\, D_d)$ is 0 if $d < F_c$ and 1 if $d = W$. Next, consider the events $D_0, D_1, \ldots, D_W$ corresponding to the possible values of D. Since the occurrence of *NONE* implies exactly one of $D_0, D_1, \ldots, D_W$, then

$$NONE = (NONE \cap D_0) \cup (NONE \cap D_1) \cup \ldots \cup (NONE \cap D_W)$$

and since $D_0, D_1, \ldots, D_W$ are mutually exclusive

$$P(NONE) = P(NONE \cap D_0) + P(NONE \cap D_1) + \ldots + P(NONE \cap D_W)$$

Using the relation $P(X \cap Y) = P(Y)P(X|\, Y)$,

$$P(NONE) = P(D_0)P(NONE|\, D_0) + P(D_1)P(NONE|\, D_1) + \ldots + P(D_W)P(NONE|\, D_W)$$

The terms $P(D_d)$ are given by the Poisson distribution (as discussed in Section 3) with parameter λ_g, written $p(\lambda_g, d)$, so that

$$P(NONE) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot P(NONE|\, D_d)$$

and, substituting Equation 2,

$$P(NONE) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{F_c}}{{}_WC_{F_c}}$$

Finally,

$$P(X_1) = 1 - P(NONE) = 1 - \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}^{d}C_{F_c}}{{}^{W}C_{F_c}} \qquad 3$$

Note that Equation 3 involves an error because the Poisson distribution has an infinite tail, whereas the summation has an upper limit of *W*. This means that there is a non-zero probability of channel densities above *W*, but for practical values of *W* this error is very small and can be ignored. This same statement also applies to other equations that appear later in this paper.

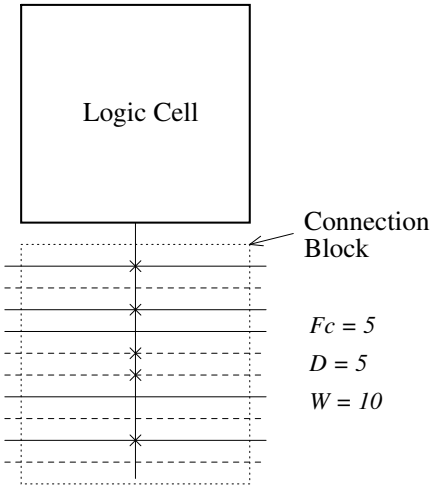

Figure 6 - *The Event* X_1.

Equation 3 has been developed in a way that does not depend upon the channel densities being Poisson distributed. This approach is taken because the densities in some FPGAs, such as those having tracks with segments that span multiple logic blocks, may have distributions that are not Poisson. The stochastic model can still be used for such FPGAs, by replacing $p(\lambda_g, d)$ with an appropriate distribution. It is interesting to note, however, that the properties of the Poisson distribution allow expressions like Equation 3 to be simplified, as described below.

Equation 3 can be simplified by realizing that a Poisson distribution is divisible. In the case of event X_1, this means that rather than considering a Poisson process over *W* tracks, with mean λ_g, it is sufficient to deal with a smaller Poisson process over F_c tracks, with mean $\lambda_g \frac{F_c}{W}$. Then, $P(NONE)$ is given by $p(\lambda_g \frac{F_c}{W}, F_c)$, and Equation 3 can be expressed as

$$P(X_1) = 1 - P(NONE) = 1 - p(\lambda_g \frac{F_c}{W}, F_c)$$

Similar simplifications can be made for other expressions shown later in this section, but they are easily developed and so are not shown.

Equation 3 calculates $P(X_1)$ based on the relationship between the event X_1 and the event *NONE*. An alternative is to calculate $P(X_1)$ directly by defining $A_1^{X_1}, A_2^{X_1}, \ldots, A_{F_c}^{X_1}$ as the events that X_1 occurs with exactly 1, 2, …, F_c available tracks. Using this approach,

$$X_1 = A_1^{X_1} \cup A_2^{X_1} \cup \ldots \cup A_{F_c}^{X_1}$$

and since $A_1^{X_1}, A_2^{X_1}, \ldots, A_{F_c}^{X_1}$ are mutually exclusive,

$$P(X_1) = P(A_1^{X_1}) + P(A_2^{X_1}) + \ldots + P(A_{F_c}^{X_1})$$

Although $P(X_1)$ can be calculated using Equation 3, each of $P(A_a^{X_1})$ will be required in the next section, and so they are derived here. Consider the general case of X_1 occurring with exactly (a) available tracks, and the corresponding event $A_a^{X_1}$. Assuming a specific number of occupied tracks, $D = d$, the conditional probability $P(A_a^{X_1} \mid D_d)$ can be expressed using combinatorial analysis as

$$P(A_a^{X_1} \mid D_d) = \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a$$

In words, this is the number of ways that a set of $F_c - a$ tracks can be within (d) used tracks times the number of ways of choosing a set of (a) tracks from F_c tracks, all divided by the number of ways that two distinguishable sets of (a) and $F_c - a$ tracks can be within W tracks. Since the occurrence of $A_a^{X_1}$ implies exactly one of $D_0, D_1, \ldots, D_W$, following the steps shown for Equation 3,

$$\begin{aligned} P(A_a^{X_1}) &= \sum_{d=0}^{W} p(\lambda_g, d) \cdot P(A_a^{X_1} \mid D_d) \\ &= \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a \end{aligned} \qquad 4$$

As a check, it is easily verified that $P(NONE)$ can be obtained using Equation 4 by setting $a = 0$, which must be true since $P(NONE) \equiv P(A_0^{X_1})$. Finally,

$$P(X_1) = \sum_{a=1}^{F_c} P(A_a^{X_1})$$

$$= \sum_{a=1}^{F_c} \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(F_c - a)} \cdot {}_{(W-d)}C_a}{{}_WC_{(F_c - a)} \cdot {}_{(W-(F_c - a))}C_a} \cdot {}_{F_c}C_a$$

4.2 The S Block Events

All of the events that are associated with S blocks can be treated in a uniform way. This section first derives probability expressions for $S_1 | X_1$ and then shows how the result can be applied to subsequent S blocks.

4.2.1 The First S Block Event, for $F_s = 3$

Since $P(S_1 | X_1)$ will be affected by the flexibility of the S block, it is convenient to assume a specific value of F_s. In the following derivation, the case $F_s = 3$ is assumed. This is the easiest case to handle because it means that each wire segment that enters an S block can connect to exactly one wire segment on each other side. Also, the derivation need not be concerned with whether a connection turns or passes straight through an S block since the effect is the same in both cases. Section 4.2.2 shows how the result can be extended to any value of F_s.

The event $S_1 | X_1$ is depicted in Figure 7, which shows an S block and a routing channel that has W tracks. The figure shows a set of A^{X_1} tracks, drawn as bold lines, that are available at the incoming side of the S block and a set of D tracks, drawn as dashed lines on the outgoing side of the S block, that are already used by other connections. In the figure, $D = 4$, $W = 10$, and $A^{X_1} = 3$. Note that setting A^{X_1} to three corresponds to the event $A_3^{X_1}$, from Section 4.1. Figure 7 uses dotted lines to indicate S block switches and shows that each track on the incoming side of the S block can be connected to one other track on the outgoing side. The S block event can then be considered to be a random process in which each of the A^{X_1} incoming tracks can connect to one track on the outgoing side of the S block, as long as that outgoing track is not among the D used tracks. In other words, given that there are A^{X_1} tracks that are available on the incoming side of the S block, it is necessary to find the probability that one or more of these tracks are also available on the outgoing side.

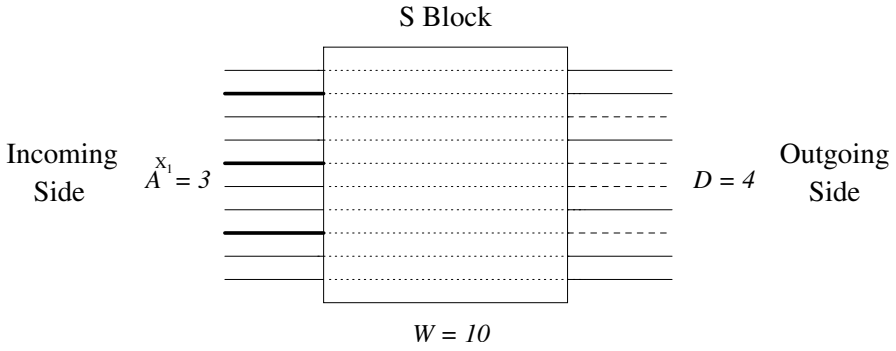

Figure 7 - *The Event* S_1.

The event $S_1 | X_1$ can occur with one or more available outgoing tracks. To calculate $P(S_1 | X_1)$, define $A_1^{S_1}, A_2^{S_1}, \ldots, A_{F_c}^{S_1}$ as the events that $S_1 | X_1$ occurs with exactly 1, 2, …, F_c available tracks on the outgoing side. Since

$$S_1 | X_1 = A_1^{S_1} \cup A_2^{S_1} \cup \ldots \cup A_{F_c}^{S_1}$$

and $A_1^{S_1}, A_2^{S_1}, \ldots, A_{F_c}^{S_1}$ are mutually exclusive

$$P(S_1 | X_1) = P(A_1^{S_1}) + P(A_2^{S_1}) + \ldots + P(A_{F_c}^{S_1}) \qquad 5$$

Solving for each term in this summation requires several steps. Consider the general case where $S_1 | X_1$ occurs with exactly k available outgoing tracks. The corresponding event is written $A_k^{S_1}$. The probability of $A_k^{S_1}$ will depend on the number of tracks available on the incoming side, given by A^{X_1}, and on the value of D. Assume a specific value of $A^{X_1} = a$. Since X_1 is known to have occurred, this corresponds to assuming that X_1 occurred with exactly (a) available tracks. The appropriate statistical event for this assumption is then written as $A_a^{X_1} | X_1$. Also, assume that $D = d$. A conditional probability for $A_k^{S_1}$ can then be expressed using combinatorial analysis as

$$P((A_k^{S_1} | (A_a^{X_1} | X_1)) | D_d) = \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{W-(a-k)}C_k} \cdot {}_aC_k \qquad 6$$

Equation 6 expresses the ratio of the number of ways in which exactly (k) of the (a) available incoming tracks can end up on unoccupied tracks on the outgoing side of the S block to the number of ways in which two distinguishable groups of (k) and (a - k) tracks can appear on any of the W tracks. To expand Equation 6, following the steps outlined in the previous section, consider the events $D_0, D_1, \ldots, D_W$ corresponding to the possible

values of D. Since the occurrence of $(A_k^{S_1} \mid (A_a^{X_1} \mid X_1))$ implies exactly one of $D_0, D_1, \ldots, D_W$, then

$$P(A_k^{S_1} \mid (A_a^{X_1} \mid X_1)) = \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{(W-(a-k))}C_k} \cdot {}_aC_k$$

Next, consider the events $(A_1^{X_1} \mid X_1), \ldots, (A_{F_c}^{X_1} \mid X_1)$ corresponding to the possible values of A^{X_1}. The occurrence of $A_k^{S_1}$ implies exactly one of $(A_1^{X_1} \mid X_1), \ldots, (A_{F_c}^{X_1} \mid X_1)$, so that

$$P(A_k^{S_1}) = \sum_{a=1}^{F_c} P(A_a^{X_1} \mid X_1) \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{(W-(a-k))}C_k} \cdot {}_aC_k \qquad 7$$

As stated above, the terms $P(A_a^{X_1} \mid X_1)$ express the probability that, given the occurrence of event X_1, X_1 occurred with exactly (a) available tracks. Each of $P(A_a^{X_1} \mid X_1)$ is defined by Bayes' rule [14], according to

$$P(A_a^{X_1} \mid X_1) = \frac{P(A_a^{X_1})}{\sum_{j=1}^{F_c} P(A_j^{X_1})} \qquad 8$$

where $P(A_1^{X_1}), \ldots, P(A_{F_c}^{X_1})$ are given by Equation 4. Substituting Equations 7 and 8 into 5,

$$P(S_1 \mid X_1) = \sum_{k=1}^{F_c} P(A_k^{S_1})$$

$$= \sum_{k=1}^{F_c} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\left(\sum_{j=1}^{F_c} P(A_j^{X_1}) \right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{(W-(a-k))}C_k} \cdot {}_aC_k \qquad 9$$

4.2.2 The First S Block Event, for Any Value of F_s

Equation 9 assumes a specific value of S block flexibility, $F_s = 3$. This section shows how Equation 9 can be generalized for other values of F_s. In Equation 6, a one-to-one correspondence was assumed between the subscript (a) in $A_a^{X_1} \mid X_1$, on the left hand side of the

equation, and the variable (a), on the right hand side. This relation holds for $F_s = 3$ but does not necessarily apply for other values of F_s. For example, if $F_s = 6$ a more appropriate variable for the right hand side of the equation is $2a$. In general, the subscript (a) should be scaled by some factor, α, and Equation 6 becomes

$$P(\,(A_k^{S_1} \,|\, (A_a^{X_1} \,|\, X_1)\,) \,|\, D_d) = \frac{{}_dC_{(\alpha a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha a - k)} \cdot {}_{(W-(\alpha a - k))}C_k} \cdot {}_{\alpha a}C_k \qquad 10$$

Clearly, α depends on the value of F_s, but α may also depend on whether a connection passes straight through a particular S block, or turns. Define Z_1 as the event that a connection passes straight through an S block, and Z_2 as the event that it turns. Also, define α_1 and α_2 as the values of α corresponding to Z_1 and Z_2. Since $S_1 | X_1$ implies one of Z_1 and Z_2, then

$$P(S_1 | X_1) = P(Z_1) \cdot P(\,(S_1 | X_1) \,|\, Z_1) + P(Z_2) \cdot P(\,(S_1 | X_1) \,|\, Z_2)$$

and using Equation 9 and 10,

$$P(S_1 | X_1) =$$

$$P(Z_1) \cdot \sum_{k=1}^{W} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\sum_{j=1}^{F_c} P(A_j^{X_1})} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_1 a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_1 a - k)} \cdot {}_{(W-(\alpha_1 a - k))}C_k} \cdot {}_{\alpha_1 a}C_k +$$

$$P(Z_2) \cdot \sum_{k=1}^{W} \sum_{a=1}^{F_c} \frac{P(A_a^{X_1})}{\sum_{j=1}^{F_c} P(A_j^{X_1})} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_2 a - k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_2 a - k)} \cdot {}_{(W-(\alpha_2 a - k))}C_k} \cdot {}_{\alpha_2 a}C_k \qquad 11$$

Appropriate values for $P(Z_1)$ (note that $P(Z_2) = 1 - P(Z_1)$), α_1, and α_2 are discussed in Section 5. Note that the (k) summation in Equation 11 has an upper limit of W, whereas the corresponding upper limit in Equation 9 is F_c. This change is required since it may be possible to connect to all W tracks in a channel for values of F_s that are greater than three.

4.2.3 The Remaining S Block Events

Thus far, this section has dealt specifically with the event $S_1 | X_1$, but the derived expressions are applicable to any of the other S block events, with two changes. First, for the m^{th} S block event, $(S_m | (S_{m-1} \cap \ldots \cap S_1 \cap X_1))$, all summations must reach an

upper limit of W. Second, the probabilities $P(A_1^{X_1}), \ldots, P(A_{F_c}^{X_1})$ in Equation 11 are replaced by $P(A_1^{S_{m-1}}), \ldots, P(A_W^{S_{m-1}})$, which are defined by Equation 12, with $m = m - 1$. Applying these changes, Equation 7 becomes

$$P(A_k^{S_m}) = \sum_{a=1}^{W} P(A_a^{S_{m-1}} \mid (S_{m-1} \cap \ldots \cap S_1 \cap X_1)) \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(a-k)} \cdot {}_{(W-(a-k))}C_k} \cdot {}_aC_k \qquad 12$$

and Equation 11 becomes

$$P(S_m \mid (S_{m-1} \cap \ldots \cap S_1 \cap X_1)) =$$

$$P(Z_1) \cdot \sum_{k=1}^{W} \sum_{a=1}^{W} \frac{P(A_a^{S_{m-1}})}{\left(\sum_{j=1}^{W} P(A_j^{S_{m-1}}) \right)} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_1 a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_1 a-k)} \cdot {}_{(W-(\alpha_1 a-k))}C_k} \cdot {}_{\alpha_1 a}C_k +$$

$$P(Z_2) \cdot \sum_{k=1}^{W} \sum_{a=1}^{W} \frac{P(A_a^{S_{m-1}})}{\sum_{j=1}^{W} P(A_j^{S_{m-1}})} \cdot \sum_{d=0}^{W} p(\lambda_g, d) \cdot \frac{{}_dC_{(\alpha_2 a-k)} \cdot {}_{(W-d)}C_k}{{}_WC_{(\alpha_2 a-k)} \cdot {}_{(W-(\alpha_2 a-k))}C_k} \cdot {}_{\alpha_2 a}C_k \qquad 13$$

4.3 The C Block to Logic Block Event

The event X_2 is depicted by Figure 8, which shows a set of $A^{S_n} = 4$ tracks, drawn as bold lines, that are available at a C block (this corresponds to the event $A_4^{S_n}$ in Section 4.2) and a set of $F_c = 5$ tracks that connect to the appropriate logic block pin for the connection. The event X_2 can then be viewed as a random process in which the logic block pin can be connected to any of the set of A^{S_n} tracks where there are switches. Stated differently, given that one or more tracks were available at the outgoing side of the last S block, it is necessary to determine the probability that one or more of these tracks connects to the appropriate logic block pin. To simplify the notation, the expression $S_n \cap \ldots \cap S_1 \cap X_1$ will be substituted for by SX. To calculate the probability of $X_2 \mid SX$, define the opposite event $NONE \mid SX$, where $P(X_2 \mid SX) = 1 - P(NONE \mid SX)$. To find $P(NONE \mid SX)$, assume

a specific value of $A^{S_n} = a$ and define the corresponding event $A_a^{S_n} \mid SX$. A conditional probability for $NONE \mid SX$ can then be defined by

$$P((NONE \mid SX) \mid (A_a^{S_n} \mid SX)) = \frac{(W - F_c)C_a}{{}_W C_a} \qquad 14$$

Equation 14 assumes that each of the F_c switches for the logic block pin associated with event X_2 is equally likely to be on any of the W tracks. This may not be realistic since a good C block would be designed to ensure that the tracks that are connectable to one pin would overlap the tracks connectable to others. A detailed discussion of this issue can be found in [10]. This inaccuracy in Equation 14 will have the effect of producing low predictions of routability for low values of F_c, which is discussed further in Section 5.1.

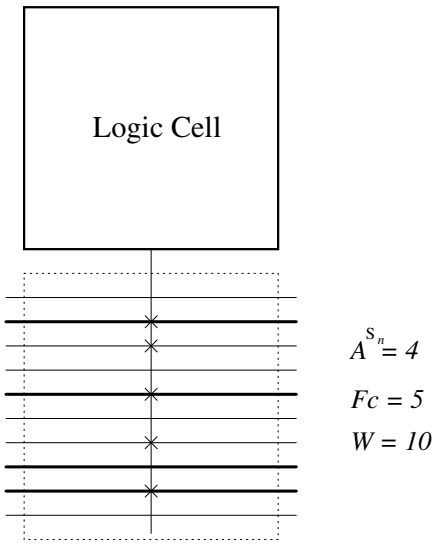

Figure 8 - *The Event X_2.*

Consider the events $A_1^{S_n}, A_2^{S_n}, \ldots, A_W^{S_n}$ corresponding to the possible values of A_n^S. Since the occurrence of $NONE \mid SX$ implies exactly one of $A_1^{S_n}, A_2^{S_n}, \ldots, A_W^{S_n}$, it follows that

$$P(NONE \mid SX) = \sum_{a=1}^{W} P(A_a^{S_n} \mid SX) \cdot P((NONE \mid SX) \mid (A_a^{S_n} \mid SX))$$

where each of $P(A_a^{S_n} \mid SX)$ is given by Bayes' rule, so that

$$P(X_2|\,SX) \;=\; 1 - P(NONE|\,SX) \;=\; 1 - \sum_{a\,=\,1}^{W} \frac{P(A_a^{S_n})}{\left(\sum_{j\,=\,1}^{W} P(A_j^{S_n})\right)} \cdot \frac{{}^{(W\,-\,F_c)}C_a}{{}_{W}C_a} \qquad 15$$

Each of $P(A_1^{S_n})$, …, $P(A_W^{S_n})$ can be calculated using Equation 12, with $m = n$. Note that for the case of a connection that has length one, there are no S block events, so that $A_a^{S_n}$ in Equation 15 are replaced by $A_a^{X_1}$. Each of $P(A_1^{X_1})$, …, $P(A_{F_c}^{X_1})$ can be calculated using Equation 4.

4.4 The Probability of R_{C_i}

Equation 1 can now be solved using the expressions developed in this section to calculate $P(R_{C_i})$, for the given value of $LC_i = n + 1$. Equation 1 is reproduced below, as Equation 16.

$$\begin{aligned} P(R_{C_i}|\,L_{n+1}) \;&=\; P(X_1 \cap S_1 \cap S_2 \cap \ldots \cap S_n \cap X_2) \\ &=\; P(X_1)P(S_1|\,X_1)P(S_2|\,S_1 \cap X_1)\ldots P(S_n|\,S_{n-1} \cap \ldots \cap S_1 \cap X_1) \cdot \\ &\quad\; P(X_2|\,S_n \cap \ldots \cap S_1 \cap X_1) \end{aligned} \qquad 16$$

To make use of this result to calculate $P(R_{C_i})$, define $LC_i = l_{max}$ as the maximum length of any connection and $L_{l_{max}}$ as the corresponding event. Appropriate values for l_{max} are discussed in Section 5. Next, consider the events L_1, …, $L_{l_{max}}$ corresponding to the possible values of LC_i. Since the occurrence of R_{C_i} implies exactly one of L_1, …, $L_{l_{max}}$, then

$$P(R_{C_i}) \;=\; \sum_{l\,=\,0}^{l_{max}} P(L_l) \cdot P(R_{C_i}|\,L_l) \qquad 17$$

where $P(L_l)$ are given by the probability distribution of connection length, referred to in Section 2 as P_L, and each $P(R_{C_i}|\,L_l)$ is defined by Equation 16. As mentioned in Section 2, P_L is assumed to be geometric, with mean $\overline{R}$. Thus, $P(L_l)$ is given by

$$P(L_l) \;=\; pq^{l\,-\,1}$$

where $p = \frac{1}{\overline{R}}$ and $q = 1 - p$. The following section shows how Equation 17 is evaluated to predict routability.

5 Using the Stochastic Model to Predict Routability

In order to make use of Equation 17, it is necessary to choose appropriate values for the various parameters that appear in the expressions developed in Section 4, as well as to evaluate the function λ_g, that is used to predict channel densities. This section first shows how λ_g is calculated and then gives appropriate values for each of the parameters. The routability predictions produced by the stochastic model are then presented, and are validated by comparisons with the results of an experimental study that has been previously published [2].

As stated in Section 3, the parameter λ_g is defined by $\lambda_g = (\lambda\overline{R})/2$, where $\overline{R}$ is the average connection length and λ is the ratio of the expected number of routed connections to the total number of logic blocks. Given this definition, λ must be re-calculated after each connection is probabilistically 'routed' by the stochastic process. Thus, after $i-1$ connections have been 'routed', λ can be calculated as

$$\lambda = \frac{1}{N^2}\sum_{c=1}^{i-1} P(R_{C_c}) \qquad 18$$

It is necessary to assign values to the following parameters: N, W, l_{max}, C_T, $\overline{R}$, $P(Z_1)$, α_1, α_2, F_s, and F_c. The first three of these depend on the size of the FPGA array and the next three are determined by the characteristics of the circuit to be routed. The routability predictions that are generated here will be compared with the results from a previously published experimental study, so the parameters will be taken from the FPGA circuits that were used there [2]. The corresponding values are listed in Table 1. Note that some of

Circuit	N	W	l_{max}	C_T	$\overline{R}$	$P(Z_1)$
BUSC	11	11	20	392	2.7	.71
DMA	15	12	28	771	2.8	.75
BNRE	20	14	38	1257	3.0	.75
DFSM	21	13	40	1422	2.85	.76
Z03	25	13	48	2135	3.15	.75

Table 1 - *Stochastic Model Parameters for Experimental Circuits.*

these parameters did not appear in the original paper [2], but the values in Table 1 have all been measured from the actual circuits.

	F_s									
	2	3	4	5	6	7	8	9	10	…
α_1	1.0	1.0	2.0	2.0	2.0	3.0	3.0	3.0	4.0	…
α_2	0.5	1.0	1.0	1.5	2.0	2.0	2.5	3.0	3.0	…

Table 2 - *Approximations to* α_1 *and* α_2.

The parameters α_1 and α_2 can be approximated by making some assumptions concerning the topology of the S blocks. It is assumed here that the topology is similar to the one used in [2]. This means that as F_s is increased from its minimum value of 2, switches are added to the wire segments in the order straight across, right turn, left turn, straight across, right turn, etc. It is further assumed that the topology spreads the switches among the tracks such that every wire segment can be switched to exactly F_s others. Given these assumptions, appropriate values for α_1 and α_2 are shown in Table 2.

5.1 Routability Predictions

Recall, from Section 2, that routability is defined as

$$\text{Routability} = \frac{1}{C_T}\sum_{i=1}^{C_T} P(R_{C_i}). \qquad 19$$

This equation can now be evaluated using Equation 17, the expressions developed in Section 4, Equation 18, and Tables 1 and 2. A typical result is shown in Figure 9, which gives a plot of the expected percentage of successfully completed connections versus connection block flexibility, F_c, for parameters that correspond to the circuit called BNRE. Each curve in the figure corresponds to a different value of S block flexibility, F_s. The lowest curve represents the case $F_s = 2$ and the highest curve corresponds to $F_s = 10$. The figure indicates that the routability is low for small values of F_c and only approaches 100% when F_c is at least one-half of *W*. The figure also shows that increasing the S block flexibility improves the completion rate at a given F_c, but to get near 100% the value of F_c must always be high (above 7 for this circuit). These conclusions are the same as those reached in the experimental study described in [2].

Figure 10 is a plot of the expected percentage of successfully completed connections versus S block flexibility, F_s, also for the circuit BNRE. This plot represents the same data

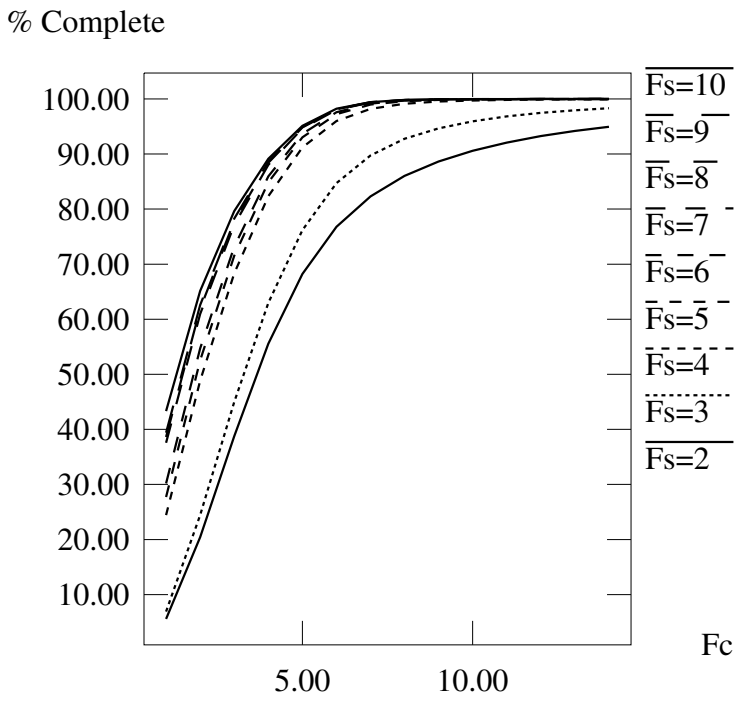

Figure 9 - *Routability Predictions vs. F_c, for Circuit BNRE.*

as that shown in Figure 9 but a different insight is provided by plotting F_s along the x-axis, instead of F_c. Each curve in the figure corresponds to a different value of F_c, with the lowest curve representing $F_c = 1$ and the highest curve corresponding to $F_c = W$. The curves show an increase in slope at F_s values of 4, 7, and 10. This occurs because switches are added straight across the S blocks for these values of F_s and, as Table 1 shows, connections pass straight through the S blocks more than 70 percent of the time.[1] It is clear from Figure 10 that if F_c is at least one-half of *W*, then very low values of F_s approach 100% routability.

While the theoretical and experimental results lead to the same general conclusions, they are not identical. Figure 11 directly compares the routability results produced by the stochastic model with the experimental results from [2]. The solid curve corresponds to the result published in [2] whereas the dashed curve is produced by the stochastic model. Both curves correspond to circuit BNRE, with $F_s = 6$. As Figure 11 indicates, the two results are quite similar. The fact that the theoretical curve is lower than the experimental one for low values of F_c is due in part to Equation 14, which, as discussed in Section 4, does not accurately represent how a good C block topology would perform. A summary of comparisons between theory and experiment for all the circuits appears in Table 3. For

1. Note that whether each added switch corresponds to a turn or a straight-through connection depends on the values used for α_1 and α_2. The reason for choosing the values shown in Table 2 is that this corresponds to the way that switches were added in the experimental study to which the predictions from the stochastic model are being compared.

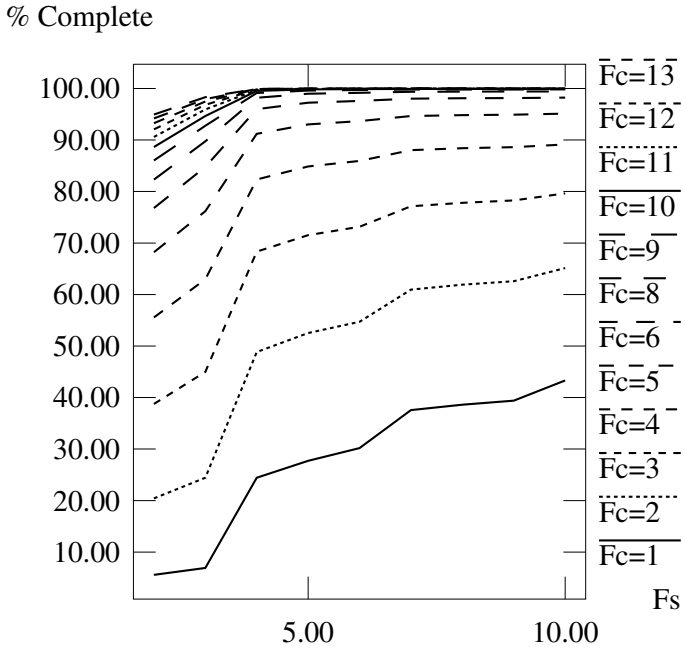

Figure 10 - *Routability Predictions vs. F_s, for Circuit BNRE.*

each circuit, the table shows the difference between the theoretical and experimental routability results, for each value of F_s. Each entry gives the mean value (and standard

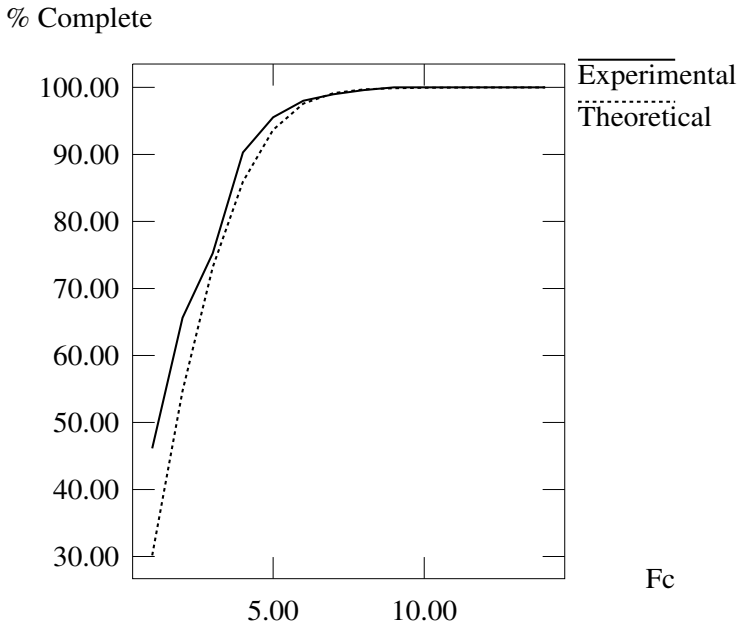

Figure 11 - *Comparison of Predictions and Experiments, for $F_s = 6$.*

deviation) of the difference, over the range of values of F_c from 1 to *W*. The values in the table are in percentages since those are the units of routability. Absolute values are used in the table to avoid a misleading average that could be caused by combining negative and positive differences. However, this is not really necessary since, as Figure 11 indicates, the theoretical predictions are almost always pessimistic. As Table 3 shows, the experimental measurements and theoretical predictions of routability are close, especially for values of F_s greater than three.

	BUSC		**DMA**		**BNRE**		**DFSM**		**Z03**	
F_s	Mean	S.D.	Mean	S.D.	Mean	S.D.	Mean	S.D.	Mean	S.D.
2	7.7	4.9	10.2	7.5	7.3	6.3	8.9	8.3	7.2	5.9
3	9.7	5.6	12.5	8.1	8.7	6.7	10.8	9.4	10.2	5.6
4	2.9	2.9	4.1	4.5	1.5	3.1	2.7	5.3	1.9	2.1
5	3.7	4.3	4.9	5.8	2.4	4.3	3.7	6.1	1.8	2.7
6	3.2	3.5	5.0	6.2	2.6	4.7	4.0	6.7	2.1	3.3
7	4.8	4.3	5.1	6.6	2.8	4.3	3.9	6.1	1.8	2.8
8	4.3	4.6	5.1	6.5	3.1	4.3	4.1	6.2	2.2	2.6
9	4.3	4.9	5.0	6.3	3.2	4.4	4.2	6.2	2.5	3.0
10	4.3	4.8	5.2	6.7	3.2	4.3	4.2	5.9	2.9	3.4

Table 3 - *Summary of Comparisons Between Theory and Experiment.*

5.1.1 Practical Use of Routability Predictions

The routability predictions produced by the stochastic model can be viewed as the likelihood of successfully routing a circuit. In this context, routability is useful as a means of making the binary decision of whether or not a particular circuit can be routed in an FPGA with a given routing architecture. Making this decision requires the selection of a minimum value of routability for which a circuit should be deemed routable. In [11], Heller et. al. suggest that this minimum value should be at least 90 percent, but that for large circuits it may be better to specify an absolute number of failed connections rather than a percentage. However, Heller's results are based on mask-programmed chips so they should not be blindly applied to FPGAs. Comparisons with experimental results indicate that routability should be at least 95 percent in order for a circuit to be deemed routable in an FPGA, but this is based on a small set of examples. More research should be carried out to decide what minimum value of routability is applicable to a wide range of circuits. Also, this value is likely to vary depending on the flexibility of the FPGA's routing structures.

6 Conclusions and Future Work

This paper has described a stochastic model that can be used to study the effect of the flexibility of an FPGA's routing architecture on its routability. It has been shown that the model can be used to reach the same conclusions that were generated in a previous paper using an experimental approach. In future work the model should be extended to handle the case where some of the routing switches in the S blocks are replaced by hard-wired connections. This would allow the modelling of routing architectures in which the tracks may be composed of segments of various lengths and would allow the stochastic model to be used to study such architectures.

It was illustrated in Section 5.1 that the routability predictions produced by the stochastic model are pessimistic. Part of the reason for this may be that the model assumes that all connections to be routed are influenced in a statistical way by all others so that any connection has a non-zero chance of failure. This does not truly correspond to an actual circuit, in which a large percentage of the connections are trivial to route and only a small number have a chance of failure due to interference with other connections. It would be interesting to see how the stochastic model could be modified to account for the fact that most of the connections in a circuit are trivial to route, while still handling the important side effects for the difficult connections.

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