SYNTHETIC CIRCUIT GENERATION USING CLUSTERING AND ITERATION

by

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Graduate Department of Electrical and Computer Engineering

University of Toronto

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ABSTRACT

The development of next-generation CAD tools and FPGA architectures require benchmark circuits to experiment with new algorithms and architectures. There has always been a shortage of good public benchmarks for these purposes, and even companies that have access to proprietary customer designs could benefit from designs that meet size and other particular specifications. In this thesis, we present a new method of generating realistic synthetic benchmark circuits to help alleviate this shortage. The method significantly improves the quality of previous work by imposing the natural hierarchy of circuits through clustering and by using a simpler method of characterizing the nature of sequential circuits. Also, in contrast to current constructive generation methods, we employ new iterative techniques in the generation that provide better control over the generated circuit's characteristics. As in previous work, we assess the realism of the generated circuits by comparing properties of real circuits and generated "clones" of the real circuit after placement and routing. On average, the real and clone circuits' total detailed wirelength differed by only 14%, a major improvement over previous results. In addition, the minimum track count was within 14% and the critical path delay was within 10%.

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GLOSSARY

API

Application Programming Interface. A method of interfacing to another program

ASIC

Application Specific Integrated Circuit

Binary Tree Distribution

A probability mass function built by using a balanced binary tree

Bi-partitioning

Dividing a circuit by repeated bisection

BLIF

Berkeley Logic Interchange Format

CAD

Computer Aided Design

Circ

A software tool that Mike Hutton built to characterize circuits.

Clones

Synthetic circuits generated from the unchanged characterization of the original circuits

Comb

A matrix that measures the number inter-cluster connections to combinational nodes

Combinational Delay Structure

The part of the delay structure that contains connections to combinational nodes

Delay Level

The maximum delay over all directed paths beginning at a primary input or a flip-flop

Delay Structure

A graph *G = (Level Nodes, Super Edges)*

d_{max}

The maximum combinational delay over all nodes in a circuit

DFF

A flip-flop

DFF edge

An edge that connects to the input of a flip-flop

E

The set of edges in a graph G = (V,E)

Edge Length

For an edge *e=(x,y)* with nodes *x* and *y* the *length(e) = delay_level(y) - delay_level(x)* if *delay_level(y) > delay_level(x)*, and 0 otherwise

Edge Length Distribution

The number of edges at each edge length

Edge Rotation

Relocating an edge to a new sink node

Edge Swap

Swapping an edge between two source nodes

Fanout

The number of connections to combinational nodes

Fanout Assigned Delay Graph Structure

The delay structure with where the level nodes have been assigned fanouts for their individual nodes

Fanout Distribution

The number of nodes of each fanout, starting at 0

FPGA

Field Programmable Gate Arrays

Gen

A software tool that Mike Hutton built to generate synthetic circuits

Ghost Input Shape

A shape measurement of the number of edge entering a sequential level

Ghost Output Shape

A shape measurement of the number of edge leaving a sequential level

GIshape

see Ghost Input Shape

GOshape

see Ghost Output Shape

hMetis

A partitioner

Individual Node

A node in the graph. A future gate in the circuit.

Intra-cluster Edge Length Distribution

The number of edges internal to a cluster at each edge length

Inter-cluster Input Edge Length Distribution

The number of inter-cluster inputs into a cluster at each edge length

Inter-cluster Output Edge Length Distribution

The number of inter-cluster outputs out of a cluster at each edge length

Input Shape

A measurement of shape for the number of inputs into each delay level

Latched

A matrix that measures the number latched node to flip-flop connections between clusters

Latched Node

A node that outputs to a flip-flop

Latched Shape

A measurement of shape for the number of latched nodes at each delay level

Level Nodes

An aggregation of individual nodes at a delay level

Long Edge

An edge of length greater than one

LUT

Look-up Table

k-way Partitioning

Dividing a circuit into k-clusters

MCNC

An organization that published a benchmark circuit suite

NCirc

A software tool built to characterize circuits

Netlist

A circuit represented as a list of gates and a list of the connections between the gates

NGen

A software tool built to generate synthetic circuits

Node Shape

A measurement of shape for the number of nodes at each delay level

Node Violation

A node with one or more of the following properties: no outputs, no inputs, too many inputs, two or more connections from the same source node, or a connection to itself.

Output Shape

A measurement of shape for the number of inputs into each delay level

PI

Primary Input

PO

Primary Output

PO Shape

A measurement of shape for the number of primary outputs at each delay level

Pre-Edge Assignment Structure

The delay structure ready for final edge assignment

V

The set of nodes in a graph G = (V,E)

Sequential Levels

A method of modeling sequential circuits as chains of combinational logic that are connected to the next stage by flip-flops and are connected to any previous stage by feedback connections.

Shape

A measurement made over the delay levels in a circuit or a cluster of a circuit

Super Edge

An aggregation of edges between two level nodes with weight equal to the number of edges

Unit Edge

An edge of length one

VPR

An FGPA place and route tool

VLSI

Very Large Scale Integration

1 INTRODUCTION

There currently exists a shortage of good quality public-domain benchmark circuits that can be used to test the next generation of CAD algorithms for VLSI ASICs and FPGA architectures. Most public domain benchmarks are either too small or not of the right size to give a realistic assessment of the performance of new architectures and algorithms.

The shortage of large circuits exists because companies that possess large circuits regard them as proprietary. A number of efforts have been made to assemble public domain benchmarks, but those that do exist tend to be small or lack crucial information [1-3]. For example, the largest circuits from the MCNC benchmarks [1], common benchmarks used for FPGA research, are on the order of 8000 four-input look-up tables (4-LUT)s. By contrast, the largest planned FPGAs that will be available within a year from Altera and Xilinx have space for up to 114,140 [4] and 104,832 [5] 4-LUTs respectively. This means that the circuits used to evaluate FPGA algorithms and architectures in the research community take up less than 10% of the largest commercial FPGA's area. Furthermore, if the research community is to explore FPGA designs that are five to ten years in the future then circuits that are three to twelve times larger are needed as chip size is forecast to grow by that amount according to the International Technology Roadmap for Semiconductors [6].

This shortage of larger circuits is even more acute when one considers that what is really needed to fully test FPGA architectures or algorithms are larger circuits of the *right size*. In testing, a circuit that consumes half the logic resources of the target FPGA is often not as interesting as a circuit that consumes 90% of an FPGA and places large demands on the architecture or the

CAD tool algorithms. Furthermore, unlike research into ASICs, if the benchmark circuit does not fit into the FPGA, then that benchmark circuit is of no use for testing purposes.

Recently, researchers have proposed several approaches to *synthetic* benchmark generation in an attempt to alleviate these problems. Synthetic benchmarks are netlists created by an automated program and are constrained to have a specific set of desirable characteristics. However, for synthetic circuits to be useful, they must be shown to be realistic proxies for real circuits.

Hutton et al. [7,8] demonstrated realism by comparing real benchmark circuits to "clones" generated synthetically from the characterization of the real circuits. The real and clone circuits are compared on the basis of an important circuit characteristic or property (such as power consumption, critical path delay or total wirelength after placement and routing) that was *not* constrained as part of the synthetic generation process. The circuit characteristic that was used for comparison was post-place and route wirelength. Against this metric Hutton et al. were successful in generating good quality clones of circuits that were purely combinational, but the approach did not work as well for the larger sequential circuits. For sequential circuits it was found that the clones used too much wirelength over the real circuits and hence were unrealistic from that perspective.

We believe that the reasons why Hutton's method generates sequential circuits that are too difficult to place and route are two-fold: First, we suspect the sequential circuits generated lack the natural hierarchy of organization that can be found in real circuits [9]. This natural hierarchy exists because designers tend to build circuits hierarchically in clumps in order to deal with complexity [10]. For combinational circuits, this natural hierarchy is not as evident because the circuits tend to be small and therefore do not require multiple levels of hierarchy to design. For the larger sequential circuits however, design hierarchy is necessary and we believe that the natural hierarchy that results from it is not captured in characterization or imposed in generation in Hutton's method and as a result the sequential synthetic circuits are unrealistic. Second, we

believe that Hutton's sequential circuit model is not a natural circuit model for sequential circuits and results in the wrong circuit structure being characterized and generated.

In this work, we set out to improve the results for sequential circuits three ways: First, we designed a simpler and more intuitive sequential circuit model that maintains the key strength of Hutton's work, which is ability to directly specify the unit delay profile of the synthesized circuits. Second, we characterize the natural hierarchy in circuits and incorporate this hierarchy into generation. The natural hierarchy in a circuit is identified by partitioning the circuit into strongly connected clusters. After partitioning, the natural hierarchy is captured by characterizing the structure of connections between and within the clusters. Third, we use an iterative approach in the generation algorithms to achieve better control over the generation process, which allows us to produce synthetic circuits whose properties are closer to the properties of the real circuits that we characterize.

1.1 THESIS OVERVIEW

This thesis is organized as follows: in Chapter 2, we review previous work in synthetic circuit generation, including Hutton et al., upon which this research is based. In Chapter 3, we describe the new clustered circuit model and new characterization that will improve the generation results. In Chapter 4, we describe the new generation algorithms that mesh with the new characterizations. In Chapter 5, we present the results that demonstrate the increased realism of our synthetic circuits and the effect that clustering and iteration have on the quality of synthetic circuits. We conclude and present avenues of future research in Chapter 6.

2 BACKGROUND AND PREVIOUS WORK

This chapter provides the background of the work of Hutton et al. [7,8] upon which this research is based. This is followed by a review of other circuit generators that exist in the literature.

2.1 Hutton's Characterization and Generation

The first work of Hutton et al. [7] was to characterize key physical circuit properties of combinational circuits and then to generate synthetic circuits that are constrained to have these properties. When the properties of the original circuits are unchanged, these generated circuits are called *clones* of the original circuit. Examples of physical properties include the fanout distribution of the gates of the original circuits, the delay structure, and the number and type of connections in the circuit. In [8], Hutton extended his method to generate sequential circuits, with flip-flops. In the sections below, we first define the combinational circuit model and definitions. Second, we discuss the set of circuit characterizations and the method of combinational synthetic circuit generation. Third, we provide a brief description of the extensions made for sequential circuits. Lastly, we describe the process by which the circuits are judged realistic and reprise Hutton's results.

2.1.1 Circuit Model and Definitions

Circuits are modeled as a directed acyclic graph $G = (V,E)$ where the nodes V represent gates in the circuit and edges E represent two-point connections between gates. In order to reduce the

wide variation of gate types, both Hutton and this work assumes all gates are 4-input lookup tables (4-LUTs).

A key concern of modern digital design is the speed at which circuits operate and therefore a central principal of Hutton's work is to control the delay of the synthetic circuits. He employed the unit delay model in which every gate incurred a single unit of delay. With this delay model, the *delay level* of a node in the graph is defined as the maximum delay over all directed paths beginning at a primary input (PI) or a flip-flop (DFF) and terminating at the given node. The maximum combinational delay over all nodes in a circuit is defined as d_{max}.

The delay structure of the circuit is characterized by a collection of measurements at the various delay levels. *Shape* is defined as the number of objects at each delay level. Accordingly, Hutton defines *node shape*, *input shape*, *output shape*, and *PO shape* as the total number of nodes, inputs, outputs, and primary outputs (POs) at each delay level respectively. The concept of shape is illustrated in Figure 2.1 for the MCNC circuit cm151a. The graph of the circuit shows the nodes arrayed and labelled by delay level. Figure 2.1 also gives a histogram of node, input, output, and primary output shapes. Primary inputs, which occupy the 0th delay level, are labelled PI. Looking at the 1st delay level we see it has 4 nodes, 16 inputs from the 0th delay level, and 4 outputs, and no primary outputs.

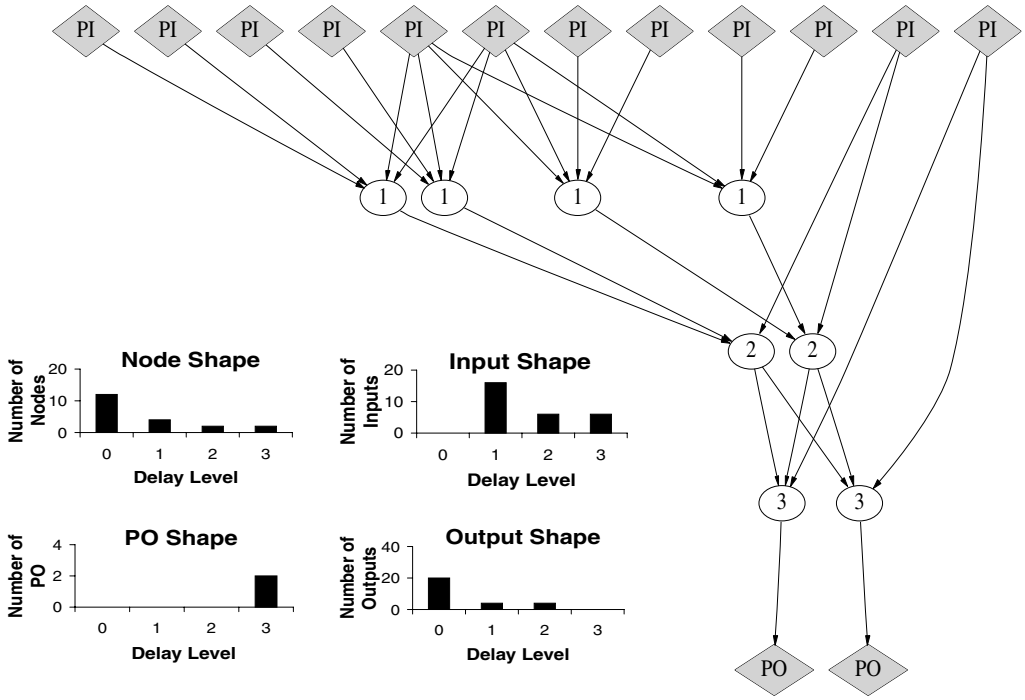


Figure 2.1 - Circuit and Shape Functions

For a node *x*, *fanout(x)* is the combinational output degree of the node. For a circuit Hutton describes the fanout in terms of the *fanout distribution,* defined as the number of nodes of each fanout, starting at 0.

To characterize the connections in the combinational circuit, Hutton defines an *edge length* property: For an edge *e=(x,y)* with nodes *x* and *y* he defines the *length(e) = delay_level(y) - delay_level(x)* if *delay_level(y) > delay_level(x)*. An edge of length 1 is termed a *unit edge* while any edge with a length greater than 1 is termed a *long edge.* Using this definition of length Hutton defines the *edge length distribution* as the number of edges at each edge length.

2.1.2 Combinational Generation Algorithms

Hutton's method of generating combinational circuits proceeds in a few basic steps as illustrated in Figure 2.2 (modified from [7]). The input into the generation phase is the node shape, the fanout distribution, the edge length distribution and several other parameters that are

omitted here for simplicity. In the algorithm, nodes are organized by delay level into larger groupings called *level nodes.* In Step I, the input shape's and output shape's upper and lower bounds are computed at each level node. In Step II, the majority of edges are assigned between the level nodes. In Step III, the fanout distribution is partitioned among the level nodes. In Step IV, each level node is split into individual nodes with a specific fanout. In Step V, edges are assigned between individual nodes.

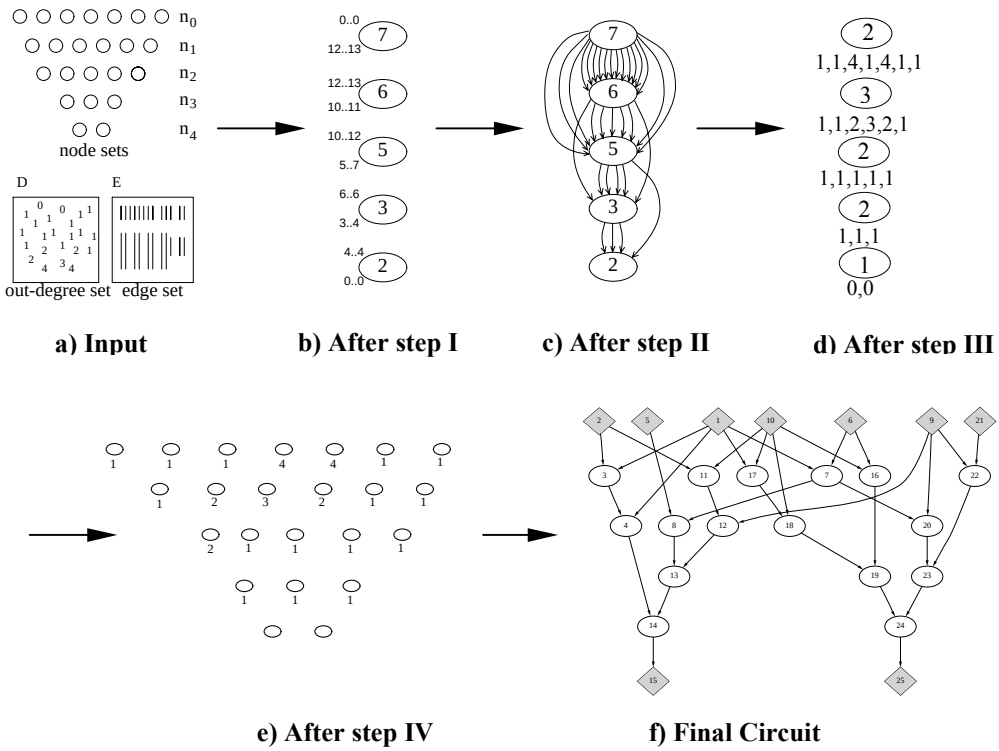


Figure 2.2 - Combinational Generation Algorithm [7]

It is at this point that Hutton attempts to achieve realistic wirelengths in the final generated circuit by imposing a notion of "locality" on the edge assignments. Here each node at each delay level is assigned a horizontal position, and edges are chosen in such a way as to minimize the horizontal distance between joined nodes. Hutton found that deterministically always choosing the closest nodes for each edge assignment produced combinational synthetic circuits

that were too easy to place and route and so he introduced an element of randomness into edge assignment. Hutton assigns edges by choosing a destination node and connecting it to the closest source node chosen from a random sample of *L* potential source nodes where L is a parameter input into the generation process. Hutton found that by choosing the right L he could produce good wirelength for combinational circuits in practice. However, no method was found to adequately characterize this number and Hutton found the lack of connection between characterization and generation theoretically displeasing.

The output from the process, ideally, is a graph where the specified size, distributions and shape functions are met. For example, each node should have a fanout value from the fanout distribution that matches its number of output edges and each node should belong to the correct delay level as dictated by the shape function. Furthermore, there are no *node violations,* defined as nodes that have one or more of the following properties: no outputs, no inputs, too many inputs, or two or more connections from the same source node. Hutton et al. showed that it was often difficult to precisely meet the specification as given, and that it was difficult to prevent all node violations. In order to deal with this, they reduced the length of edges and fanout values, dropped the edges during Step V that could not find valid connections, and assigned primary outputs to nodes with no output edges.

It is relevant to note that this generation approach was largely constructive: at each Step, an assignment is made based on a calculated ordering, which was in turn based on a specific cost metric. In the present work, we propose a new method that iterates over potential choices ripping up connections and replacing them while maintaining an ensemble cost function that attempts to address all of the generation goals.

2.1.3 Extensions for Sequential Circuits

In Hutton et al. [8], the above method of generating combinational circuits was extended to generate sequential circuits. The method was extended by breaking a sequential circuit into combinational sub-circuits separated by flip-flops that could be characterized and generated separately and then “glued” together during generation to form a full circuit.

The combinational sub-circuits are identified by thinking of sequential circuits as consisting of chains of combinational logic that are connected to the next stage by flip-flops and are connected to any previous stage by feedback connections. To find these combinational sub-circuits the nodes in a circuit are partitioning into groups, termed *sequential levels,* based on the *sequential level numbers* of the nodes. The sequential level number of a node x, *sequential_level (x)*, is defined as *0* if x is a Primary Input, *1 + sequential_level (y)* for a flip-flop x with input y, and *MIN(sequential_level(y_i))* over all inputs y_i to x otherwise. In combinational circuits, there is a single sequential level. In sequential circuits, the sequential levels form a hierarchy. An example of this abstract model of a sequential circuit is given in Figure 2.3 [8].

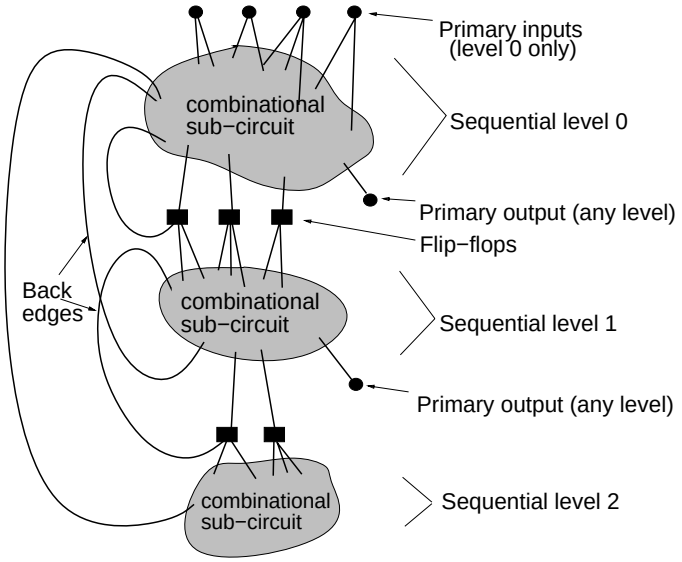


Figure 2.3 - Hutton Model of a Sequential Circuit [8]

With the circuit broken into a hierarchy of sequential levels, Hutton's combinational characterization is applied to each sequential level with extra characterization added to model flip-flop and feedback connections that cross sequential level boundaries. Hutton characterizes the connections that enter or leave each sequential level with the *ghost input shape* (GIshape) defined as the number of edges entering a sequential level at each delay level and the *ghost output shape* (GOshape) defined as the number of edges that exit from a sequential level at each delay level.

Hutton generates synthetic sequential circuits in two steps: In Step I, the combinational logic at each sequential level is generated separately by the method in Section 2.1.2 above with modifications made to choose the set of nodes for flip-flop connections and the set of nodes for feedback connections from the ghost input and output shapes. In Step II, the sequential levels are connected together first, by connecting each sequential level to the flip-flops at the next sequential level and second, by connecting each sequential level to the previous sequential levels by randomly making feedback connections. In Step II, the nodes connected for flip-flop connections or feedback connections are chosen from the respective sets.

The key disadvantage of Hutton's sequential circuit model is that while sequential levels may map nicely to a strictly pipeline circuit, it is not natural for most other forms of circuits and result in the wrong structure being characterized and generated.

2.1.4 Quality of Hutton's Synthetic Circuits

In [7] and [8] the quality of the synthetic circuits produced were judged by comparing real circuits and clone circuits. This process of judging real circuits against their clones is called *validation* and is illustrated in Figure 2.4.

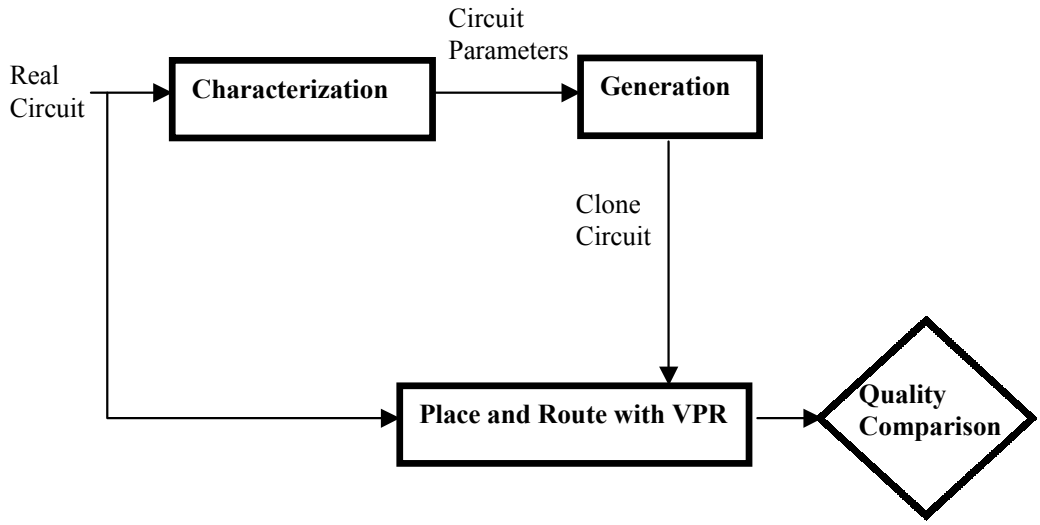


Figure 2.4 -Validation Process

In [7] and [8] the real and clone circuits were validated based on post-place and route routability. Circuits were placed and globally routed using VPR [11,12] and two routability metrics measured. The first, and most important metric, was the total wirelength of the global routing, which is the sum over all nets of the number of segments needed to route the FPGA. The second metric was the minimum number of tracks per channel in the FPGA needed to successfully route the circuit.

For combinational circuits, it was found that the average of the absolute difference in wirelength was 17% while the average absolute difference in the minimum number of tracks was 14%. For sequential circuits, it was found that the average of the absolute difference in wirelength was 40% while the average absolute difference in the minimum number of tracks was also 40%. Note that for the sequential circuits, in almost all cases, the wirelength of the clone circuit was *greater* than that of the original circuit

While the quality of synthetic combinational circuits generated was reasonably good, the quality of sequential circuits generation is too poor to be used as reasonable proxies in FPGA architecture development. Hutton et al. [8] suspected that the reason behind the wirelength differences is that the generated circuits lack the natural hierarchy that can be observed in typical circuits. The purpose of the present research is to impose that hierarchy on the generated circuits, with the goal of improving this wirelength result.

2.2 Other Generation Efforts

A number of other synthetic circuit generators have recently been proposed in the literature [13-20], which we review below.

2.2.1 Generating Circuits Top Down

Darnauer and Dai [13], generate synthetic circuits with a fixed number of inputs, outputs, LUTs, and with an average fanin and approximate Rent exponent [9]. The method constructs the synthetic circuit by recursively bi-partitioning the circuit and making connections after each

partition until the clusters consist of single LUTs. The method is notable in its attempt to capture the hierarchical nature of a circuit. However, the approach lacks control over the fanout and unit delay profile of gates in the circuit. No validation is done on the quality of the synthetic circuits generated as the work focused on determining the routability of the synthetic circuits with given input parameters.

2.2.2 Generating Circuits by Transformation

Iwama et al. [14], create synthetic benchmark circuits using functional transformations of pre-existing real circuits that preserve the logical function of the circuit. While the resulting circuit is "realistic" from a logical standpoint, the method suffers from a lack of control over the physical properties of the netlist and the need for prior circuits. In [15] the method was extended to limit the fanin values of gates in the circuits but the lack of control over physical properties still remains. To alleviate the need for a prior circuit, a trivial random circuit generator was also described that generates single sum-of-product term circuits. No validation was done on any of the synthetic circuits as the application of their work was towards evaluating the ability of synthesis tools to reoptimize circuits they transform.

2.2.3 Generating Circuits by Mutation

Harlow and Brglez [16] and Ghosh et al. [17,18], propose the idea that synthetic circuits should be generated by characterizing properties about circuits that will remain invariant under transformations or "mutations" of the circuits. The focus of their work is towards removing the influence that different starting conditions have on the testing of algorithm performance. They claim that by expanding each circuit used in testing into an equivalence class of mutant circuits and averaging over the experimental results they can negate the effect of different starting conditions. The advantage of this approach is that the circuits are not completely random. However, the approach does not lend itself to the possibility of scaling the mutants to larger circuit sizes, which is the main motivation behind synthetic circuit generation. Furthermore, they present their results based on a small number of small-sized circuits and thus it is unclear how their method performs for larger circuits.

2.2.4 Generating Circuits based on Logic Types

Pistorius et al. [19] characterize digital designs as consisting of two levels of hierarchy with five different types of logic. At the bottom level of the hierarchy are regular combinational logic, irregular combinational logic, memory blocks, and combinational and sequential logic. At the top level of the hierarchy is the interconnection logic connecting these different sub-circuits. Generators are proposed for the regular combinational logic, the memory, the combinational and sequential logic, and the interconnection logic. Success is judged in the context of partitioning multiple FPGA systems. Here the utilization of the FPGAs is a key concern, and their method achieves an average filling rate for the clones that deviated by less than 17% from the original circuits. Success is not judged on the basis of the wirelength or delay properties and it is unclear as to whether under these latter criteria the circuits would prove realistic. No characterization or method to judge success is given at the second level of hierarchy.

2.2.5 Generating Circuits with Memory

Wilton et al. [20], generate synthetic circuits with both logic and memory. Their method of generation is, first, to characterize large numbers of real circuits with a view to how logic and memory interconnect and the number, size, and shapes of the memories. Second, synthetic circuits are generated stochastically by randomly selecting a memory configuration and interconnect pattern from the characterization, randomly selecting combinational logic from the MCNC benchmarks [1] and making connections between the memory and logic based on the interconnect pattern. The strength of the method is the inclusion of memory into generation and the realistic connections between memory and logic. The weakness of the method is its use of only combinational MCNC benchmarks in logic portions of the generated circuits.

2.2.6 Generating Circuits Bottom Up

Stroobandt et al. [21], developed a synthetic benchmark generation method that generates circuits using a bottom up clustering approach. This method produces circuits that are too regular and that have unrealistic delay profiles [22]. Verplaetse [22] attempts to fix these

problems and gets good wirelength results that differ by 7% on average, but it is unclear whether or not the delay profile problem has been sufficiently fixed since no comparison is made between the synthetic circuit delay profile and that of a real circuit.

2.3 Summary

In this chapter, we have reviewed the synthetic circuit generation methods that this research is based upon and as well as other approaches. Results were presented that showed that while the quality of combinational synthetic circuit from [7] is reasonably good, the quality of sequential circuits from [8] is too far off to be used as reasonable proxies for real circuits. In the next chapter, we introduce new circuit characterization that captures the natural hierarchy of circuits that will significantly improve the quality of the synthetic circuits produced.

3 NEW CIRCUIT MODEL AND CHARCTERIZATION

In order to introduce hierarchy into synthetic circuits in this chapter, we define a new circuit model to model sequential circuits that allows natural hierarchy to be correctly identified, a clustering method to identify the natural hierarchy, and new set of characterizations that capture the natural hierarchy. We discuss each of these points below. Afterwards, we describe the software tool we have implemented to characterize circuits and discuss the amount of information we have used in our characterizations.

3.1 New Circuit Model for Sequential Circuits

As described in Section 2.1.3, Hutton's sequential circuit model is not natural for all circuits. Here we choose a simpler circuit model that makes it easier for the natural hierarchy to be identified. In the new model, a sequential circuit is viewed as a cloud of logic arrayed by delay level. It is similar to Hutton's combinational circuit model described in Section 2.1.1 but with three additions made to account for flip-flops. The first addition is that flip-flops are placed at delay level 0, the same as the primary inputs. The outputs of these flip-flops drive into the combinational logic just as primary inputs do. Second, the flip-flops themselves must be driven. To do so, some of the regular combinational nodes are designated as *latched nodes*, meaning that the node's output drives the data input of a flip-flop. Finally, this edge that joins a latched

node to its flip-flop ("a DFF edge") is defined to have an edge length of 0. An example of this new circuit model is depicted in Figure 3.1.

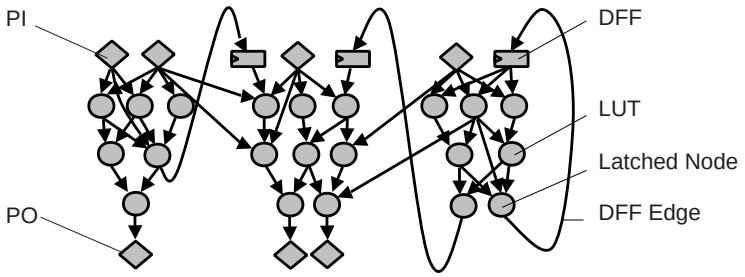


Figure 3.1 - New Circuit Model

These changes to the circuit model remove the pipeline-like assumption of the previous model, but still permit a well-defined characterization of all sequential circuits with a single clock. The new circuit model is also simpler, making it easier to identify the natural hierarchy (described in the next section) and to perform iterative-based generation (described in Section 4).

3.2 Identifying Natural Hierarchy

To identify the natural hierarchy in a circuit (while characterizing a pre-existing circuit) we partition the circuit into clusters. Figure 3.2 shows our sample circuit partitioned into three connected clusters. The clusters in the circuit are formally defined given the graph of the circuit $G = (V,E)$ as resulting from a partition of V into a series of k clusters $C_1, C_2, \ldots C_k$ where the k-clusters are disjoint vertex sets that fully cover V.

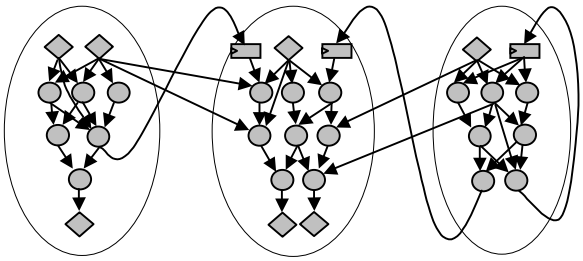


Figure 3.2 - The Sample Circuit Partitioned into Three Clusters.

3.3 Characterization of Clustered Circuits

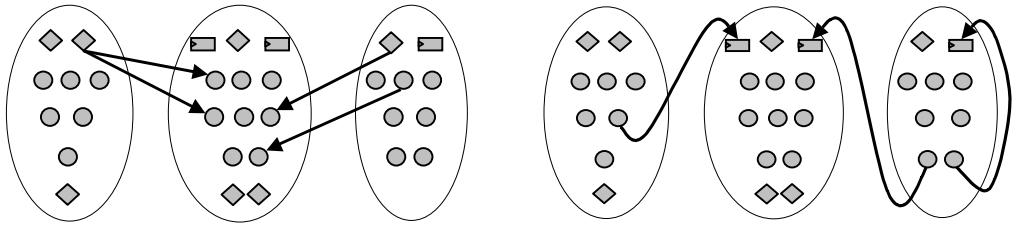
We break the description of the new characterization into four sections. First, we describe the characterizations that we apply unchanged from Hutton's work. Second, we describe the characterization of the connections between clusters. Third, we describe the new characterizations needed to deal with changes made necessary by the fact that the circuits are no longer single cluster systems. Lastly, we describe a characterization of an approximation to wirelength that we will use to control wirelength in the synthetic circuits that are generated.

3.3.1 Unchanged Characterization

We keep unmodified from Hutton's characterizations the number of nodes, the number of primary inputs, the number of flip-flops, the node shape, Primary Output (PO) shape, and fanout distribution. These characterizations are applied to each cluster separately.

3.3.2 Inter-cluster Characterization

The structure of the connections between clusters $C_1..C_k$ is captured through two matrices that count the number of connections to combinational nodes and flip-flops between clusters. The first matrix we define as $Comb=[comb_{ij}]$ where $comb_{ij}$ is the number of inter-cluster connections that drive combinational nodes from clusters C_i *to* C_j. The second matrix we define as $Latched=[latch_{ij}]$ where $latch_{ij}$ is the number of connections that drive flip-flops from C_i *to* C_j. Figure 3.3 illustrate the inter-cluster connections that each of these matrices separately capture for the circuit in Figure 3.1. We have separated the inter-cluster connectivity into these two matrices because they have different connectivity. This different connectivity is evidenced in Figure 3.4, which shows the mean of the correlation coefficient [23] between Comb and Latched across 23 real circuits as a function of the number of clusters in the characterization. Error bars in the graph indicate the standard deviation of the correlation coefficient. As can be seen, the correlation is weak for experiments for which the number of clusters was greater than two.



a) Connections to Combinational b) Connections to DFFs

Figure 3.3. Characterization of Inter-cluster Connections

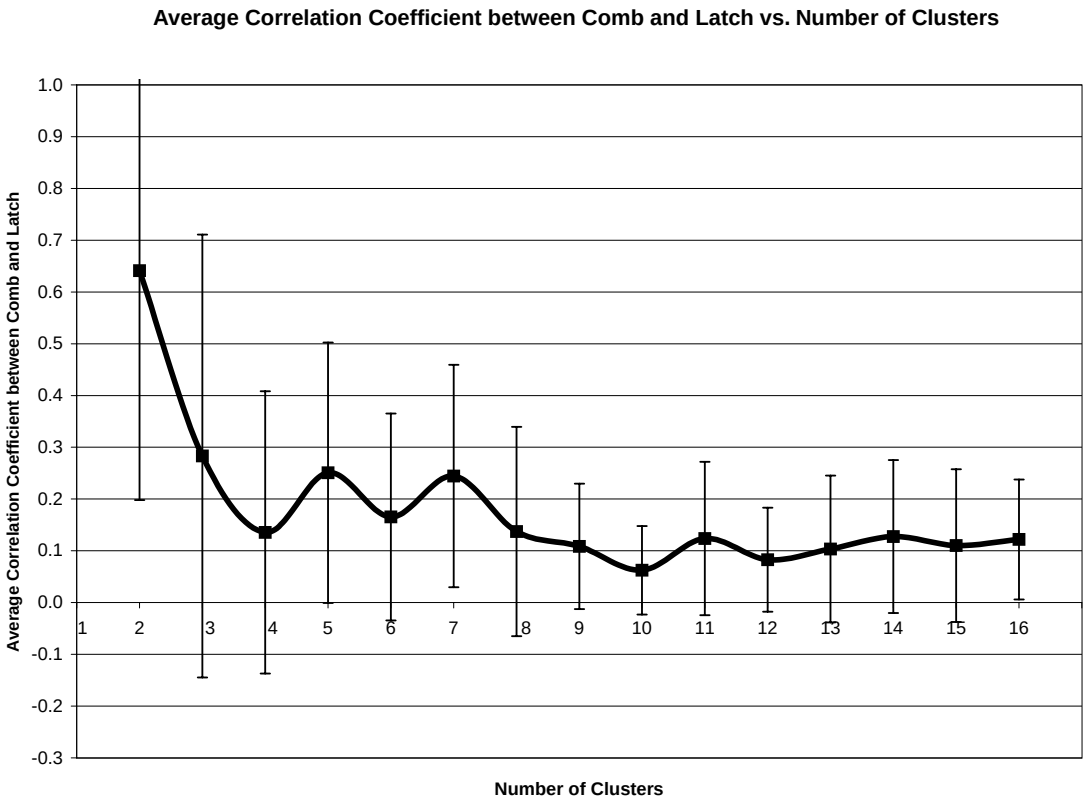


Figure 3.4 - Correlation between Comb and Latched vs. Number of Clusters

3.3.3 New Intra-cluster Characterization

Inside each cluster, we add additional characterizations for the input and output shapes, the latched shape, and the edge length distribution.

The first addition to the circuit characterization was to explicitly include input and output shapes– the number of inputs and outputs entering each combinational delay level. Hutton's generation method derived bounds for these values, but we instead include it explicitly as his process was too complex with the inclusion of multiple clusters.

The second addition is the *latched shape*, which is defined as the number of nodes connected to flip-flops at each delay level.

The last addition is modification of the edge length distribution. The edge length distribution is important because it characterizes the connections between delay levels. In generation, the length of an edge prescribes the possible delay levels that it can connect to without which we would be forced to make connections randomly between delay levels.

Hutton’s work only considered intra-cluster edges. Edges that connected to other combinational sub-circuits were handled with ghost input and output shapes. To deal with the inter-cluster edges four choices presented themselves to us.

The first choice is not to add any additional characterization and to rely on the inter-cluster connection matrices to capture the structure of inter-cluster connections. This would mean that during generation, connections would be made randomly between nodes at random delay levels. This is not acceptable, as the number of inter-cluster edges is from 5-45% of the total number of edges in a circuit as can be seen in Figure 3.5, (which shows the minimum, mean and standard deviation, and maximum percentage of inter-cluster edges across 23 circuits) and therefore play a role considerable to that of intra-cluster edges in the circuit structure.

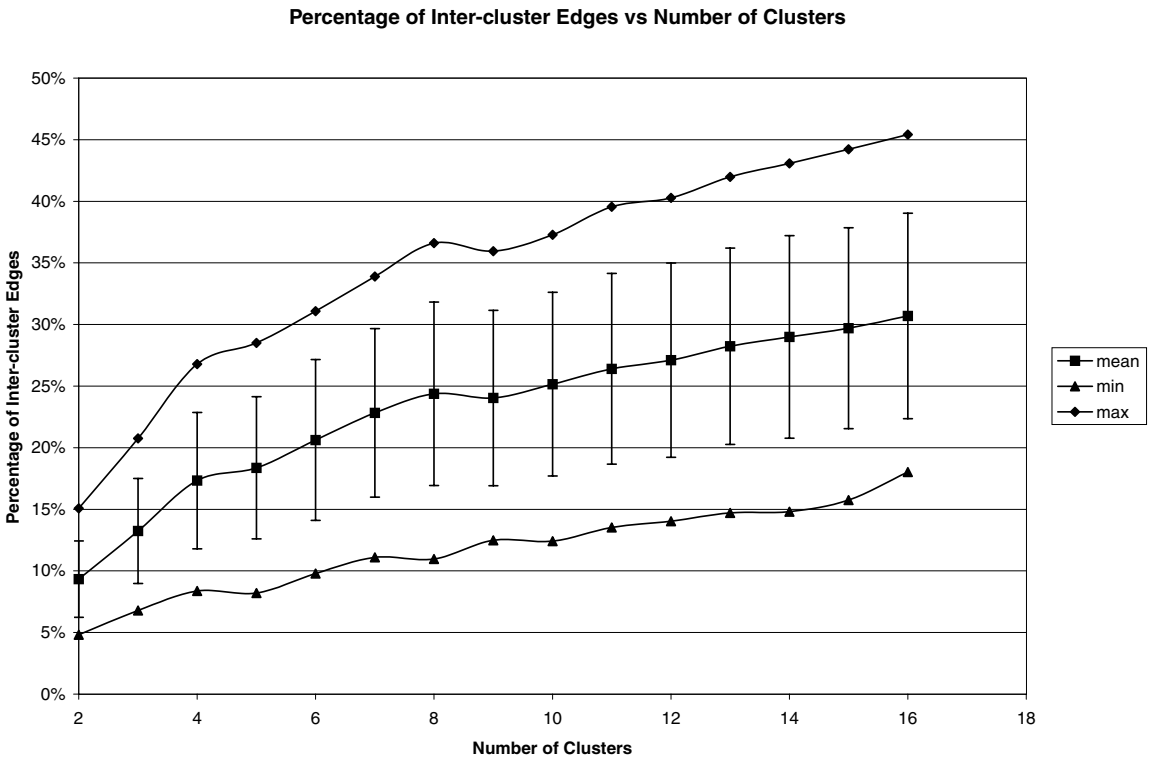


Figure 3.5 - Percentage of Inter-cluster Edges vs. Number of Clusters

Our second choice then is to have an inter-cluster connection matrix for each edge length. But we rule out this approach as the amount of characterization information it requires is k^2*delay which we think would be too much information for someone to understand or for someone to attempt to modify. A more complete discussion of characterization information can be found in Section 3.5.

The only alternative left, therefore, is to try to characterize the connections entering and leaving a cluster. Two approaches to this are: to measure the number of inter-cluster edges entering or leaving each delay level in a cluster with shape functions or to add edge lengths distributions for the inter-cluster edges that enter and leave a cluster. We choose to add additional edge length distributions.

We characterize the edge length distribution in three parts: the *intra-cluster edge length distribution, the inter-cluster input edge length distribution,* and *the inter-cluster output edge length distribution* defined as the number of edges at each edge length that are internal to the cluster, that input into input into the cluster, and that output out of the cluster respectively.

As a quick example of the importance of edge length, from the characterization of real circuits we generated synthetic circuits (using the methods that we will described in Chapter 4) where we used edge length distributions and also where we disregarded them and forced all edges to be length one. We wanted to see if not having the correct edge length distribution had an effect on the fidelity of the synthetic circuits to their original characterization and on the critical path delay. Figure 3.6, shows a comparison of the synthetic circuit's fidelity as a function of the number of clusters used in characterization. The metric of fidelity is the average across all generated circuits of the total deviation from characterization normalized to the number of edges. As can be seen when all the edges are length one, the generator has a much harder time meeting the specification. Figure 3.7, shows a comparison of critical path delay by measuring the average absolute difference in critical path delay between the synthetic circuits and real circuits. The length one edge case had a significantly different critical path delay than the real circuit. Both experiments show that having the right edge length distribution is important to the quality of synthetic circuits produced.

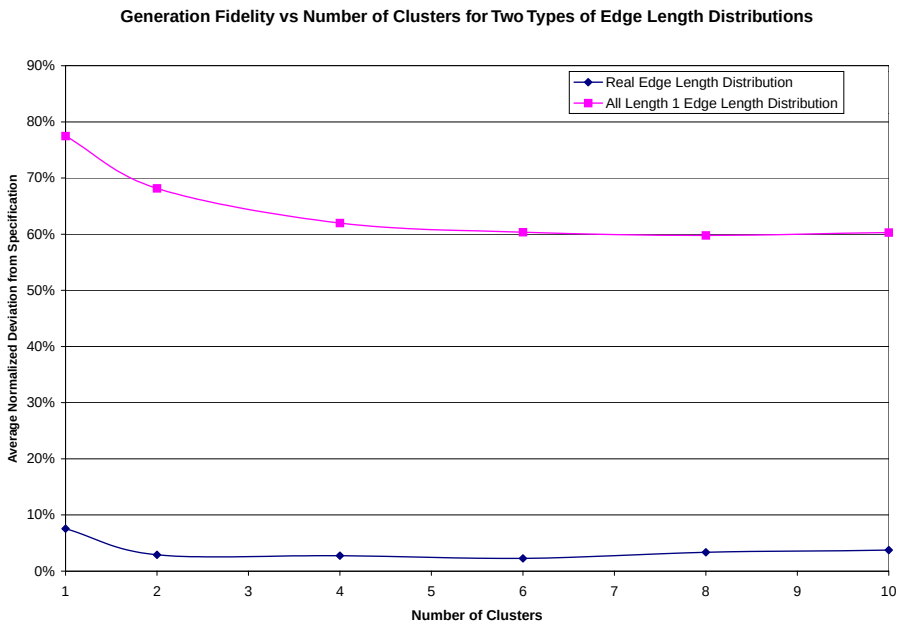


Figure 3.6 - Generation Fidelity for Two Types of Edge Length Distributions

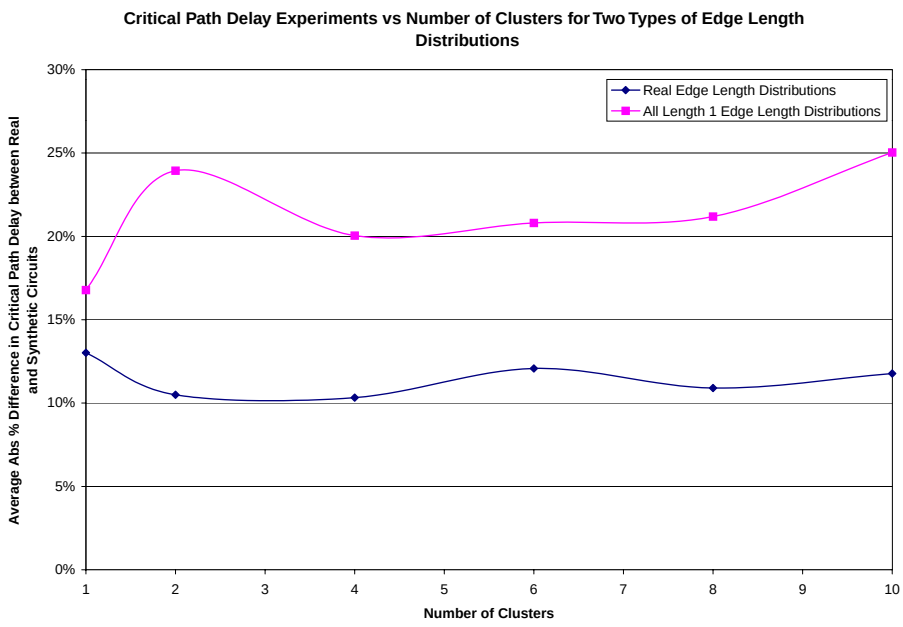


Figure 3.7 - Critical Path Delay Experiments for Two Types of Edge Length Distributions

3.3.4 Wirelength Characterization

To control the post-place and route wirelength of the synthetic circuits that we output from our generation process (described in Section 4) we measure an approximation to wirelength in characterization that we will use in generation. The approximation is a metric that Hutton defined in characterization but never used in generation [24]. First, we will describe the measurement and its motivation. Second, we will describe an algorithm to measure it.

Hutton used an approximation of wirelength instead of real post-place and route wirelength because he wanted to quickly characterize a small amount of information about local structure and thought that a full placement and routing of a circuit on an FPGA or ASIC would be too computationally expensive. Instead, he "placed" the graph within the combinational delay graph structure by assigning each node at each delay level a horizontal position and ordering the horizontal position so as to minimize the number of edges that crossed and the horizontal distance between connected nodes. In our modification of this placement algorithm, we minimize only the total horizontal distance.

With the circuit "placed", Hutton measured his approximation to wirelength that he defined as:

$$wirelength(G) = \sum_{x \in V(G)} \sum_{y \in Source\_nodes(x)} \left| \text{horizontal\_position}(y) - \text{horizontal\_position}(x) \right|$$

He found a strong linear correlation between this metric and the total post-place and route wirelength of the real circuit although there existed large variance in the correlation.

The algorithm we use to "place" the graph is different than Hutton's method. The input into the algorithm is a graph G with clusters $C_1,..,C_k$ where the delay levels of the nodes are well defined. The output from the algorithm is a measurement of wirelength(G). The algorithm proceeds in two steps. In Step 1, we assign horizontal positions to nodes in each cluster of graph G to space them out evenly across each delay level. Pseudo-code for the horizontal position algorithm is shown in Figure 3.8. A picture of the clusters $C_1,..,C_k$ with their horizontal position assigned is depicted in Figure 3.9. Shown in this figure are the clusters stacked on top of each

other to denote that we do not pre-place the clusters in any fashion and that for the purpose of wirelength inter-cluster edges are treated the same way as intra-cluster edges.

In Step 2, we minimize the wirelength(G) measured by optimizing with a simulated annealing algorithm [25] where a move in the algorithm is the exchange of the horizontal position of two randomly selected nodes in a randomly selected delay level. Pseudo-code for the algorithm is shown in Figure 3.10.

```
Width = 16*maximum number of nodes in a
         delay level over all clusters

 for (cluster, C1 to Ck) {
    for(delay level, 0 to dmax) {
       nNodes = number of nodes in the delay level

       /* uniformly space the nodes in the delay level
          out over the width of the circuit */

       spacing_of_nodes = width/nNodes

       for (i,0..nNodes) {
          horizontal_position = i* spacing_of_nodes +
               offset to centre nodes about width/2
        }
     }
 }
```

Figure 3.8 - Horizontal Spacing Algorithm

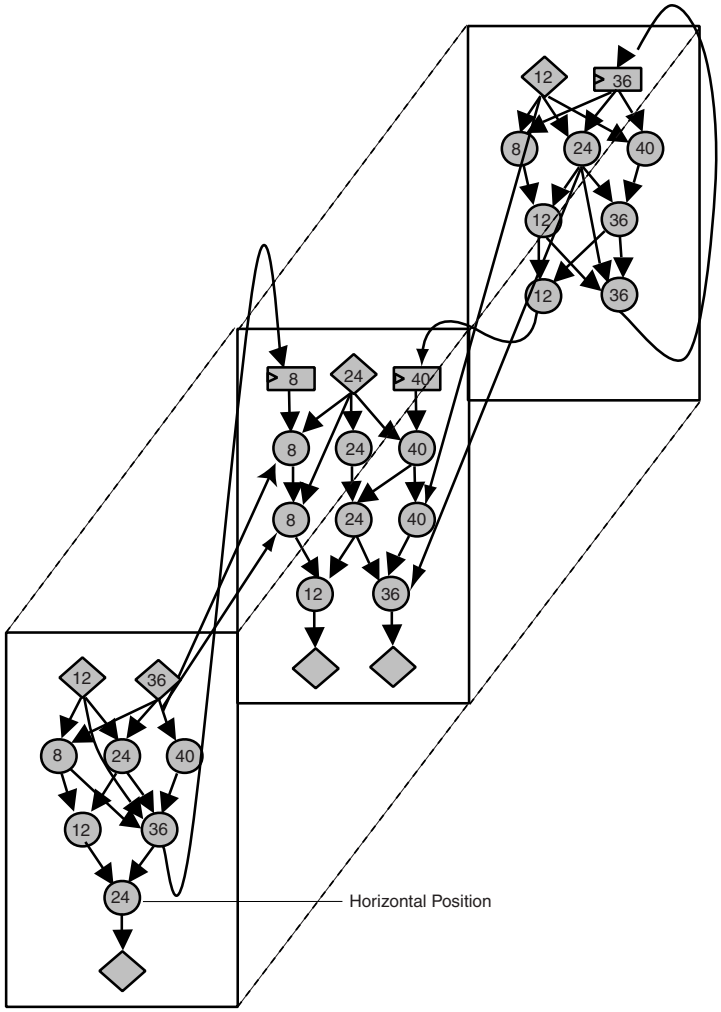


Figure 3.9 - Graph with Nodes Assigned Horizontal Position

```
 cost = wirelength(G)

temperature = 0.01
nNodes = |V(G)|
output_loops = inner_loops = 0

while ( cost > 0 and output_loops < 1000*nNodes ){
    while (inner_loops < nNodes )  {
        move = generate_move()
        Δcost = get_cost_change_of_move(move)
                                                  -Δcost
        if (Δcost < 0 or random_number(0..1) < e^(temperature)) {
              make_the_move
              cost = wirelength(G)
        }
        inner_loops = inner_loops + 1
    }
    temperature = Update_Temperature
    output_loops = output_loops + 1
}
```

Figure 3.10 - Algorithm for Finding Graph Wirelength

3.4 Software Implementation

We rewrote Circ the software tool that Hutton built to characterize circuits. The new Circ, *NCirc*, takes as input a circuit in the BLIF [1] netlist format and outputs statistical information.

A sample of the statistical information output can be seen in Figure 3.11 for the MCNC circuit s526 divided into 2 clusters.

```
######################## BASIC ############################
Name:  s526
Number of Nodes:  76
Number of PI: 3
Number of DFF: 21
Number of Combinational Nodes: 52
Number of Edges: 178
Maximum Delay: 4
Number of PO: 6
kin: 4
Number of Clusters: 2
Wirelength-Approx: 12658
======================= Stats per Cluster ================
Number of Nodes: ( 38 38 )
Number of PI: ( 3 0 )
Number of DFF: ( 10 11 )
Number of Combinational Nodes: ( 25 27)
Number of Intra-Cluster Edges: ( 83 83 )
Number of Inter-Cluster Edges: ( 12 12 )
#################### CLUSTERS #######################
#################### Cluster 0 #######################
Number of Nodes: 38
Number of PI: 3
Number of DFF: 10
Number of Combinational Nodes: 25
Number of Edges: 95
Number of Intra-Cluster Edges: 83
Number of Inter-Cluster Edges: 12
Number of PO: 0
Maximum Fanout: 15
======================= SHAPES ===========================
Node Shape: ( 13 12 9 4 0 )
Input Shape: ( 0 38 35 12 0 )
Output Shape: ( 70 17 6 0 0 )
Latched Shape: ( 0 4 3 4 0 )
PO Shape: ( 0 0 0 0 0 )
======================= EDGE LENGTHS =====================
Intra-cluster Edge Length Distribution: ( 0 59 19 5 0 )
Inter-Cluster Input Edge Length Distribution: ( 0 1 1 0 0 )
Inter-Cluster Output Edge Length Distribution: ( 0 2 2 5 1 )
======================= FANOUT DISTRIBUTION ==============
Fanout Distribution: ( 11 13 3 1 1 3 1 2 1 1 0 0 0 0 0 1 )
#################### Cluster 1 #######################
Number of Nodes:  38
Number of PI: 0
Number of DFF: 11
Number of Combinational Nodes: 27
Number of Edges: 95
Number of Intra-Cluster Edges: 83
Number of Inter-Cluster Edges: 12
Number of PO: 6
Maximum Fanout: 14
```

```
======================== SHAPES ============================
Node Shape: ( 11 13 2 10 2 )
Input Shape: ( 0 44 8 35 6 )
Output Shape: ( 57 14 12 2 0 )
Latched Shape: ( 0 0 0 8 2 )
POshape: ( 6 0 0 0 0 )
======================== EDGE LENGTHS =====================
Intra-Cluster Edge Length Distribution: ( 0 57 15 11 0 )
Inter-Cluster Input Edge Length Distribution: ( 0 2 2 5 1 )
Inter-Cluster Output Edge Length Distribution: ( 0 1 1 0 0 )
======================== FANOUT DISTRIBUTION ==============
Fanout Distribution: ( 10 20 2 0 1 0 0 0 2 0 0 0 0 1 2 )
################### Inter-cluster Connectivity Matrices ######################
Comb

0 10
2 0

Latched

10 1
0 10
```

Figure 3.11 - Statistical Output from NCirc

NCirc uses a partitioner to identify the natural hierarchy in a circuit. The partitioner we choose is the hMetis partitioning package [26] to divide the circuit into clusters because it is a well-regarded partitioner that is freely available. It also possesses an easy-to-use API that can be called from within NCirc. hMetis is a multilevel min-cut partitioner and can partition circuits using a recursive bi-partition or k-way method with different node balancing conditions.

The source code for NCirc can be found at:

http://www.eecg.toronto.edu/~jayar/software/software.html

3.5 Amount of Characterization Information

An important issue in characterization is the quantity of information that is stored. Characterization is used to understand the properties of circuits and, when modified, is the basis for generation of new and different circuits. If the amount of information scales linearly with the

size of the circuit then we will not be able to understand or modify the properties of the circuits in any meaningful way.

The upper-bound on the amount of information used in our characterization of a circuit with k-clusters and delay d_{max} is: k^2 from the inter-cluster connection matrices, $5k(d_{max}+1)$ from the shape functions, $3k(d_{max}+1)$ from the edge length distributions, $k * (max\ fanout+1)$ from the fanout distribution, and $2k$ for the number of primary inputs and flip-flops. This leads to a total upper-bound on the amount of information of:

$$characterization\ information\ upper\ bound = k^2 + 8k(d_{max} + 1) + k(max\_fanout + 1) + 2k$$

If we take a look at the numbers involved in the above equation we see that: k is a function of the number of high level design blocks and is typically not too large (in our work we have experimented with k being up to 32 clusters); d_{max} does not scale linearly with the size of circuit as designers are always looking at ways to reduce it; and while max fanout can be quite high, the fanout distribution vector is quite sparse for all fanouts above 20 and hence in practice does not contain too much information.

4 GENERATION

We now describe a method of generating synthetic circuits. Its three key features are that i) it employs the new sequential model described in Section 3.1, ii) it generates circuits as groups of connected clusters as described in Section 3.2, and iii) its overall approach is to use iteration in the generation process, as opposed to the constructive approach taken by Hutton [7,8].

The input to the generation process is the characterizations we defined in the previous section which are: *Comb*, *Latched*, the number of clusters, and for each cluster the number of nodes, the number of primary inputs, the number of flip-flops, the node shape, the primary output shape, the latched shape, the input shape, the output shape, the fanout distribution, the intra-cluster edge length distribution, inter-cluster input and output edge length distributions. The output from the generation process is a circuit in BLIF [1] format ready to be placed and routed. We set the function of each LUT to be a NAND gate to give each LUT a logic type.

The generation algorithm proceeds in four steps. In Step 1, we create the delay structure of the circuit by assigning edges between the level nodes in the circuit (recall that a level node contains all of the individual nodes at each delay level). In Step 2, the fanout distribution in each cluster is partitioned among the level nodes. In Step 3, the level nodes are split into individual nodes and the individual nodes are prepared for final edge assignment. In Step 4, edges are assigned between individual nodes in the circuit based on the delay structure of the circuit and the fanouts assigned to the individual nodes.

4.1 Creation of Delay Structure

The input to this step is the *delay structure characterization* which consists of the *Comb* and *Latched* matrices, d_{max}, and for each cluster the node shape, the input shape, the output shape, the latched shape, the intra-cluster edge length distribution, the inter-cluster input edge length distribution, and the inter-cluster output edge length distribution. The delay structure of a circuit can be thought of as the large-scale connectivity between delay levels in the clusters of the circuit. Individual nodes in the delay levels of a cluster are aggregated into level nodes. Edges between the level nodes are aggregated into *super edges* where a super edge is an edge between two levels nodes with a weight equal to the number of edges intended to be formed between the two level nodes.

With the aggregations, we define the delay structure of a circuit as the graph *delay structure = (Level Nodes, Super Edges)*, where *Level Nodes* represents the set of all level nodes and *Super Edges* represents the set of all possible super edges in a circuit.

The desired output is the delay structure with the weights of the super edges assigned to ensure that each node will be able to have its delay level correctly set, the delay structure will not force node violations to be made during final edge assignment, and deviations from the given characterization are minimized.

The algorithm for solving this problem is divided into two parts. The first part creates the combinational connections in the circuit while the second part creates the sequential connections in the circuit making connections from level nodes with latched nodes to level nodes with flip-flops. We describe each of these parts separately.

4.1.1 Creating the Combinational Delay Structure

The initial solution for the combinational connection part of the algorithm is created by inserting all intra- and inter- cluster edges into the graph. Input into the algorithm is the delay structure characterization without the latched shapes or *Latched* matrix. Output from the algorithm is the Combinational Delay Graph Structure, an example of which is shown in

Figure 4.1. The figure shows the level nodes in each cluster (and the number of individual nodes contained in a level node), the weight assigned to the super edges and the specification of the number of inputs and outputs each level node requires.

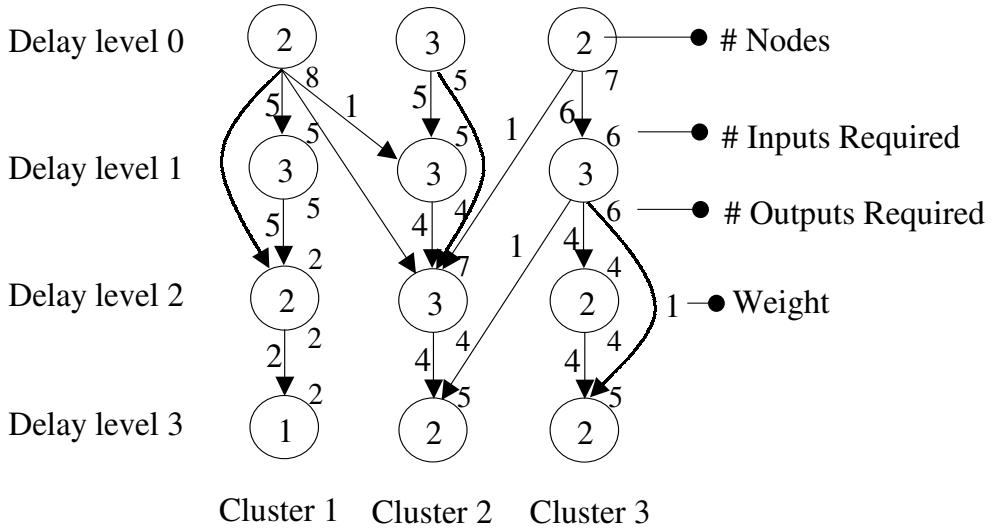


Figure 4.1 - Combinational Delay Graph Structure

The algorithm to create the initial solution proceeds in four steps. In Step 1, we create the level nodes and super edges between the level nodes. In Step 2, we assign the maximum possible weight to each super edge based on the input specifications. If the super edge is intra-cluster, we limit the maximum weight by the cluster's intra-cluster edge length distribution, input shape, output shape, and by the possible number of unique connections between nodes in the source level node and nodes in the sink level node. If the super edge is inter-cluster, we limit the maximum weight by the source cluster's inter-cluster output edge length distribution and output shape, the sink cluster's inter-cluster input edge length distribution and input shape, and by the possible number of unique connections between nodes in the source level node and nodes in the sink level node. The maximum weight assigned to a super edge is used as a starting point in the creation of the initial solution and as an upper bound on super edge weight when we later try to improve the initial solution (described in the paragraphs below). In Step 3, we randomly reduce

weight on the inter-cluster edges to meet *Comb*, and in each cluster the inter-cluster input edge length distribution and inter-cluster output edge length distribution while making sure that each level node has enough unit edges to define the delay level of its nodes. The delay level of a node is defined if it has a unit edge from a node in the delay level above. In Step 4, we randomly reduce weight on the intra-cluster edges to meet the intra-cluster edge length distribution in each cluster while making sure that each level node has enough unit edges to define the delay level of its nodes.

After creating the initial solution, we employ an iterative algorithm that selects certain edges as candidates for relocation and accepts or rejects proposed changes based on a cost function.

In the following paragraphs, we will describe the cost function, how edges are selected and modified ("moves"), the overall structure of the algorithm, and the performance of the algorithm.

The cost function of the iterative algorithm is as follows:

$$cost_{Delay\ structure} = \mathrm{cost}_{Comb} + cost_{Edge\ Length} + cost_{Level\ Shape} + cost_{Problem\ Node}$$

Here, $cost_{Comb}$ measures the absolute difference between the current *Comb* and its specification, $cost_{EdgeLength}$ measures the absolute difference between the current edge length distributions and their specifications, $cost_{LevelShape}$ measures the absolute difference between the current input and output shapes and their specifications with congestion factors multiplying this cost at each level node to penalize level nodes that have too many inputs or outputs. Finally, $cost_{Problem\ Node}$ measures the number of node violations that would be forced to be made during final edge assignment because of the number of edges input or output of a level node.

The algorithm selects super edges to change in the graph as follows: First, we randomly select a super edge to move with edges that contribute more to the $cost_{Level\ Shape}$ having a higher probability of being selected. We weight the probability of an edge being selected according to Figure 4.2, in which we give higher selection weights to super edges between source level nodes that have too many outputs and too many inputs and give lower selection weights to

super edges that have source level nodes with not enough outputs or sink level nodes with not enough inputs. We also add a small bias to the selection weight of each super edge to ensure that each edge has a small probability of being chosen.

```
nOutputs = source level node's number number of output edges
nInputs = sink level node's number of input edges
Output difference = source level node's (nOutputs - spec nOutputs)
Input difference = sink level node's (nInputs - spec nInputs)
                        Output_difference*weight(edge)/nOutputs+
selection_weight(edge)= Input_difference*weight(edge)/nInputs+
                         Small Bias
```

Figure 4.2 – Edge Selection Weight

Second, after selecting an edge to move, we randomly choose a new destination for the edge from the possible super-edges that can accept the edge with its given length. A super edge can accept the individual edge to move if it has the same length and if the super edge is not already at its maximum possible weight (the weight we calculated above during the creation of the initial solution).

Figure 4.3 illustrates a move of an inter-cluster edge and its effect on the weight of the corresponding super edges.

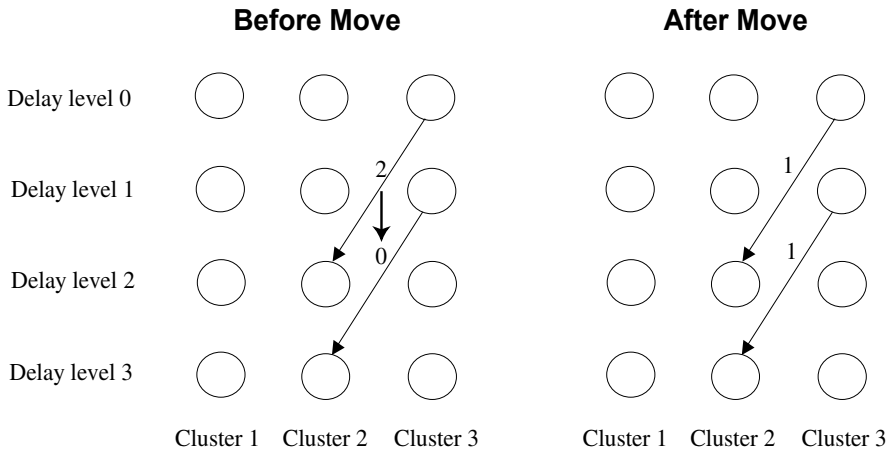


Figure 4.3 – Example of Edge Movement

To improve the solution, we employ a simulated annealing-like algorithm [25], the pseudo-code for which can be seen in Figure 4.4. In the algorithm, all valid moves that improve the cost function are accepted, and valid bad moves are accepted with a probability that decreases exponentially with an increasing change of cost. A move is valid if, after the move, the sink level nodes involved will still have enough unit edges to correctly define the delay level of their individual nodes. The algorithm terminates when the cost is zero or after the number of moves attempted is fifty times the number of edges in the graph. During iteration, to help resolve contentions for level nodes among the edges every |E(G)|/2 moves we increase the congestion costs of level nodes that have too many inputs or outputs and decrease the congestion costs of level nodes that no longer have too many inputs or outputs. Also during iteration, after attempting moves equal to forty times the number of edges, we decrease the temperature to perform more of a greedy optimization.

```
nNodes = |E(G)|
loops = 0
temperature = 6
while ( cost_delay structure > 0 and loops < 100*nEdges ){
     move = generate move()
     if (move is valid) {
           Δcost = get cost change of move(move)
           if (Δcost < 0 or random number(0..1) < e^(-Δcost/temperature) ) {
               make the move
           }
     }
    loops = loops + 1
    if (loops is a multiple of 40*nEdges) {
           temperature = temperature/2
     } else if (loops is a multiple of nEdges/2) {
           increase congestion costs at congested level nodes
           decrease the congestion costs at decongested level nodes
    }
}
```

Figure 4.4 – Combinational Delay Structure Iteration Algorithm

Once the iteration terminates, it is possible that node violations (which are nodes that have one or more of the following properties: no outputs, no inputs, too many inputs, or nodes with two or more connections from the same source node) remain. In this case, we post-process the graph by removing or adding any edges to remove the violations.

To evaluate the performance of our algorithm we ran it over the characterizations of 23 circuits (described in Section 5.2) partitioned into 1-16 clusters and measured $cost_{Delay\ Structure}$ before iteration and at the end of iteration. We then normalized each measurement by the number of edges in each graph, averaged the normalized measurements over the 23 circuits, and plotted the results as a function of number of clusters as shown in Figure 4.5. We normalized to the number of edges because deviations from specification are the result of misplaced edges. We can see in the figure that cost is fairly constant and, at less than 5% for all clusters greater than one, fairly low.

To examine the makeup of $cost_{Delay\ Structure}$ we then divided $cost_{Delay\ Structure}$ into its constituent costs as can be seen in Figure 4.6. It shows the average percentage that each of the constituent costs makes up of the total cost. From the graph, we see that $cost_{Edge\ Length}$ and $cost_{Level\ Shape}$ make up the majority of the total cost.

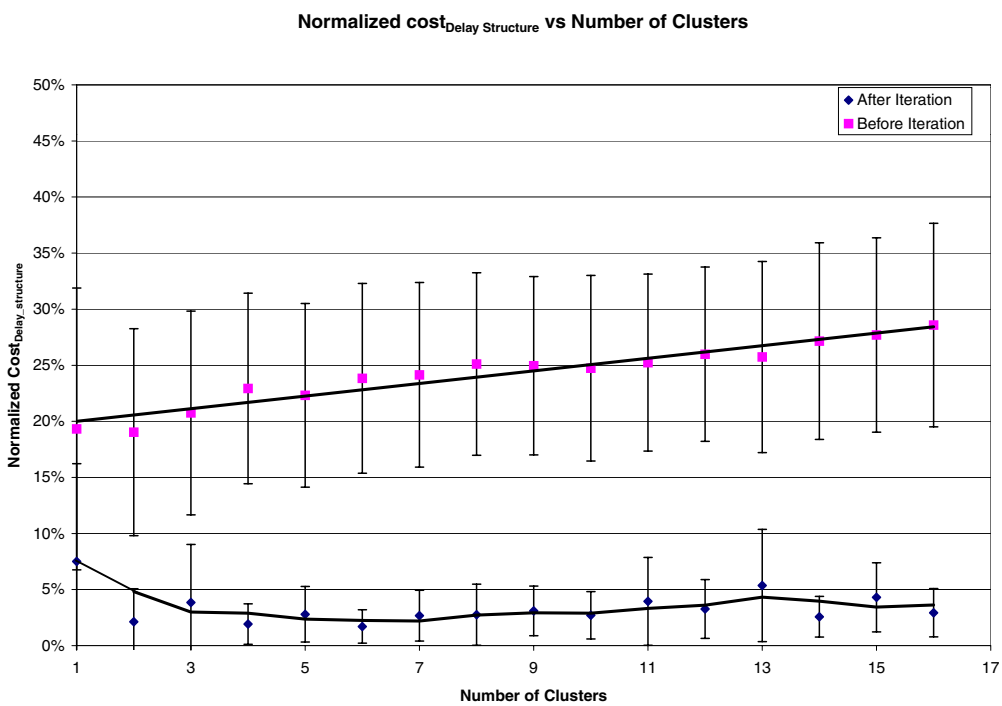


Figure 4.5 - Normalized $Cost_{Delay\ Structure}$ vs. Number of Clusters

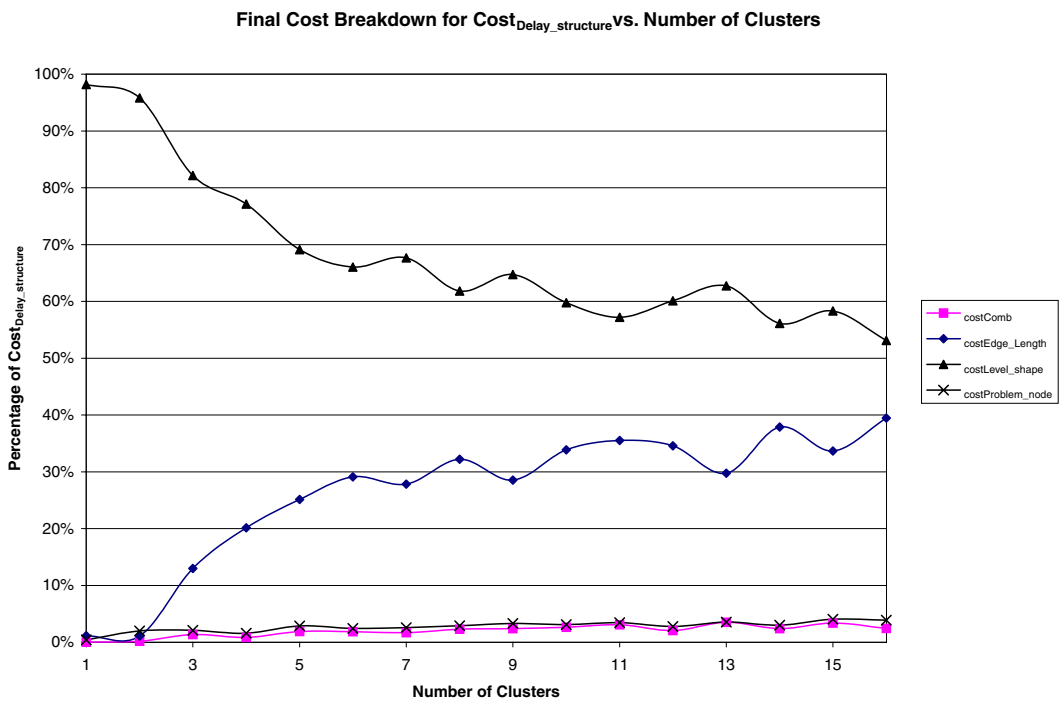


Figure 4.6 – Cost break down for $Cost_{Delay\ Stucture}$ vs. Number of Clusters

4.1.2 Creating the Sequential Delay Structure

With the global combinational delay structure complete, the delay structure is finished by forming the connections between the level nodes with latched nodes and the level nodes with flip-flops. The input into this phase of the algorithm is the matrix *Latched* and the latched shapes in each cluster. The output is the finished delay structure graph. Each connection in the graph is formed in three steps. First, we randomly select a source and sink cluster from the *Latched* matrix. Next, we randomly select the source level node from the set of all level nodes with latched nodes as dictated by the latched shape in the source cluster. Finally, a connection is made between the source level node and the 0th delay level in the sink cluster. A picture of the completed delay graph structure can be seen in Figure 4.7, which shows the addition of the latched node to flip-flop connections.

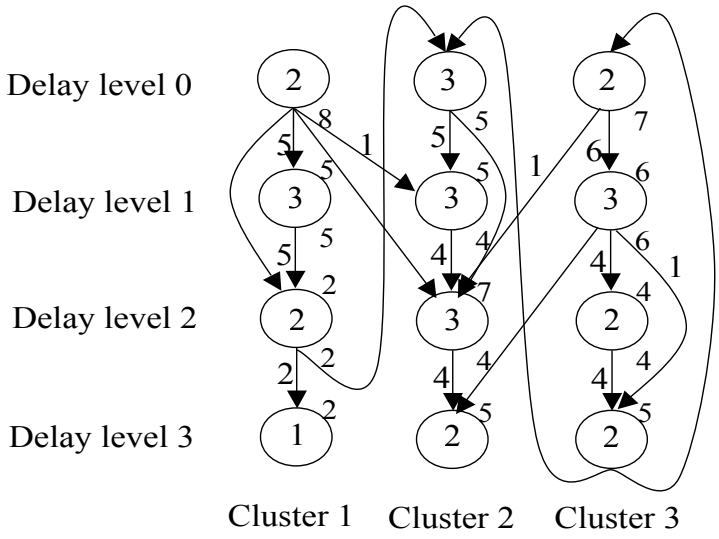


Figure 4.7 - Completed Delay Structure

4.2 Degree Partitioning

After creating the delay structure, the fanout distribution of each cluster (which is a set of fanout values that ultimately will be assigned to each individual node) is partitioned among the level nodes in the cluster. The input into this degree partitioning step is the delay structure (generated above in Step 1) and the fanout distribution. The output is the delay structure graph with the fanout distribution partitioned among the level nodes such that the sum of the fanout degrees assigned to each level node matching the number of edges that leave the level node. An example of delay structure with the fanout assigned can be seen in Figure 4.8.

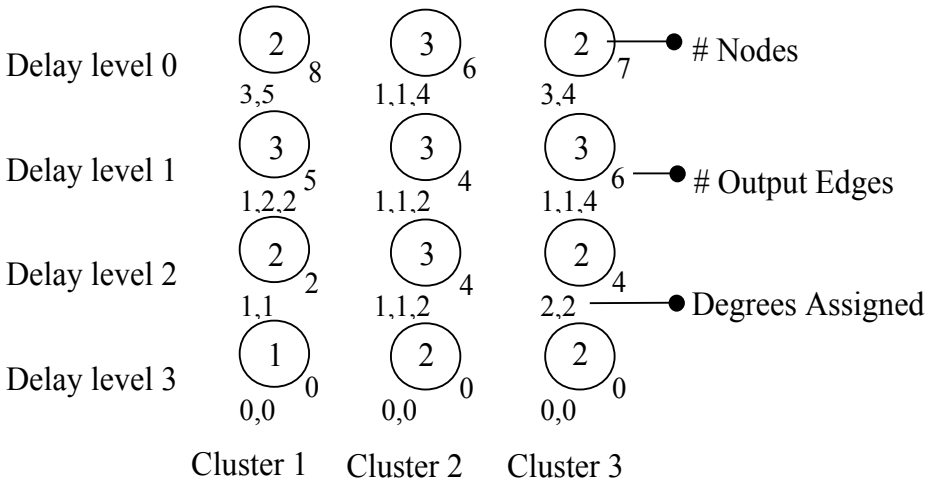


Figure 4.8 - Fanout Assigned Delay Graph Structure

The degree partitioning occurs in three steps. In the first step, an initial assignment is made. In the second step, the degree partition is iteratively improved. In the third step, post processing is done to enforce the equality described above.

The initial fanout assignment in each cluster is made based on the fanout distribution and the node shape and output shape of the delay structure. It occurs in five steps with Steps 1, 4, and 5 being based on Hutton's [7] work. In Step 1, the level node at delay level d_{max} is assigned a fanout of 0 for each node because nodes with maximum combinational delay are either latched or are a primary output. In Step 2, level nodes with latches are assigned the lowest unassigned fanout degrees. In Step 3, if any zero degree fanouts remain, they are assigned to level nodes with POs. In Step 4, pre-assignment of low fanout degrees are made to level nodes with a small ratio of output degree to number of nodes. In Step 5, the remainder of the fanouts are assigned beginning with the largest fanouts based on the fanout capacity of the level nodes.

After the initial assignment, the degree assignment is improved by swapping fanout degrees between level nodes in an attempt to improve the solution quality defined as:

$$cost_{Degree} = \sum_{LN \in Level\ Nodes} \text{cost}_{Fanout\ Edge\ Misassignment}(LN) + \text{cost}_{Fanout\ Penalty}(LN)$$

Here $cost_{FanoutEdgeMissassignment}$ measures for each level node the absolute difference between the sum of the fanout degrees assigned and the number of output edges that were assigned in Section 4.1 and $cost_{FanoutPenality}$ is a cost that penalizes level nodes with fanouts that will force node violations in the final edge assignment (described below in Section 4.4).

The degrees to be swapped are chosen by first, randomly choosing a non-zero fanout degree from the level nodes with higher total fanout than number of output edges assigned. Next, we randomly choose a non-zero lower fanout degree from the level nodes with lower total fanout than the number of output edges assigned. Zero fanout degrees are never chosen because they can only be assigned to either a latched node or a node with a primary output and hence their movement is more complicated. An example of a degree move is given in Figure 4.9.

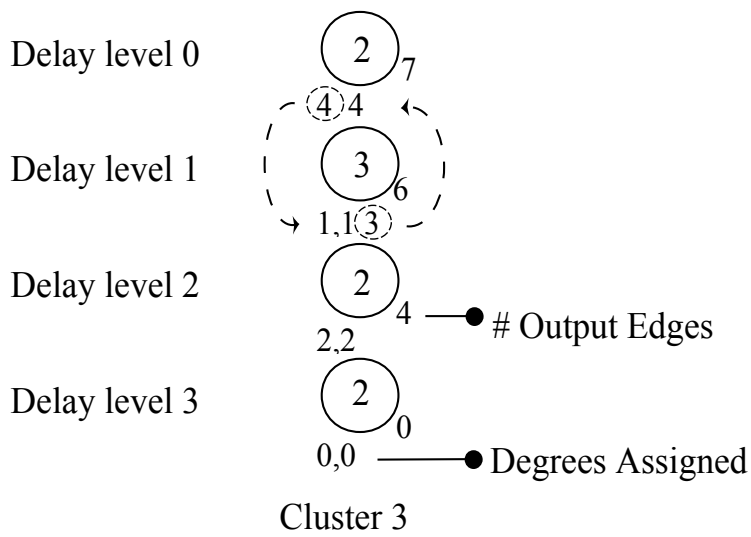


Figure 4.9 - Example of a Degree Move

We employ a hill climbing iterator, in which all changes that improve the cost function are accepted, and bad moves are accepted with a probability that decreases exponentially with the change in cost. Moves are continually generated in the algorithm until there is no change in the lowest cost for 5000 iterations or until the total cost is zero. Pseudo code for the iterative improvement algorithm can be seen in Figure 4.10.

```
loops = 0
while ( cost_Degree > 0 and loops < 5000 ){
     move = generate move()
     Δcost = get cost change of move(move)
     if (Δcost < 0 or random number(0..1) < e^(-Δcost) ) {
          make the move
     }
}
```

Figure 4.10 - Degree Partitioning Iteration Algorithm

After improving the solution quality, some small discrepancies may still exist between the sum of the fanout degrees assigned to each level node and the number of edges that exit the level node. Furthermore, there may still exist level nodes that have fanouts that will force multiple connections between two nodes during final edge assignment. The discrepancies exist in these cases because the output shape of the delay graph structure often does not exactly match the specification of the output shape. These discrepancies are resolved by randomly selecting and decreasing fanout values biasing the degree selection towards larger fanouts or if that cannot be done by adding extra edges. The number of these discrepancies tends to be small involving less than 1% of the total edges.

4.3 Splitting Level Nodes into Individual Nodes

The next step in the generation process is to split the level nodes into individual nodes (which will ultimately become 4-input LUTs, primary inputs, and flip-flops in the final generated circuit). The graph is also prepared for final edge assignment. The input into this phase of the algorithm is the fanout-assigned delay graph structure (described in Section 4.2) with the

latched shape, the primary output shape, and the number of primary inputs and flip-flops. The output from this is a graph where the individual nodes have been created at each level node and assigned a logic type from one of flip-flop, primary input, or LUT; where each node has an assigned fanout; where each node has a horizontal position and where all latched nodes and nodes that are primary outputs have been designated. This structure is called the *pre-edge assignment structure* and is shown in Figure 4.11.

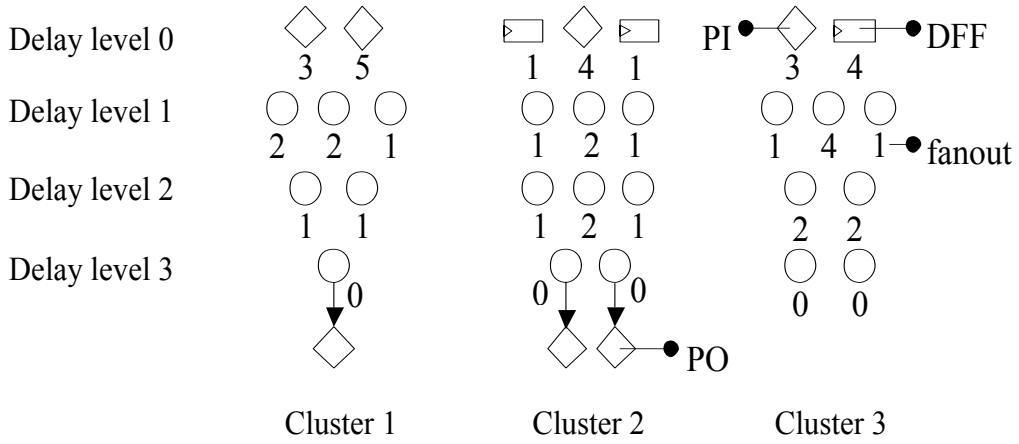


Figure 4.11 - Pre-edge Assignment Structure

In the first step, we assign each individual node a fanout from the fanouts assigned to its level node.

Next, we select nodes to designate as latched by randomly selecting nodes of zero fanout or, if there are more latched nodes than zero fanout nodes, we randomly select nodes of the lowest fanout.

Third, we assign a logic type to all nodes. We start by designating all nodes at delay levels greater than one as 4-LUTs. Next, in two steps we designate the nodes at the 0th delay level as either a primary input or a flip-flop. In Step 1, we assign all nodes with zero fanouts at the 0th delay level that are not latched to be flip-flops because only primary inputs that are latched or flip-flops with primary outputs can have zero degree fanout assignments. In Step 2, we

randomly designate the rest of the nodes as primary input or flip-flop until we designate all primary inputs and flip-flops.

Next, we assign primary outputs by first attaching primary outputs to all non-latched nodes with zero fanout. Then, if there are any remaining POs that need to be assigned, the POs are assigned by randomly attaching PO to non-latched non-PI nodes.

In the last step, before final edge assignment, we assign each node a horizontal position to give meaning to the wirelength approximation discussed in Section 3.3.4. We assign horizontal positions according to Hutton's method [7], in which high fanout nodes are assigned positions that balance them across each level node so as to not skew $wirelength_{Approx}$. The only change we make to the algorithm is that we assign a slightly different set of horizontal positions. The input into the algorithm is the level nodes where the individual nodes within have been assigned a fanout value. The output from the algorithm, depicted in Figure 4.12, is the level nodes where the individual nodes within have been assigned a horizontal position. We assign horizontal positions to the nodes in each level node in three steps. The pseudo-code for the algorithm is given in Figure 4.13.

In Step 1, we create a list of horizontal positions. In Step 2, we create a *binary tree probability mass function* (pmf) that assigns a probability to each horizontal position. To calculate this distribution we first take a balanced binary tree, of size equal to the number of individual nodes, and label its interior nodes with the number of leaves in the interior node's subtree and label its leaves with the number one. Next, we traverse this tree in-order and record the labels into a vector. An example of a vector of length 15 is [1,2,1,4,1,2,1,8,1,2,1,4,1,2,1]. Last in this step, we create the pmf from this vector by normalizing each entry in the vector by the total sum over all entries. At this point, each entry in the pmf corresponds to an entry in the list of horizontal positions. In Step 3, we assign a horizontal position to each node by sampling the pmf for an index into the list of horizontal positions in order of nodes of highest fanout to nodes of lowest fanout. After each sample the entry in the pmf is zeroed and the vector renormalized in order to

keep the sum of the probabilities in the pmf equal to one. As Hutton noted, this method will most likely assign the highest fanout to the centre, with the next two fanouts to the quartiles.

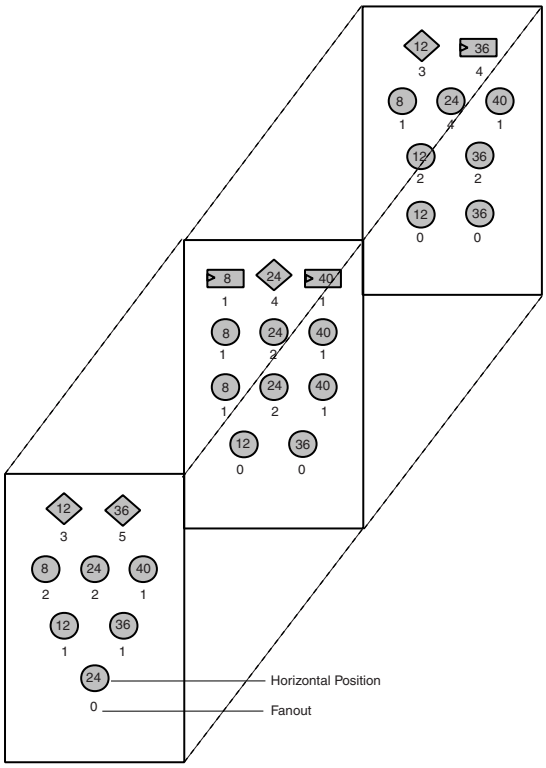


Figure 4.12 - Graph where Nodes have been Assigned a Horizontal Position

```
Width = 16*maximum number of nodes in a
         delay level over all clusters

 for (cluster, C1 to Ck) {
    for(delay level, 0 to dmax) {
      nNodes = number of nodes in the delay level
      spacing of nodes = width/nNodes

      /* Step 1: Build a list of horizontal positions */

       for (i,0..nNodes) {
          horizontal position[i] = i* spacing of nodes +
               offset to centre nodes about width/2
        }

      /* Step 2: Build a probablity density function that will
         be used to assign nodes to those positions */

      pdf = create binary tree distribution of length nNodes()

      /* Step 3: Assign Horizontal Positions to the nodes starting
         with nodes of highest fanout */

      list of nodes = sort highest fanout to lowest fanout(nodes)
      for (i,0..nNodes) {
            node = list of nodes[i]
            index = sample without replacement(pdf)
            node's position = horizontal position[index]
     }
 }
```

Figure 4.13 - Horizontal Spacing Algorithm before Final Edge Assignment

4.4 Final Edge Assignment

The last stage in the algorithm is final edge assignment. The input into the algorithm is the pre-edge assignment structure described above in Section 4.3. The output from this step is the completed synthetic benchmark circuit. The algorithm proceeds by creating an initial solution and then iterating to improve the solution.

The initial solution is created in two parts. First, we create the connections to the combinational (individual) nodes and secondly we create the connections between the latched nodes and flip-flops.

We make the connections to combinational nodes in the graph by visiting each level node in turn and forming connections to the individual nodes it contains in four steps. Our method to construct the initial solution is based on and evolves from Hutton's work [7]. It is illustrated in Figure 4.14.

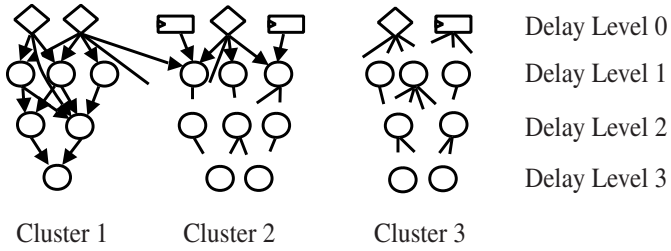
In Step 1, we create a list of source and destination nodes for the connections we want to form. The destination node list we create from the level node's individual nodes. The source node list we create by sampling individual nodes with unassigned fanout from the *source level nodes*, which are all the level nodes with a super edge input into the level node. The number of nodes sampled from each source level node is the weight of its corresponding super edge. When making connections, we remove nodes in the destination list once they can no longer accept an input and nodes in the source list once the numbers of connections that have been made from it equal the number of times it was sampled.

In Step 2, we ensure that each destination node has its delay level well defined by assigning an edge between it and a source node that is a unit edge length apart. The source node is chosen by randomly sampling the source node list for nodes that are a unit distant apart and choosing the source node that is closest in horizontal position to the destination node. This process of sampling the source nodes for a node that we can make a connection to is called the *edge connection process.*

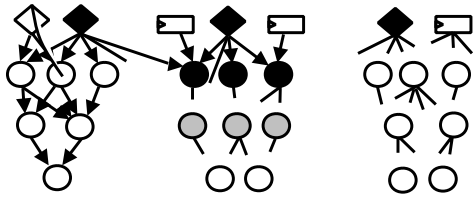
In Step 3, we ensure that the destination nodes are not single-input buffers by assigning them a second edge with the edge connection process. The only restriction on this node selection process is that the destination node cannot make a second connection to the same source node.

In Step 4, we form the remainder of the connections. We randomly select destination nodes and make connections using the edge connection process until either we can no longer make further connections without creating node violations or we run out of source nodes. If any source nodes remain, we randomly select destination nodes and make connections in spite of node violations in the hope that they will be resolved later during iterative improvement.

Connection Assignment at Cluster 2 Delay Level 2

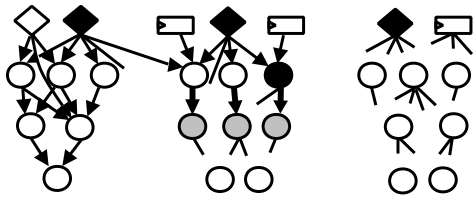


Step1 Making Source and Destination List



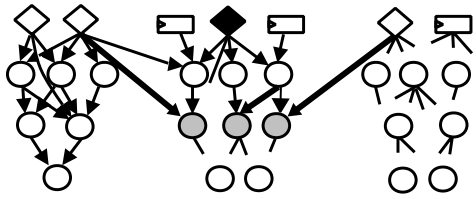
Sources: Black
Destinations: Grey

Step2 Ensuring Delay



Each Node has a connection from a unit edge

Step 3 Ensuring no Buffers



Each node has two inputs

Step 4 Assigning Rest of Connections to Delay Level

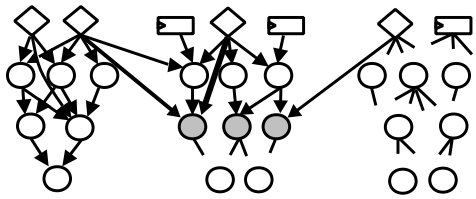


Figure 4.14 - Edge Assignment Algorithm at Cluster 2 Delay Level 2

After making the connections to the combinational nodes, a similar method is used to make the latched connections. For each level node with flip-flops, a source node list is created by sampling unconnected latched nodes from its source level nodes. This source node list is then used to make connections between latched nodes and flip-flops. The connections are made by connecting each flip-flop to a latched node chosen by randomly sampling the source list a number of times and selecting the latched node that is closest in horizontal position.

After creating the initial solution, we employ an iterative algorithm that selects certain edges as candidates for relocation and accepts or rejects proposed changes ("moves") based on a cost function.

The cost function of the algorithm is as follows:

$$cost_{Edge\ Assign} = \beta(\text{wirelength}_{\text{Approx}}(\text{G}) - desired\_wirelength) + (1-\beta)\sum_{n \in V(G)} \text{Number of Violations}(n)$$

Here, *desired wirelength* is a parameter in generation that is discussed more fully in Section 4.5, and *Number of Violations* is a function that returns the number of nodes that have no inputs, too many inputs, two or more connections from the same source node, or if the node is a flip-flop a connection to itself. The wirelength costs are normalized to the maximum horizontal position multiplied by the number of edges while the *Number of Violations* cost is normalized to the number of edges. We use the factor β to balance the goal of achieving the desired wirelength against the goal of having no node violations. The value is set to 0.02 because the wirelength cost is often much larger than the no node violation cost and while achieving the desired wirelength is important it is more important that we have no node violations because they create sizeable difficulties.

We generate moves 95% of the time purely randomly while 5% of the time we target nodes with violations.

When we generate a purely random move, we start by randomly selecting an edge in the graph. With this edge we attempt one of two possible move types with equal probability. Each move

preserves the combinational delay structure and the number of edges that output from each node.

In the first move type, defined as an *edge rotation*, we move the end point of the edge to a new sink node. The new sink node is randomly chosen from within the same level node as the old sink node.

In the second move type, defined as a *double edge swap,* we select a second edge and move the end point of each edge to the other edge's sink node. The second edge is randomly chosen from the edges that output from the same level node that the first edge outputs from. Both move types can be seen in Figure 4.15.

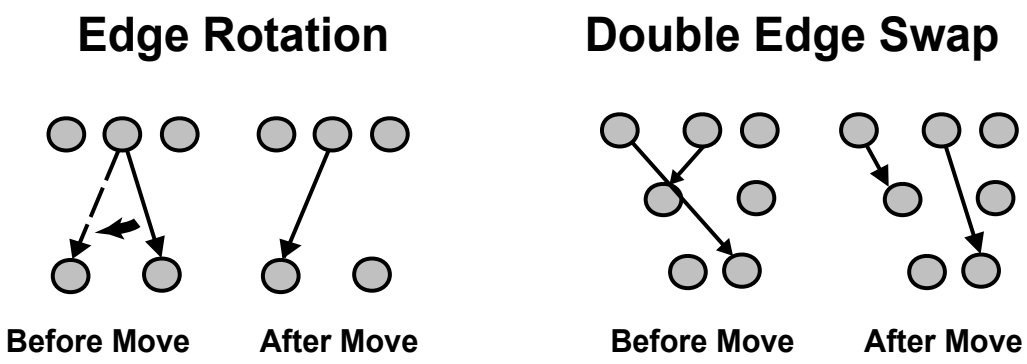


Figure 4.15 - Edge Movements in Final Edge Assignment

For the 5% of moves that explicitly attempt to eliminate node violations, we randomly select a node that is in violation. If the violation type is either too many inputs or two or more connections from same source node, we select one of the problem edges and attempt an edge rotation. If the node violation is a flip-flop that connects to itself we attempt a double edge swap where we choose the first edge that connects the flip-flop to itself and the second edge from the list of all edges in the graph that connect to flip-flops and whose choice will preserve the Latched specification.

We employ a hill climbing iterator, in which all valid changes that improve the cost function are accepted, and valid bad moves are accepted with a probability that decreases exponentially with

the change in cost. A move is valid if it will not create any flip-flops with loops back to themselves. The algorithm continues until the cost is zero or until the number of moves attempted is a hundred times the number of edges in the graph. Pseudo-code for the algorithm can be seen in Figure 4.16.

```
nEdges = |E(G)|
loops = 0
temperature = 0000001
while ( cost_Degree > 0 and loops < 100*nEdges ){
     move = generate move()
     Δcost = get cost change of move(move)
     if (move is valid) {
           if (Δcost < 0 or random number(0..1) < e^(-Δcost / temperature) ) {
                 make the move
           }
     }
}
```

Figure 4.16 – Final Edge Assignment Iteration Algorithm

After iteratively improving the graph, if we still have node violations we post process the graph by removing or adding any edges to remove the violations.

4.5 Wirelength Control

We have three methods of setting the *desired wirelength* parameter in the cost function given above. In the first method, *desired wirelength* is set to be the $wirelength_{Approx}$ of the initial solution. In the second method we set *desired wirelength* to be zero to drive $wirelength_{Approx}$ to a minimum while in the third method we set *desired wirelength* to be the value of $wirelength_{Approx}$ measured in the characterization of the original circuit as described in Section 3.3.4.

To evaluate the three different methods of setting $wirelength_{Approx}$ we generated synthetic circuits as described in Section 5.2, placed and routed them as described in Section 5.3, and examined the post-place and route wirelength. We show the results for combinational circuits in Figure 4.17 and the results for sequential circuits in Figure 4.18. In both graphs, we plot the average absolute percent difference in $Wirelength_{bb\ cost}$ cost between the clone circuits and the original circuits versus the number of clusters used in the characterization. Also, in both graphs we have signified the different partitioning conditions with the labels t1, t2, and t3. A summary of what these partitioning conditions mean can be found in Table 4.1.

Table 4.1- Partitioning Conditions for Experiments

Partitioning Condition	Partitioner Type	Node Balancing Condition
t1	k-way	The heaviest cluster's weight is no more than 20% greater than the average cluster's weight
t2	Recursive bi-partitioning	For each bi-partition, there is a no more than 40% difference in weight between the clusters
t3	k-way	The heaviest cluster's weight is no more than 30% greater than the average cluster's weight

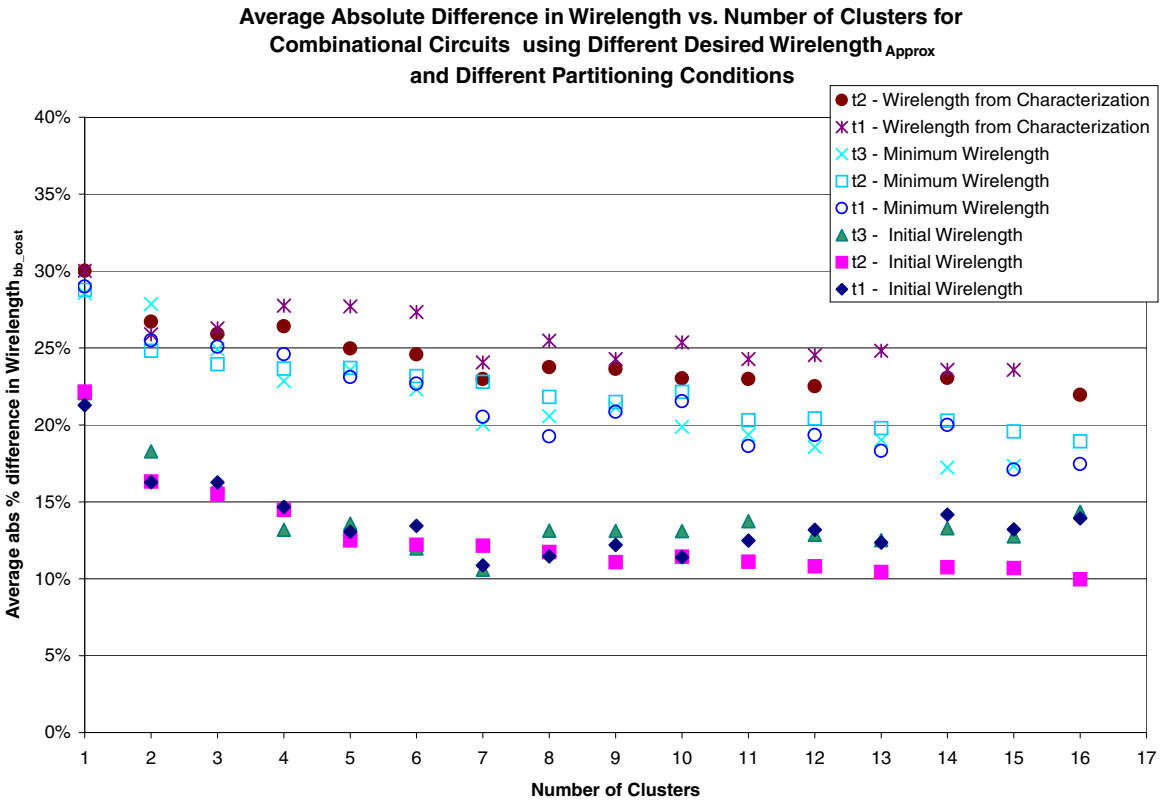


Figure 4.17 – Absolute Difference in Wirelength Cost vs. Number of Clusters for Combinational Circuits

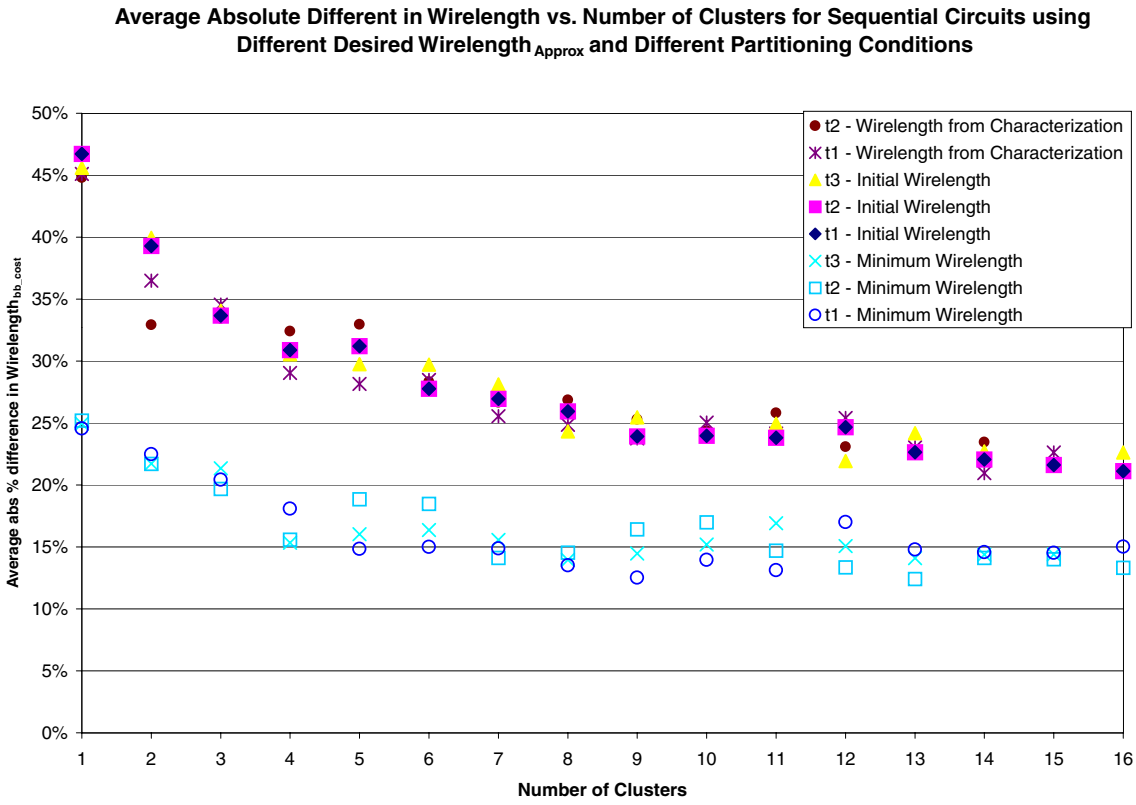


Figure 4.18 – Absolute Difference in Wirelength Costs vs. Number of Clusters for Sequential Circuits

We can see from each graph that that the *desired wirelength* conditions that produced the best set of clones were to accept the initial $wirelength_{Approx}$ for combinational circuits and to minimize $wirelength_{Approx}$ for sequential circuits irrespective of the partitioning conditions. The reason behind the difference between combinational and sequential circuits can be seen in Figure 4.19. It shows a typical relationship between real wirelength and $wirelength_{Approx}$ for two example combinational and sequential circuits from the MCNC benchmark suite. On both graphs, the point at which the real wirelength of the clone matches or would have matched the real wirelength of the original circuit is marked. We defined this point as the *best desired wirelength point*. This point is within the graph for the combinational circuit and not within the graph for the sequential circuits. This relationship was seen in almost all circuits. Cloned

combinational circuits typically used less wirelength than the original circuit at the lowest values of $wirelength_{Approx}$ and more wirelength at the highest levels of $wirelength_{Approx}$. Cloned sequential circuits however, typically used more wirelength at all possible values of $wirelength_{Approx}$. The best desired wirelength point was closest to the initial $\text{wirelength}_{\text{Approx}}$ for combinational circuits while for sequential circuits the best wirelength point was closest to the lowest $wirelength_{Approx}$. This suggests that combinational and sequential circuits have very different structures with sequential circuits being more tightly connected.

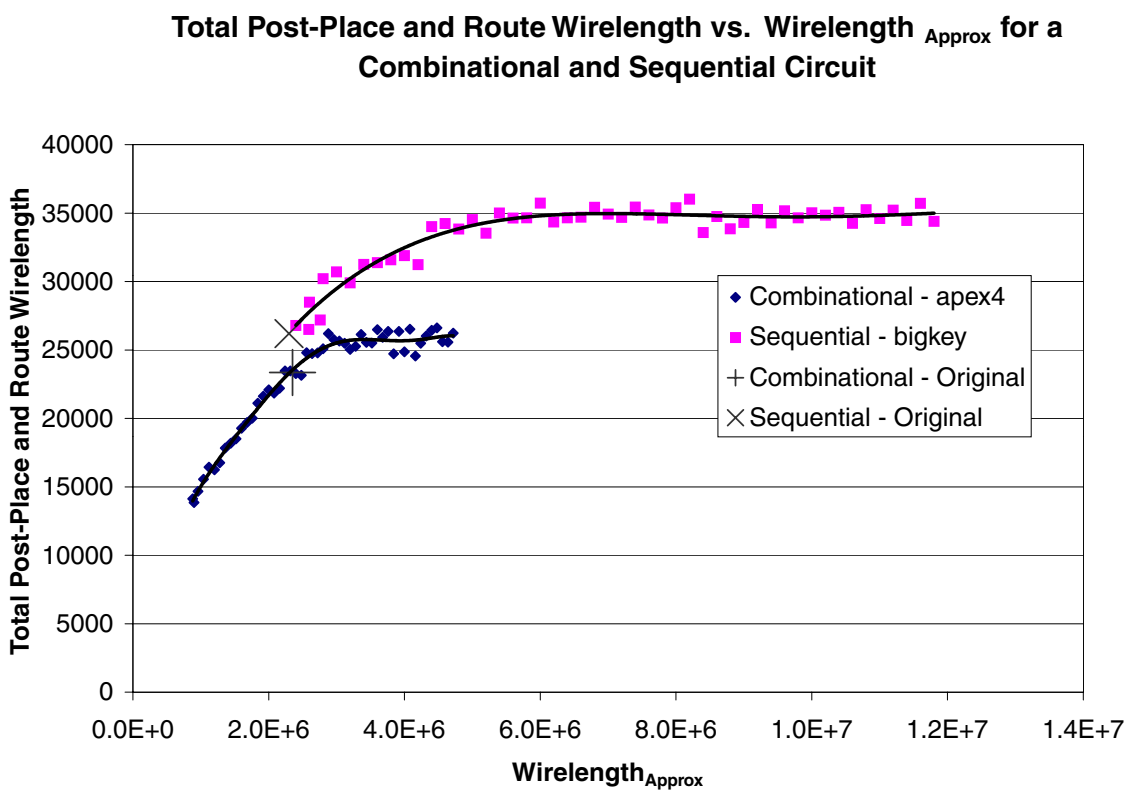


Figure 4.19 - Wirelength vs. $\text{Wirelength}_{\text{Approx}}$

4.6 Final Solution Quality

For each clone, we examined the fidelity of the clones to their original specifications. The metric of fidelity is the average across all generated circuits of the total deviation from characterization normalized to the number of edges. We normalized to the number of non-clock edges because deviations from specification are the result of misplaced edges. In Figure 4.20 we plot the average normalized deviation from specification for the specification of the various shapes (e.g. input shapes and output shapes), the fanout distribution, the edge length distributions, and the Comb matrix versus the number of clusters. Also plotted on the graph is the total over all the characterizations. We can see that the average deviation is under 3% for all characterizations and that the total is under 5% for most cluster sizes.

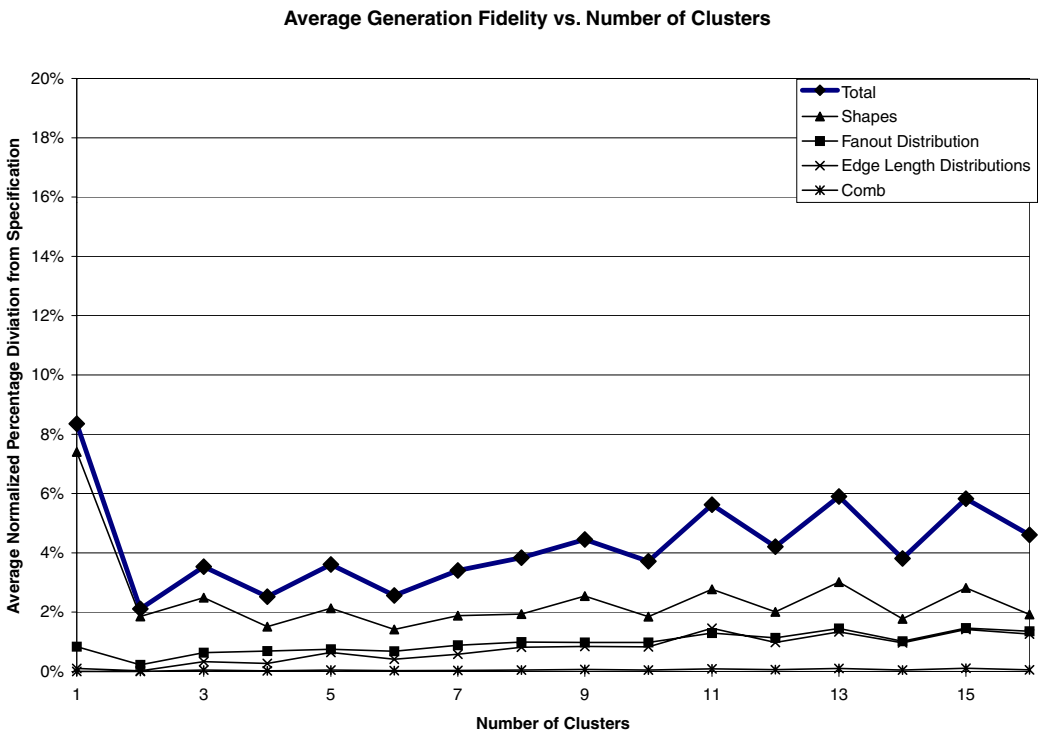


Figure 4.20 - Average Generation Fidelity vs Number of Clusters

4.7 Software Implementation of Generation

We have built an implementation of the algorithm described in this section and called it, *NGen*, after Hutton's *Gen.* NGen takes as input, statistics from NCirc and outputs a circuit in BLIF format. The source code for NGen can be found at:

http://www.eecg.toronto.edu/~jayar/software/software.html

5 MEASUREMENT OF REALISM OF GENERATED CIRCUITS

In this chapter we present measurements of the realism of the synthetically generated circuits. Recall that Hutton determined realism by processing the original circuits and a synthetic clone of those circuits through a CAD process, and comparing the results. We compare on the basis of post-placement and routing wirelength, track count and critical path delay. First, we will present visual validation of a small circuit to elucidate the effect of clustering. Second, we describe the circuits that we cloned and the parameters that are input into generation. Third, we describe the tool used to do the placement and routing, and the FPGA architecture used to make the measurements. Finally, we present and discuss the results.

5.1 Visual Validation

To demonstrate the effect that clustering has on the quality of clones generated, we characterized s526, a small circuit from the MCNC benchmark suite [1], using a single cluster and using two clusters and generated clones from the characterization. We then compared the clones against the original circuit both visually and with post-place and route wirelength.

To visually compare the graphs we used the graph drawing program DOT [27]. Figure 5.1 shows the original circuit s526. In the picture we have used the hMETIS partitioner to identify clusters in the circuit and have coloured these clusters red and blue to bring out the differences in connectivity more clearly. We can see that in the original circuit the clustering is natural in

the sense that each cluster is strongly connected to itself. In Figure 5.2 we have drawn the one-cluster clone (where we have bi-partitioned it to identify any strongly connected clusters that may have been created in generation and have identified those clusters with blue and red) and in Figure 5.3 we have drawn the two-cluster clone. Visually, we can see that the two-cluster clone looks more similar to the original circuit as it contains some of the same locality of connections.

To see if the resemblance is more than just visual we placed and routed the three circuits and compared each clone against the original circuit. The results of that comparison is given in Table 5.1 where we see that the 2-cluster clone does indeed get better wirelength.

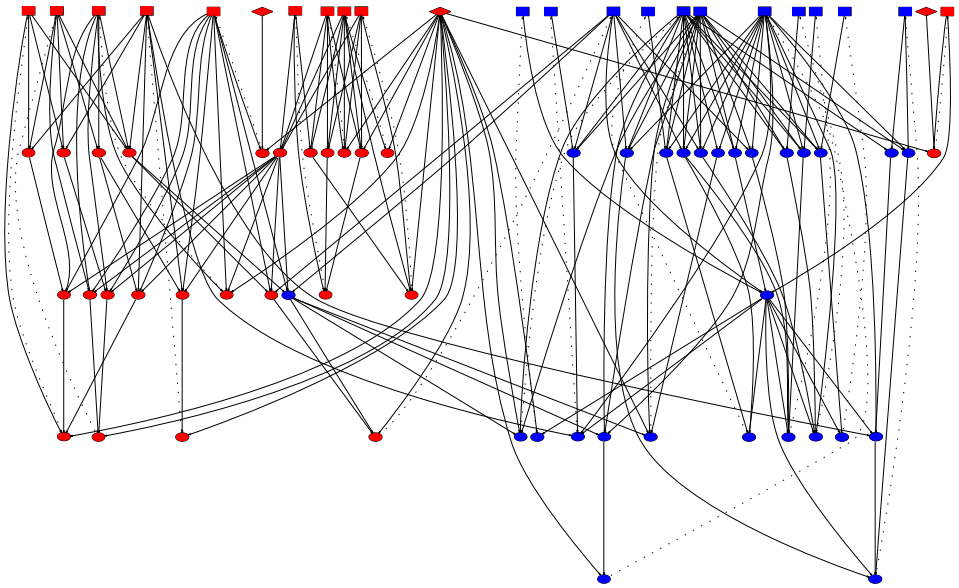


Figure 5.1 - Original Circuit in Two Clusters

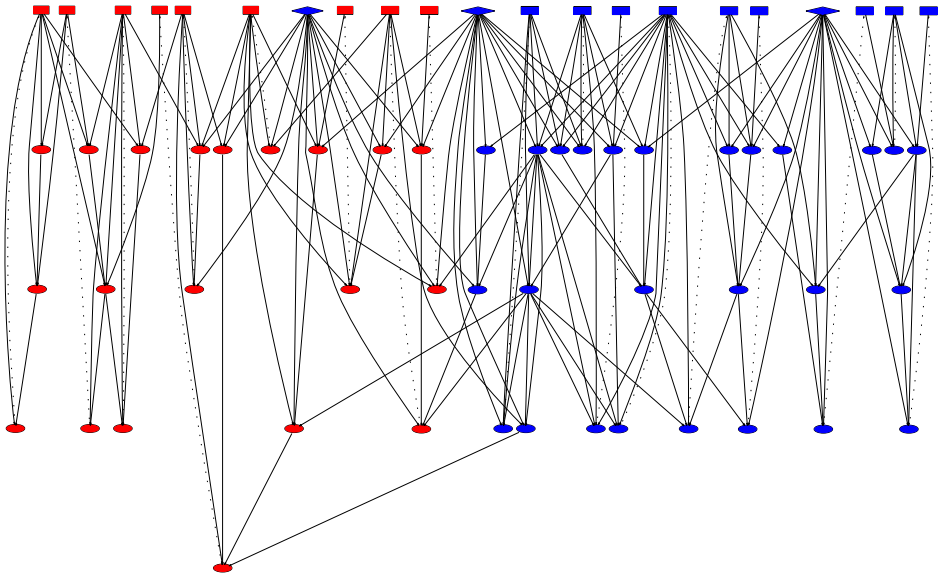


Figure 5.2 - One Cluster Clone

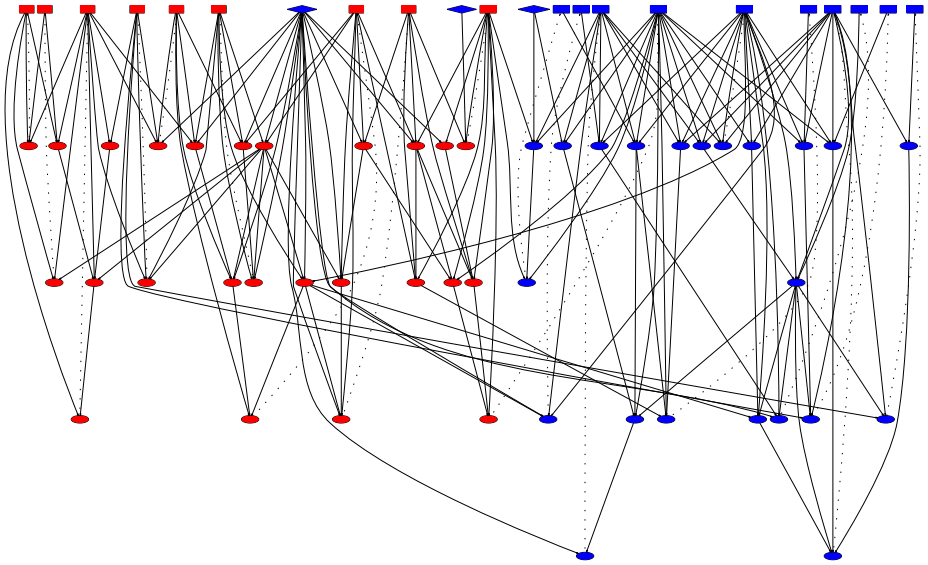


Figure 5.3 - Two Cluster Clone

Table 5.1 - Wirelength results of visual validated circuits

Circuit	Wirelength	%difference
Original	341	
1 Cluster Clone	293	-14%
2 Cluster Clone	338	-1%

5.2 Clone Generation

We used 23 circuits taken from the 17 largest MCNC benchmarks [1] and 6 new circuits created at the University of Toronto. We characterized the circuits with *NCirc* and generated clones with *NGen*.

During characterization, we varied the number of partitions from 1 to 16, in order to study the effect of this parameter. We used both recursive bi-partitioning and *k*-way partitioning types, and used two different node balancing conditions for the two partitioning types.

In generation, for final edge assignment we set *desired wirelength* to the initial $wirelength_{Approx}$ for combinational circuits and zero for sequential circuits, as described in Section 4.5.

5.3 Placement and Routing

The circuits were placed and routed with VPR [11][12]. The FPGA architecture targeted was a simple architecture in which logic blocks are a single 4-input LUT and a flip-flop, the wires span only one logic block, and all routing switches are tri-state buffers. The circuits were routed under high stress routing conditions that attempt to find the smallest number of tracks per channel that allow the circuits to be routed.

5.4 Results

In Figure 5.4, we plot the average of the absolute difference in placement cost between the clone and original circuits versus the number of clusters used in partitioning for clones

generated under the three types of partitioning conditions of Table 4.1. The placement cost we used is the sum over all nets of the half-perimer of their bounding boxes or $\text{Wirelength}_{bb\_cost}$ [12]. The partitioning conditions that produced the best results as measured by placement cost were 8 clusters created through a k-way partitioner that allowed a 20% greater weight in the largest cluster after partitioning.

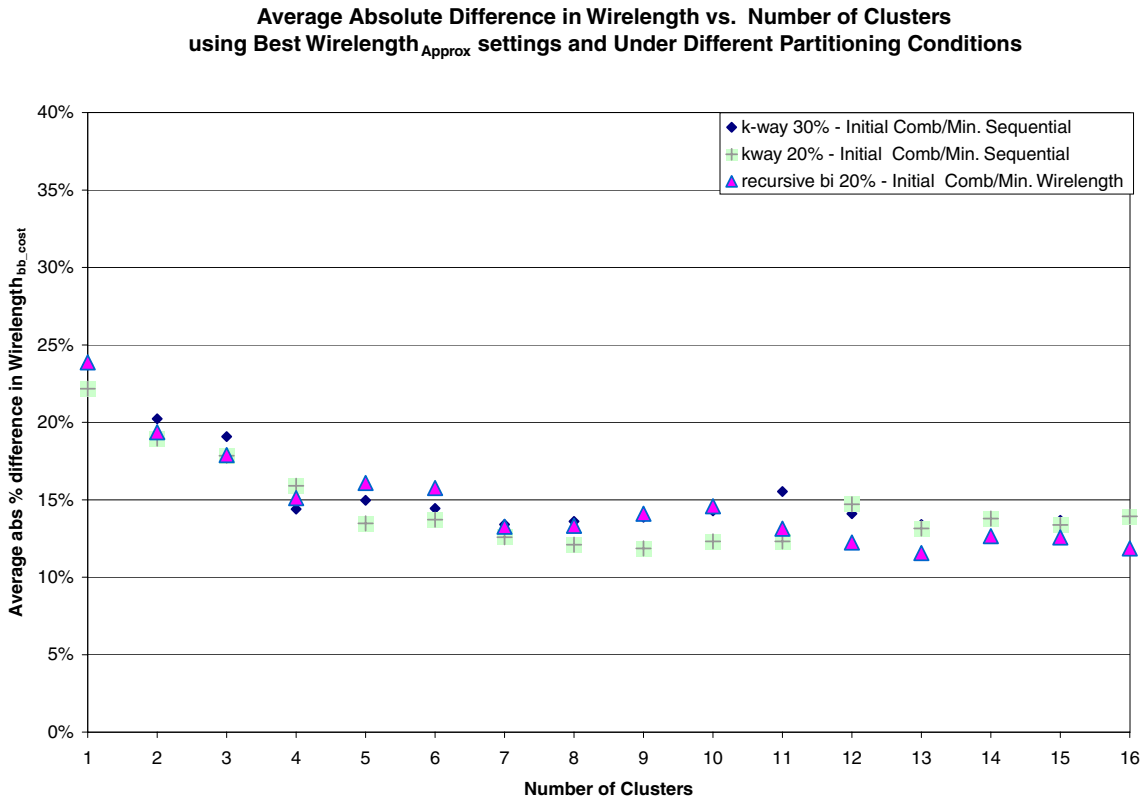


Figure 5.4 - Placement Costs vs. Number of Clusters under Best Conditions

Using these partitioning conditions, we then measured the average absolute differences between the clone and original circuit for the total-post place and route wirelength, the minimum number of tracks needed to route the FPGA, and the critical path delay as a function of the number of clusters used in characterization. The results are plotted the result in Figure 5.5. In this graph we

can see that the minimum number of tracks measurement closely follows that of wirelength while critical path delay shows no correlation to the number of clusters.

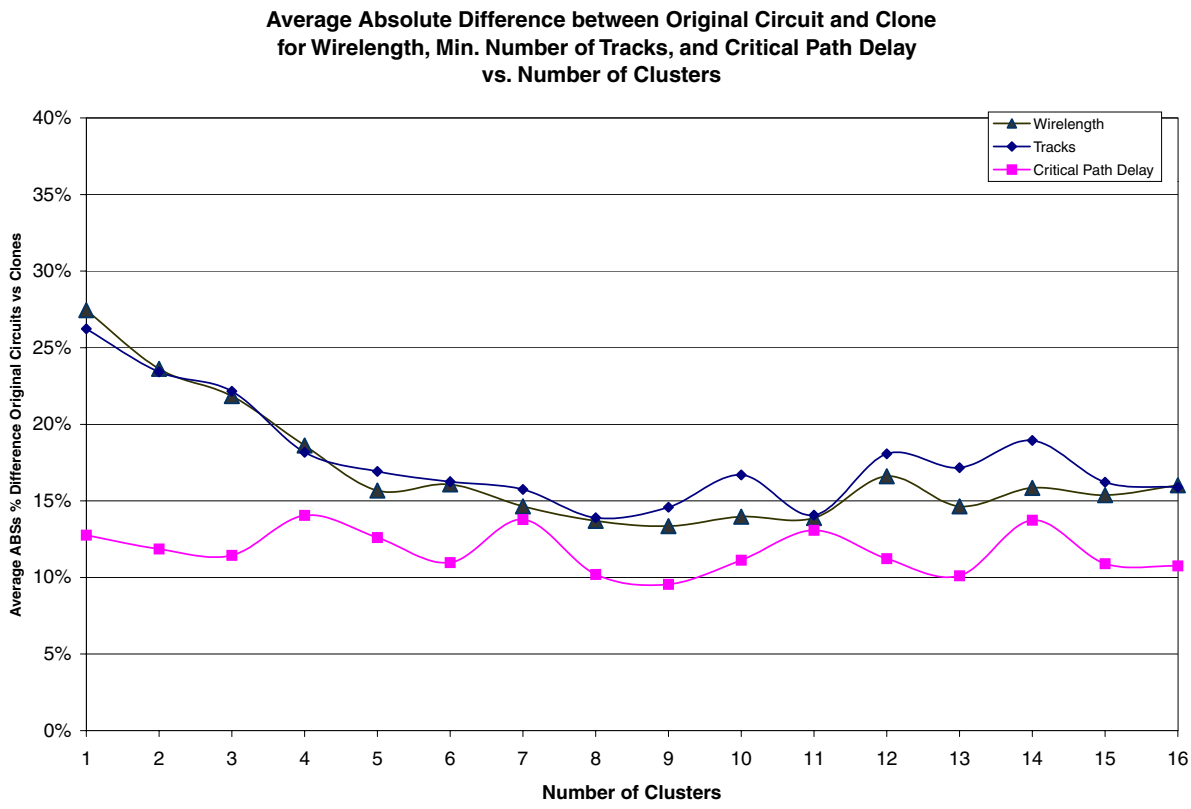


Figure 5.5 – Wirelength, Minimum Number of Tracks, and Critical Path Delay vs. Number of Clusters

In Table 5.2 we give measurements of quality for each circuit for 8 clusters. In the table, Orig. denotes the results for the original circuits, MH denotes the results using Hutton's method [8] to generate clones, and New stands for our new method of generating clones.

As can be seen from Table 5.2, the mean of the average absolute difference in total detailed wirelength between the clone and original circuit is 14%, which is a significant improvement over Hutton's method [8]. The standard deviation of this mean also has a significant improvement. The absolute difference in the number of routing tracks is 14%, which is also a significant improvement compared to Hutton's results. The critical path delay achieves roughly

the same result as Hutton's work - within about 10% of the original circuit on average. In our judgment, over all three of these measurements, the new synthetic circuits are realistic proxies for the real circuits.

Table 5.2 – Comparison between Real and Clone Circuits

Circuit	Size	Total Wirelength			Minimum Number of Tracks			Critical Path Delay		
		Orig	MH % diff	New % diff	Orig	MH % diff	New % diff	Orig	MH % diff	New % diff
alu4	1536	23852	-20%	-8%	14	-21%	-14%	8.4E-08	-18%	8%
apex2	1916	33868	-7%	4%	16	-6%	0%	8.7E-08	-1%	16%
apex4	1270	23059	-16%	-8%	17	-24%	-12%	7.9E-08	-8%	8%
des	1847	31344	49%	22%	10	70%	40%	1.0E-07	-4%	-10%
ex5p	1072	20777	-12%	-14%	17	-12%	-12%	7.1E-08	-3%	1%
ex1010	4608	76083	20%	17%	15	20%	20%	1.6E-07	-16%	-10%
misex3	1411	24100	-13%	-4%	15	-13%	0%	8.6E-08	-19%	-2%
pdc	4591	110830	-13%	12%	23	-22%	13%	2.2E-07	-43%	-39%
seq	1791	33246	-18%	1%	17	-18%	-6%	9.2E-08	-16%	-10%
spla	3706	77666	-1%	18%	22	-14%	0%	1.3E-07	-13%	7%
bigkey	2159	26476	17%	14%	9	78%	22%	5.7E-08	-6%	3%
diffeq	1934	18913	59%	15%	12	42%	0%	7.9E-08	-5%	0%
dsip	1822	23317	-19%	14%	9	22%	11%	7.9E-08	-35%	-11%
elliptic	4854	58017	66%	31%	16	44%	31%	1.1E-07	-13%	-12%
frisc	4444	69611	62%	17%	20	55%	5%	1.4E-07	13%	-5%
s298	1941	25423	8%	0%	11	36%	9%	1.4E-07	-11%	14%
tseng	1482	11520	104%	23%	11	64%	9%	5.5E-08	36%	19%
display_chip	2417	19158	116%	2%	10	90%	0%	7.6E-08	13%	-3%
img_interp	3424	32545	76%	25%	12	58%	17%	9.3E-08	30%	11%
input_chip	1106	7526	83%	11%	8	88%	25%	5.6E-08	16%	8%
peak_chip	1146	6759	60%	4%	9	22%	-11%	8.0E-08	2%	5%
scale125_chip	3856	26834	165%	29%	10	150%	40%	8.8E-08	25%	28%
scale2_chip	1524	11125	99%	19%	9	89%	22%	6.8E-08	15%	5%
abs mean			48%	14%		46%	14%		16%	10%
abs stddev			43%	9%		36%	12%		11%	9%

To ensure that we have not over-tuned our algorithms to the circuits in our test set, we verified our results with a second set of circuits. The second set of circuits consists of fifteen circuits from Sun's Pico Java Processor [28] and two MCNC circuits (s38417 and s38584.1) that were not used in the original test set. We characterized and generated clones of the circuits as in Section 5.2 and place and routed the circuits as in Section 5.3. We then measured the average absolute differences between clone and original circuit for the total-post place and route wirelength, the minimum number of routing tracks needed to route the FPGA, and the critical

path delay as a function of the number of clusters used in characterization. The results are plotted in Figure 5.6. The wirelength and minimum number of routing track results decrease rapidly with the number of clusters until they start to plateau at around 8 clusters, just as with the original test set. The absolute percent difference for these results at 8 clusters is 20% and 21% respectively, which is slightly higher than with our original test set. The critical path delay results are on par with the previous test set.

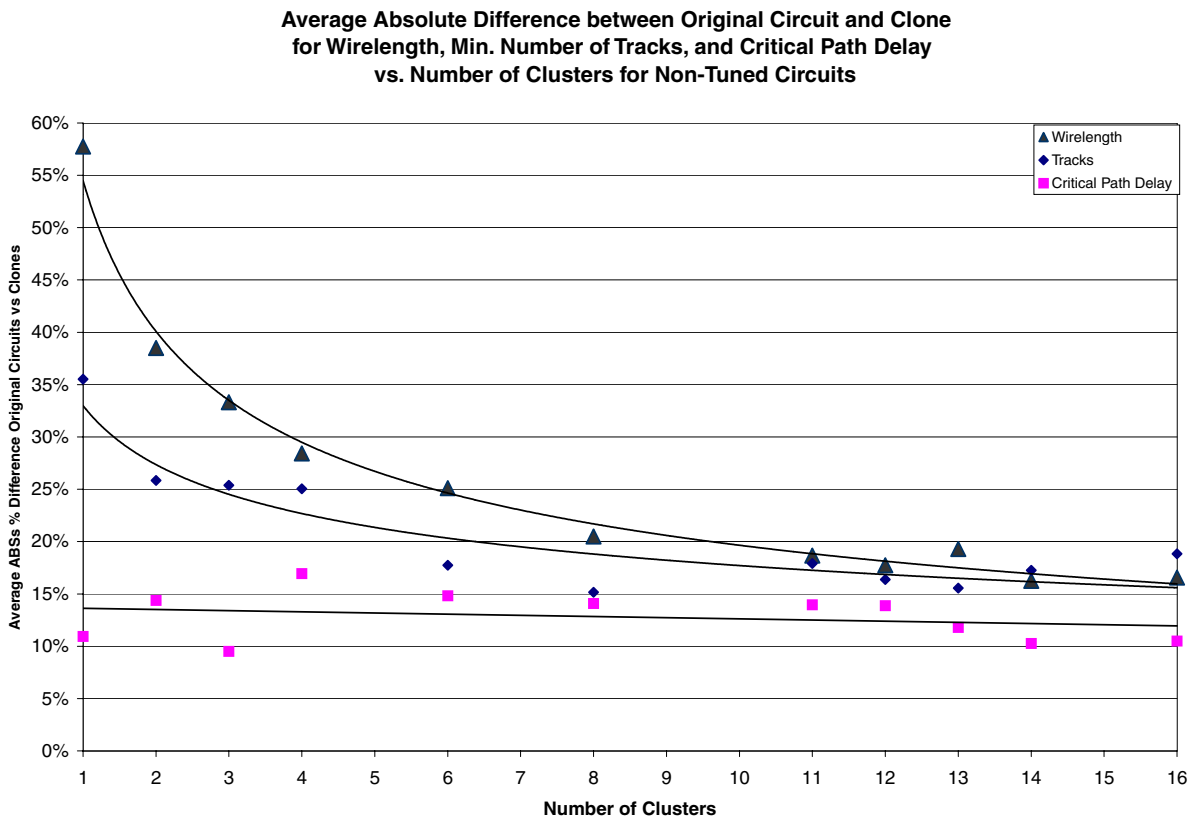


Figure 5.6 - Wirelength, Minimum Number of Tracks, and Critical Path Delay vs. Number of Clusters for Non–Tuned Circuits

In Table 5.3 we give measurements of quality for each circuit in the second test set for 8 clusters. In the table, the blanks in the MH columns indicate circuits that caused Hutton's method to crash. We can see that with our new method the mean and standard deviation of the

average absolute difference in total detailed wirelength between the clone and original circuit still shows a significant improvement over Hutton's method. If we look at the wirelength result for the two MCNC circuits, s38417 and s38584.1, we can see why the average wirelength results for the second test set is slightly higher than the first. The wirelength results for these two circuits are drastically higher than their original circuits; however, the results are still significantly better than those obtained using Hutton's method. We do not know why these two circuits use excessive wirelength, however with increasing number of clusters the wirelength difference decreases reaching 71% and 49% respectively with 24 clusters. For almost all other circuits the wirelength difference between the clone and original circuit is less than 14%. The average wirelength for these circuits is 11%, which is less than the average found for the first set of test circuits.

Table 5.3- Comparison between Real and Clone Circuits for Second Test Set

Circuit	Size	Total Wirelength			Minimum Number of Tracks			Critical Path Delay		
		Orig	MH % diff	New % diff	Orig	MH % diff	New % diff	Orig	MH % diff	New % diff
prils_dp	501	4874	12%	8%	11	0%	0%	8.5E-08	28%	24%
rsadd_dp	521	4546	26%	18%	9	0%	47%	1.4E-07	16%	2%
code_seq_dp	588	5110	-29%	19%	8	13%	6%	7.8E-08	-7%	19%
dcu_dpath	1590	23193	62%	6%	19	26%	8%	6.4E-08	22%	4%
ex_dpath	3925	133554	39%	7%	17	59%	0%	2.6E-07	23%	11%
exponent_dp	644	7543	16%	7%	12	25%	8%	8.3E-08	17%	38%
icu_dpath	3813	69064	65%	9%	19	68%	7%	1.3E-07	36%	10%
incmod	1007	11319		1%	12		7%	1.8E-07		3%
imdr_dpath	1410	22384		3%	15		8%	1.8E-07		6%
mantissa_dp	1284	32050		10%	15		13%	6.3E-08		3%
multmod_dp	1893	22532	78%	4%	13	77%	0%	1.3E-07	10%	47%
pipe_dpath	798	7351	4%	0%	8	63%	19%	5.2E-08	8%	0%
smu_dpath	866	10023		10%	9		33%	1.5E-07		14%
ucode_dat	1806	43554		9%	16		82%	8.8E-08		13%
ucode_reg	230	799	86%	48%	3	133%	0%	2.5E-08	-36%	0%
s38417	7465	71038	201%	100%	11	200%	33%	8.6E-08	23%	3%
s38584.1	7489	69751		90%	11		82%	8.8E-08		47%
abs mean			56%	20%		60%	21%		20%	14%
abs stddev			55%	30%		61%	27%		11%	16%

Because the average absolute difference in total detailed wirelength and minimum number of routing tracks needed between the clone and the original circuits for the second test set is within 6% and 7% respectively of the first test set, because for almost all circuits in the second test set

the wirelength results are lower than the average of the first test set, and because the critical path delay results are on par with those in the first test set we feel we have not over-tuned our algorithms.

6 CONCLUSIONS AND FUTURE WORK

6.1 SUMMARY

We have introduced a new circuit characterization and new synthetic generation techniques that significantly improve the quality of synthetic circuits over previous methods.

The new characterization is an extension of the characterization of [7] to capture the natural hierarchy of a circuit. Natural hierarchy was captured through partitioning the circuit into clusters and characterizing each cluster and the connections between the clusters.

Our new generation techniques impose this natural hierarchy on the synthetic circuits. The generation techniques use iteration to tightly control the generation process in contrast to all known synthetic circuit generators that use constructive approaches.

The new synthetic generation techniques were judged realistic by cloning real circuits and comparing clones on the basis of post place and route statistics. The real and clone circuits differed by 14% for total detailed wirelength, 14% for minimum number of tracks needed to route each circuit, and 10% for critical path delay.

6.2 Specific Contributions

The contributions of this thesis are:

- A new simpler sequential circuit model that allows the natural hierarchy found in real circuits to be identified

- The introduction of clustering into characterization and generation to identify and impose the natural hierarchy found in real circuits
- The introduction of the idea of iteration into synthetic circuit generation
- Several new algorithms to:
    - Create the delay structure
    - Partition the fanout distribution among the level nodes
    - Perform final edge assignment
- A software tool NCirc to characterize real circuits
- A software tool NGen to generate synthetic circuits
- Significant improvements in the quality of synthetic circuits produced

6.3 Future Work

Several areas are open to future research. One area is to see how circuit structures combine and scale with size so that we can generate larger circuits. A second area is to explore alternatives to using $wirelength_{Approx}$ to control wirelength during synthetic circuit generation. One such alternative would be to place the circuit during final edge assignment on an FPGA to obtain positions for the individual nodes in the graph and then use this information to obtain the precise wirelength information for edges. A third area is to examine the use of different partitioners in characterization to see what effect they have on synthetic circuit quality. A fourth area of research is to prove the realism of synthetic circuits by showing that their substitution for real circuits would not affect the conclusion of any FPGA architecture or CAD tool algorithm experiment. A fifth area of research is to explore something we noticed while examining how the node shape for a circuit sub-divides under clustering.

To describe what we noticed we first need to discuss one of Hutton's findings. Hutton found that the node shape for whole circuits tended to fall into one of three identifiable classes:

decreasing (decrease uniformly from the inputs), conical (increase to a maximum and then decreases), and two maxima (similar to conical but possessing two maxima) [7]. What we noticed is that circuits with one of the three identifiable shapes tended to have good wirelength results with Hutton's method whereas circuits that did not fall into one of the three identifiable classes tended to have excessive wirelength. We also noticed that if we partitioned a circuit into small enough clusters the node shapes for the clusters did fall into one of the three classes. For example, in Figure 6.1 we show the unclassifiable node shape of sequential circuit s298 subdivided into 16 clusters where the node shape of each cluster can be classified as conical.

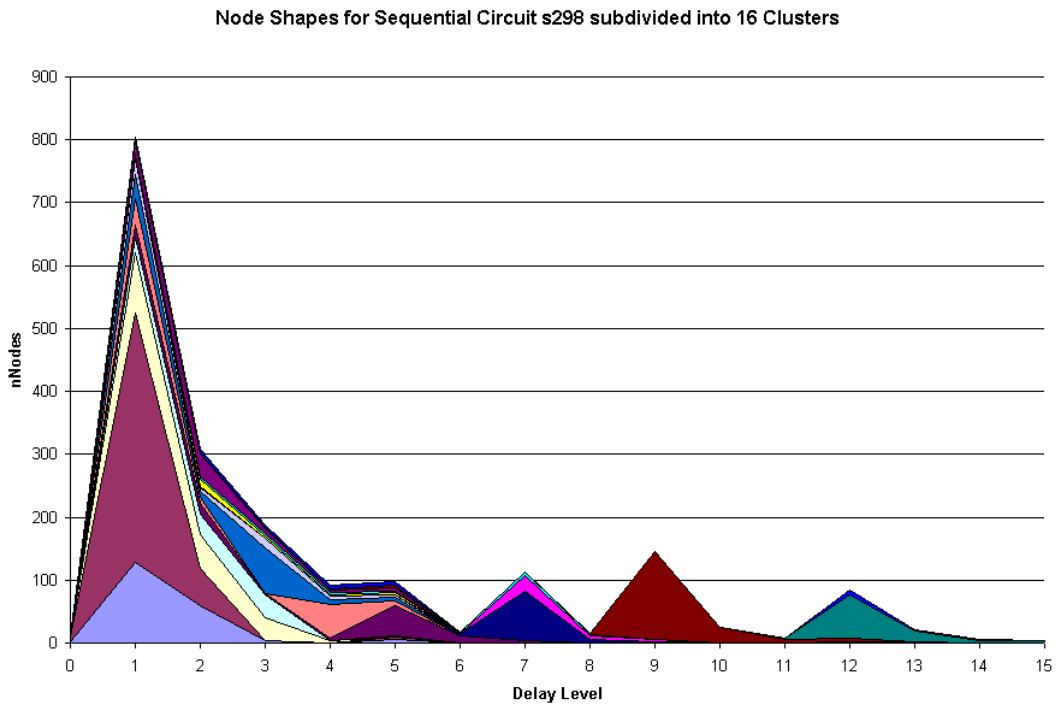


Figure 6.1 - Node Shapes for Sequential Circuit

If all clusters of small enough size fit into one of three categories of shapes, and if Hutton's method obtains good wirelength results for logic for these categories then maybe the answer to the question of how many clusters are natural for a given circuit is to partition the circuit down until each cluster is one of the three given shapes.

Appendices

A Circuit Characterizations for 8 Clusters

The following is the list of circuit characterizations for 8 clusters using the partition condition t1, which is described in Table 4.1 (k-way partitioner with the heaviest cluster's weight being no more than 20% greater than the average cluster's weight). The circuits are organized alphabetically.

alu4

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1536	230	178	179	230	178	184	179	178
Number of PI	14	5	1	2	4	1	0	1	0
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1522	225	177	177	226	177	184	178	178
Number of PO	8	1	0	1	2	1	1	1	1
Number of Edges	5400	1633	795	970	1442	786	772	778	681
Number of Intra-Cluster Edges	2943	570	265	318	524	270	389	294	313
Number of Inter-Cluster Input Edges	4914	243	362	309	294	340	275	334	300
Number of Inter-Cluster Output Edges	4914	820	168	343	624	176	108	150	68
Wirelength Approx	2.53e+06	432975	268019	317959	425942	264143	285238	267822	268202
Scaled Cost	3.56								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.5 ± 20	6 ± 32	2.4 ± 14	3.6 ± 23	5 ± 28	2.5 ± 12	2.7 ± 3.9	2.4 ± 10	2.1 ± 2.9
Avg. Comb. Fanout	1.6 ± 2.1	1.2 ± 0.8	1.4 ± 1.1	1.2 ± 0.7	1.2 ± 0.9	1.6 ± 1.7	2.7 ± 3.9	1.7 ± 2.1	2.1 ± 2.9
Avg. PI Fanout	205 ± 31	221 ± 20	185 ± 0	219 ± 0	214 ± 7	155 ± 0	N/A	127 ± 0	N/A
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.5 ± 0.6	3.6 ± 0.5	3.5 ± 0.6	3.5 ± 0.6	3.6 ± 0.5	3.4 ± 0.7	3.6 ± 0.5	3.5 ± 0.6	3.4 ± 0.6
Max Fanout	249	249	185	219	221	155	23	127	18

Node Shape										PO Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	14	5	1	2	4	1	0	1	0	0	0	0	0	0	0	0	0	0	
1	692	156	77	96	158	64	40	55	46	0	0	0	0	0	0	0	0	0	
2	518	55	59	53	50	70	82	69	80	0	0	0	0	0	0	0	0	0	
3	198	11	26	17	14	29	35	31	35	1	0	0	0	1	0	0	0	0	
4	80	2	11	7	4	9	19	17	11	1	0	0	0	1	0	0	0	0	
5	21	1	2	3	0	2	4	4	5	1	1	0	0	0	0	0	0	0	
6	11	0	2	1	0	2	3	2	1	3	0	0	1	0	0	0	1	1	
7	2	0	0	0	0	1	1	0	0	2	0	0	0	0	1	1	0	0	

Input Shape										Output Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	0	0	0	0	0	0	0	0	0	2867	1106	185	438	856	155	0	127	0	
1	2298	558	255	323	558	186	121	173	124	1700	216	147	143	226	177	353	194	244	
2	1931	203	221	195	190	261	309	252	300	529	55	60	53	50	72	83	70	86	
3	741	41	96	65	54	108	133	116	128	197	11	26	17	13	29	35	31	35	
4	298	7	39	28	16	35	70	65	38	79	2	11	7	3	9	19	17	11	
5	82	4	8	12	0	8	15	15	20	20	0	2	3	0	2	4	4	5	
6	42	0	8	4	0	8	12	7	3	8	0	2	0	0	2	3	1	0	
7	8	0	0	0	0	4	4	0	0	0	0	0	0	0	0	0	0	0	

Latched Shape										Intra-Cluster Edge Length Distribution									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	4494	508	225	279	473	211	338	239	268	
2	0	0	0	0	0	0	0	0	0	757	55	38	37	47	52	43	49	45	
3	0	0	0	0	0	0	0	0	0	125	7	2	1	2	7	8	5	0	
4	0	0	0	0	0	0	0	0	0	23	0	0	1	2	0	0	1	0	
5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	215	300	258	251	259	195	256	219	4494	636	140	272	473	144	97	127	64
2	0	23	48	34	32	61	59	61	73	757	147	27	53	116	25	9	11	3
3	0	5	14	13	9	16	12	16	8	125	33	0	12	31	4	2	10	1
4	0	0	0	4	2	3	9	1	0	23	4	1	5	4	3	0	2	0
5	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (8 1267 67 41 32 33 14 13 11 3 2 9 9 5 4 0 0 1 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 2 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 3 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (1 196 10 9 4 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0, 0 0 0 0 0 0 0 0 1)
Cluster 2: (0 152 9 2 5 5 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (1 153 6 13 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 4: (2 196 11 6 4 4 2 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 1)
Cluster 5: (1 145 8 4 6 2 4 2 2 2 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (1 143 3 1 3 5 2 6 3 0 1 2 7 2 2 0 0 1 0 0 1 0 0 1)
Cluster 7: (1 146 5 5 6 5 0 2 2 0 0 5 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (1 136 15 1 2 6 3 2 2 1 1 2 0 3 2 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	150	116	145	105	92	105	107	0	0	0	0	0	0	0	0
57	0	20	20	21	21	13	16	0	0	0	0	0	0	0	0
52	72	0	80	59	26	35	19	0	0	0	0	0	0	0	0
93	94	123	0	87	63	90	74	0	0	0	0	0	0	0	0
15	12	19	27	0	46	41	16	0	0	0	0	0	0	0	0
9	16	12	8	24	0	16	23	0	0	0	0	0	0	0	0
13	13	18	11	28	22	0	45	0	0	0	0	0	0	0	0
4	5	1	3	16	5	34	0	0	0	0	0	0	0	0	0

apex2

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1916	238	239	239	257	257	229	229	228
Number of PI	38	7	3	5	8	8	4	0	3
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1878	231	236	234	249	249	225	229	225
Number of PO	3	0	1	0	0	0	2	0	0
Number of Edges	6689	1058	1158	1236	1468	1410	894	939	999
Number of Intra-Cluster Edges	4216	576	508	532	635	653	443	447	422
Number of Inter-Cluster Input Edges	4946	249	341	307	246	233	353	363	381
Number of Inter-Cluster Output Edges	4946	233	309	397	587	524	98	129	196
Wirelength Approx	2.18e+06	267014	287921	281762	304252	291119	248449	253275	249963
Scaled Cost	2.93								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.4 ± 11	3.3 ± 8	3.4 ± 8	3.8 ± 14	5 ± 17	5 ± 15	2.3 ± 6	2.5 ± 5	2.7 ± 7
Avg. Comb. Fanout	2.1 ± 3.9	2.0 ± 2.4	2.9 ± 7	2.0 ± 2.7	1.8 ± 2.3	2.1 ± 3.5	1.9 ± 3.1	2.5 ± 5	1.9 ± 2.2
Avg. PI Fanout	69 ± 37	48 ± 15	44 ± 11	91 ± 42	96 ± 31	81 ± 33	26 ± 25	N/A	60 ± 7
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.5 ± 0.6	3.5 ± 0.5	3.5 ± 0.5	3.5 ± 0.6	3.5 ± 0.6	3.5 ± 0.6	3.5 ± 0.6	3.5 ± 0.5	3.5 ± 0.6
Max Fanout	147	74	85	142	147	133	67	55	69

Node Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	38	7	3	5	8	8	4	0	3
1	533	80	36	56	124	109	45	31	52
2	721	65	93	105	94	85	87	99	93
3	399	59	65	48	22	43	49	57	56
4	151	21	24	19	7	10	25	28	17
5	48	4	10	5	2	2	10	9	6
6	19	2	5	1	0	0	6	4	1
7	4	0	2	0	0	0	1	1	0
8	3	0	1	0	0	0	2	0	0

PO Shape

Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
3	0	1	0	0	0	2	0	0

Input Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	1742	268	114	179	419	365	138	93	166
2	2609	235	325	390	346	311	322	344	336
3	1499	221	250	178	84	164	172	219	211
4	565	79	93	68	25	38	96	101	65
5	178	14	38	20	7	8	37	33	21
6	68	8	17	4	0	0	19	16	4
7	16	0	8	0	0	0	4	4	0
8	12	0	4	0	0	0	8	0	0

Output Shape

Circuit	Cluster 1	2	3	4	5	6	7	8
2616	333	131	456	765	648	104	0	179
2311	213	386	263	328	364	228	310	219
1140	177	194	137	97	110	118	167	140
400	59	65	48	23	43	49	57	56
151	21	24	19	7	10	25	28	17
48	4	10	5	2	2	10	9	6
19	2	5	1	0	0	6	4	1
4	0	2	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0

Latched Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0

Intra-Cluster Edge Length Distribution

Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
5190	474	411	358	498	540	327	395	364
1296	90	94	157	133	87	96	41	51
157	10	3	14	3	25	14	11	3
39	2	0	3	1	1	4	0	3
5	0	0	0	0	0	1	0	1
2	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution

Edge Length	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	0	178	212	207	205	183	273	268	297
2	0	61	99	87	38	48	73	81	60
3	0	8	25	7	3	1	5	4	21
4	0	2	3	6	0	1	1	9	3
5	0	0	1	0	0	0	1	1	0
6	0	0	1	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0

Inter-cluster Output Edge Length Distribution

Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
5190	173	259	282	374	406	69	111	149
1296	55	45	99	186	81	25	17	39
157	4	4	13	16	31	2	1	3
39	1	1	2	10	6	1	0	4
5	0	0	0	1	0	1	0	1
2	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Fanout Distribution

Circuit: (3 1410 132 80 70 34 46 24 7 11 11 8 9 6 1 6 0 2 2 1 3 0 1 3 0 3 1 0 1 1 0 3 0 1 0 0 0 2,
1 1 1 1 0 0 0 1 1 0 1 2 0 0 0 0 0 3 0 1 0 0 0 0 0 1 0 0 1 1 0 2 0 0 0 0 2 0 1 0 0 0 0 1 0 0 0 1 0 0,
0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 0 0 0,
0 0 0 0 1 0 0 0 0 1)

Cluster 1: (0 165 17 14 4 6 19 2 0 0 1 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 0 0,
1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1)

Cluster 2: (1 178 9 9 10 4 3 2 3 3 2 0 3 1 1 1 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0,
0 0 0 1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 3: (0 181 14 11 7 5 1 2 1 1 3 2 2 1 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1,
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0,
0 1)

Cluster 4: (0 186 28 7 10 3 3 6 1 1 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 1)

Cluster 5: (0 187 20 12 10 2 3 6 1 1 0 1 1 0 0 1 0 0 0 0 1 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 6: (2 174 15 9 8 1 7 2 0 2 2 0 1 2 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 7: (0 173 13 6 10 6 7 3 1 1 1 1 0 1 0 1 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 8: (0 166 16 12 11 7 3 1 0 2 1 4 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies

Comb								Latched							
0	86	38	11	17	37	15	29	0	0	0	0	0	0	0	0
54	0	65	5	23	68	61	33	0	0	0	0	0	0	0	0
60	127	0	95	31	29	25	30	0	0	0	0	0	0	0	0
46	82	166	0	71	49	79	94	0	0	0	0	0	0	0	0
72	24	17	76	0	113	95	127	0	0	0	0	0	0	0	0
7	10	3	15	17	0	27	19	0	0	0	0	0	0	0	0
4	4	7	6	30	29	0	49	0	0	0	0	0	0	0	0
6	8	11	38	44	28	61	0	0	0	0	0	0	0	0	0

apex4

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1270	159	158	159	159	160	158	159	158
Number of PI	9	0	0	0	0	2	7	0	0
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1261	159	158	159	159	158	151	159	158
Number of PO	18	1	6	4	1	0	0	2	4
Number of Edges	4460	905	653	843	906	929	821	639	615
Number of Intra-Cluster Edges	2609	316	263	324	326	399	395	287	299
Number of Inter-Cluster Input Edges	3702	225	299	216	210	197	151	293	260
Number of Inter-Cluster Output Edges	3702	364	91	303	370	333	275	59	56
Wirelength Approx	1.39e+06	170452	153973	166646	163210	215516	186886	168538	165391
Scaled Cost	3.32								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.5 ± 12	4 ± 13	2.2 ± 5	3.9 ± 11	4 ± 13	5 ± 21	4 ± 14	2.1 ± 2.0	2.2 ± 1.8
Avg. Comb. Fanout	2.8 ± 8	4 ± 13	2.2 ± 5	3.9 ± 11	4 ± 13	2.1 ± 2.4	1.4 ± 1.0	2.1 ± 2.0	2.2 ± 1.8
Avg. PI Fanout	93 ± 58	N/A	N/A	N/A	N/A	194 ± 14	64 ± 24	N/A	N/A
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.5 ± 0.5	3.4 ± 0.4	3.5 ± 0.5	3.3 ± 0.5	3.3 ± 0.5	3.7 ± 0.5	3.6 ± 0.5	3.6 ± 0.5	3.5 ± 0.5
Max Fanout	207	80	65	75	83	207	118	8	8

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	9	0	0	0	0	2	7	0	0	0	0	0	0	0	0	0	0	0
1	123	8	1	6	10	19	79	0	0	0	0	0	0	0	0	0	0	0
2	574	92	58	80	93	107	55	45	44	0	0	0	0	0	0	0	0	0
3	387	43	62	52	41	27	16	79	67	0	0	0	0	0	0	0	0	0
4	127	12	24	15	12	5	1	25	33	1	0	0	1	0	0	0	0	0
5	37	3	7	6	3	0	0	8	10	4	0	0	3	1	0	0	0	0
6	13	1	6	0	0	0	0	2	4	13	1	6	0	0	0	0	2	4

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	834	0	0	0	0	387	447	0	0
1	394	24	3	18	29	52	268	0	0	1563	454	65	336	474	120	114	0	0
2	1954	301	184	251	298	424	213	146	137	1457	162	192	213	165	189	92	233	211
3	1471	159	238	198	157	102	61	307	249	445	49	66	61	43	31	16	80	99
4	468	44	92	56	40	18	4	95	119	128	12	24	14	12	5	1	25	35
5	124	10	23	17	12	0	0	24	38	33	3	7	3	2	0	0	8	10
6	49	3	22	0	0	0	0	8	16	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	3911	309	252	314	310	201	297	285	289
2	0	0	0	0	0	0	0	0	0	546	7	11	10	16	198	98	2	10
3	0	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	184	269	200	184	184	133	266	234	3911	354	87	295	361	231	213	57	56
2	0	41	30	16	25	13	18	26	25	546	10	4	8	9	100	61	2	0
3	0	0	0	0	1	0	0	1	1	3	0	0	0	0	2	1	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (18 813 144 87 59 60 36 11 3 0 1 3 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0, 0 0 2 1 0 1 1 1 0 0 0 4 0 0 0 2 1 0 0 0 1 0 2 2 1 0 1 0 0 1 0 0 0 0 0 2 1 1 0 0 0 1 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (1 109 23 9 1 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1, 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1)
Cluster 2: (6 95 17 13 14 10 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (4 87 25 15 8 8 5 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (1 107 27 6 6 2 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 5: (0 93 31 12 8 6 0 1 0 0 1 3 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (0 115 16 12 2 4 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1 0 0 0 0 0 2 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (2 111 2 7 5 9 17 5 1)
Cluster 8: (4 96 3 13 15 13 10 3 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	81	63	64	36	15	58	47	0	0	0	0	0	0	0	0
16	0	18	11	9	2	20	15	0	0	0	0	0	0	0	0
39	63	0	55	24	21	47	54	0	0	0	0	0	0	0	0
72	76	73	0	36	14	45	54	0	0	0	0	0	0	0	0
57	27	19	40	0	96	57	37	0	0	0	0	0	0	0	0
37	27	35	34	81	0	39	22	0	0	0	0	0	0	0	0
2	11	4	5	5	1	0	31	0	0	0	0	0	0	0	0
2	14	4	1	6	2	27	0	0	0	0	0	0	0	0	0

bigkey

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	2151	322	240	248	240	280	281	270	270
Number of PI	228	155	29	19	25	0	0	0	0
Number of DFF	224	0	24	28	26	36	38	36	36
Number of Combinational Nodes	1923	167	211	229	215	280	281	270	270
Number of PO	193	2	22	23	20	31	32	33	30
Number of Edges	6332	1438	753	782	759	1496	1678	900	864
Number of Intra-Cluster Edges	3994	644	390	413	389	592	630	468	468
Number of Inter-Cluster Input Edges	4676	46	308	333	325	312	258	396	360
Number of Inter-Cluster Output Edges	4676	748	55	36	45	592	790	36	36
Wirelength Approx	1.92e+06	277865	208288	225454	212182	267291	247380	242548	243646
Scaled Cost	2.19								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.9 ± 21	4 ± 36	1.8 ± 1.9	1.8 ± 1.8	1.8 ± 1.8	4 ± 30	5 ± 31	1.8 ± 2.0	1.8 ± 2.0
Avg. Comb. Fanout	1.9 ± 18	0.9 ± 0.1	1.0 ± 0.2	1.0 ± 0.2	1.0 ± 0.2	3.8 ± 32	5 ± 33	1.0 ± 0.2	1.0 ± 0.2
Avg. PI Fanout	6 ± 43	8 ± 52	2.7 ± 1.9	2 ± 0	2 ± 0	N/A	N/A	N/A	N/A
Avg. DFF Fanout	7 ± 0	N/A	7 ± 0	7 ± 0	7 ± 0	7 ± 0	7 ± 0	7 ± 0	7 ± 0
Avg. Comb. Fanin	3.5 ± 0.8	3.9 ± 0.1	3.5 ± 0.8	3.5 ± 0.8	3.5 ± 0.8	3.5 ± 0.8	3.5 ± 0.8	3.5 ± 0.8	3.5 ± 0.8
Max Fanout	460	460	9	7	7	448	448	7	7

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	452	155	53	47	51	36	38	36	36	188	0	19	23	20	31	32	33	30
1	573	166	62	61	59	56	61	54	54	2	1	1	0	0	0	0	0	0
2	900	1	99	112	104	152	144	144	144	1	1	0	0	0	0	0	0	0
3	226	0	26	28	26	36	38	36	36	2	0	2	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2963	1227	248	234	232	252	266	252	252
1	1609	663	174	160	158	114	124	108	108	2246	165	74	75	72	744	972	72	72
2	3597	3	394	448	416	608	576	576	576	899	0	99	112	104	152	144	144	144
3	902	0	102	112	104	144	152	144	144	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	4754	642	291	301	285	448	478	324	324
2	0	0	0	0	0	0	0	0	0	1351	2	99	112	104	144	152	144	144
3	224	0	24	28	26	36	38	36	36	3	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	24	28	26	36	38	36	36	0	0	0	24	28	26	36	38	36	36
1	0	22	227	251	237	202	146	288	288	4754	295	31	8	19	556	752	0	0
2	0	0	50	56	52	72	76	72	72	1351	450	0	0	0	0	0	0	0
3	224	0	3	0	0	0	0	0	0	3	3	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (229 1351 333 0 2 0 1 225 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 1: (2 165 151 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 2: (27 147 38 0 0 0 1 25 1 1)
Cluster 3: (28 159 33 0 0 0 0 28)
Cluster 4: (26 150 38 0 0 0 0 26)
Cluster 5: (36 188 18 0 0 0 0 36 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 6: (38 182 19 0 0 0 0 38 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 7: (36 180 18 0 0 0 0 36)
Cluster 8: (36 180 18 0 0 0 0 36)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	112	106	107	109	110	103	101	0	0	0	0	0	0	0	0
12	0	0	0	9	5	2	3	0	24	0	0	0	0	0	0
2	0	0	0	4	0	0	2	0	0	28	0	0	0	0	0
8	0	5	0	0	1	3	2	0	0	0	26	0	0	0	0
0	72	84	78	0	106	108	108	0	0	0	0	36	0	0	0
0	96	112	104	152	0	144	144	0	0	0	0	0	38	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	36	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	36

code_seq_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	588	74	75	76	70	62	86	71	74
Number of PI	145	18	15	14	13	19	22	22	22
Number of DFF	216	29	22	8	32	27	35	31	32
Number of Combinational Nodes	443	56	60	62	57	43	64	49	52
Number of PO	223	26	28	11	33	27	35	31	32
Number of Edges	990	153	179	243	144	118	292	126	102
Number of Intra-Cluster Edges	594	69	100	169	61	32	87	36	40
Number of Inter-Cluster Input Edges	763	46	42	45	41	59	45	59	30
Number of Inter-Cluster Output Edges	763	38	37	29	42	27	160	31	32
Wirelength Approx	122060	14198	22761	32451	10380	8731	14789	8821	9929
Scaled Cost	0.66								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	1.6 ± 4	1.4 ± 1.3	1.8 ± 2.0	2.6 ± 2.9	1.4 ± 3.5	0.9 ± 0.7	2.8 ± 10	0.9 ± 0.7	0.9 ± 0.7
Avg. Comb. Fanout	2.2 ± 6	1.3 ± 1.1	2.0 ± 2.1	2.3 ± 1.6	0.9 ± 0.2	1 ± 0	7 ± 16	1 ± 0	1 ± 0
Avg. PI Fanout	2.7 ± 3.0	2.8 ± 1.0	3.7 ± 1.5	5 ± 5	4 ± 8	1.8 ± 0.3	2 ± 0	1.8 ± 0.3	1.9 ± 0.2
Avg. DFF Fanout	0.4 ± 0.5	0.6 ± 0.8	0.1 ± 0.3	0.2 ± 0.4	0.7 ± 0.6	0.2 ± 0.4	0.3 ± 0.4	0.2 ± 0.4	0.3 ± 0.4
Avg. Comb. Fanin	3.4 ± 0.7	3.4 ± 0.5	3.5 ± 0.7	3.3 ± 0.7	3 ± 1.0	3.5 ± 0.5	3.4 ± 0.5	3.5 ± 0.5	3.5 ± 0.5
Max Fanout	55	5	9	23	27	2	55	2	2

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	361	47	37	22	45	46	57	53	54	210	25	22	8	30	27	35	31	32
1	31	2	1	12	13	0	3	0	0	4	1	0	0	3	0	0	0	0
2	68	9	4	6	9	8	13	9	10	0	0	0	0	0	0	0	0	0
3	69	12	4	12	1	8	13	9	10	0	0	0	0	0	0	0	0	0
4	10	4	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	6	0	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	2	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	2	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	4	0	1	3	0	0	0	0	0	1	0	0	1	0	0	0	0	0
10	4	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
11	5	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	4	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	12	0	11	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	8	0	6	2	0	0	0	0	0	7	0	6	1	0	0	0	0	0
15	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	353	52	48	67	70	24	35	27	30
1	75	5	2	30	28	0	10	0	0	215	1	5	45	0	0	164	0	0
2	272	36	16	24	36	32	52	36	40	77	17	4	15	1	8	13	9	10
3	218	40	12	43	3	24	39	27	30	31	8	0	23	0	0	0	0	0
4	36	12	0	24	0	0	0	0	0	12	0	0	12	0	0	0	0	0
5	21	0	0	21	0	0	0	0	0	13	0	0	13	0	0	0	0	0
6	6	0	0	6	0	0	0	0	0	4	0	0	4	0	0	0	0	0
7	8	0	0	8	0	0	0	0	0	3	0	0	3	0	0	0	0	0
8	4	0	0	4	0	0	0	0	0	4	0	0	4	0	0	0	0	0
9	12	0	4	8	0	0	0	0	0	7	0	5	2	0	0	0	0	0
10	16	0	8	0	8	0	0	0	0	6	0	6	0	0	0	0	0	0
11	18	0	18	0	0	0	0	0	0	14	0	14	0	0	0	0	0	0
12	16	0	16	0	0	0	0	0	0	22	0	22	0	0	0	0	0	0
13	48	0	44	4	0	0	0	0	0	12	0	11	1	0	0	0	0	0
14	21	0	14	7	0	0	0	0	0	1	0	0	1	0	0	0	0	0
15	3	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	129	18	12	4	10	19	22	22	22	0	0	0	0	0	0	0	0	0
1	11	0	0	0	11	0	0	0	0	356	30	44	79	28	8	39	9	10
2	8	0	0	0	8	0	0	0	0	240	20	20	37	26	16	37	18	20
3	54	7	4	2	1	8	13	9	10	91	15	5	28	1	8	11	9	10
4	4	4	0	0	0	0	0	0	0	22	4	0	17	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	4	0	0	1	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	7	0	2	2	0	0	0	0	0
10	2	0	0	0	2	0	0	0	0	14	0	3	1	6	0	0	0	0
11	0	0	0	0	0	0	0	0	0	9	0	7	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	7	0	7	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	16	0	10	1	0	0	0	0	0
14	7	0	6	1	0	0	0	0	0	3	0	2	1	0	0	0	0	0
15	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	129	22	8	32	27	35	31	32	0	0	29	22	8	32	27	35	31	32
1	11	16	10	6	13	16	10	18	20	356	0	6	12	7	0	84	0	0
2	8	7	4	5	1	8	2	9	10	240	0	5	0	0	0	41	0	0
3	54	1	0	1	0	0	2	0	0	91	0	3	0	1	0	0	0	0
4	4	0	1	0	0	0	0	0	0	22	0	0	1	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
6	0	0	2	0	0	0	0	0	0	2	0	0	2	0	0	0	0	0
7	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0
8	0	0	3	0	0	0	0	0	0	4	0	0	3	0	0	0	0	0
9	0	0	2	1	0	0	0	0	0	7	1	1	1	0	0	0	0	0
10	2	0	4	0	0	0	0	0	0	14	4	0	0	0	0	0	0	0
11	0	0	2	0	0	0	0	0	0	9	0	0	0	2	0	0	0	0
12	0	0	0	0	0	0	0	0	0	7	0	0	0	0	0	0	0	0
13	0	0	5	0	0	0	0	0	0	16	4	0	1	0	0	0	0	0
14	7	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0
15	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (250 231 59 16 7 8 4 1 5 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2)
Cluster 1: (34 16 15 6 1 2)
Cluster 2: (28 22 15 0 2 3 0 1 3 1)
Cluster 3: (11 16 25 10 4 3 4 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (43 21 4 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (30 32 0)
Cluster 6: (35 48 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2)
Cluster 7: (35 36 0)
Cluster 8: (34 40 0)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	9	0	0	0	0	0	0	29	0	0	0	0	0	0	0
0	0	7	0	0	8	0	0	0	22	0	0	0	0	0	0
0	10	0	11	0	0	0	0	0	0	8	0	0	0	0	0
1	3	0	0	0	6	0	0	0	0	0	32	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	27	0	0	0
23	12	6	3	24	0	27	30	0	0	0	0	0	35	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	31	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32

dcu_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1590	199	197	199	200	197	198	201	199
Number of PI	340	49	72	63	41	49	56	6	4
Number of DFF	288	32	0	32	36	36	6	65	81
Number of Combinational Nodes	1250	150	125	136	159	148	142	195	195
Number of PO	232	0	51	18	39	54	39	31	0
Number of Edges	3592	610	446	524	543	507	658	611	556
Number of Intra-Cluster Edges	2697	404	331	268	328	310	437	327	292
Number of Inter-Cluster Input Edges	1758	32	115	124	117	77	109	206	83
Number of Inter-Cluster Output Edges	1758	174	0	132	98	120	112	78	181
Wirelength Approx	656561	87366	68227	66343	76698	81583	117054	81110	78180
Scaled Cost	0.87								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.2 ± 6	2.9 ± 9	1.6 ± 3.8	2.0 ± 5	2.1 ± 4	2.1 ± 6	2.7 ± 3.9	2.0 ± 6	2.3 ± 6
Avg. Comb. Fanout	1.3 ± 3.1	1.5 ± 1.2	1.5 ± 4	0.8 ± 0.3	1.3 ± 3.8	0.5 ± 0.4	1.7 ± 2.5	1.4 ± 5	1.2 ± 2.8
Avg. PI Fanout	5 ± 11	6 ± 18	1.9 ± 2.6	3.2 ± 9	3.1 ± 7	6 ± 11	5 ± 5	14 ± 22	34 ± 22
Avg. DFF Fanout	2.6 ± 0.9	4 ± 1	N/A	3.2 ± 0.8	3.5 ± 1.0	2 ± 0	2 ± 0	2 ± 0	2.3 ± 0.4
Avg. Comb. Fanin	3.4 ± 0.6	3.6 ± 0.4	3.3 ± 0.8	3.4 ± 0.7	3.3 ± 0.5	3.4 ± 0.5	3.5 ± 0.6	3.4 ± 0.5	3.2 ± 0.4
Max Fanout	128	128	32	64	44	54	32	64	64

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	628	81	72	95	77	85	62	71	85	8	0	0	4	3	1	0	0	0
1	417	22	29	60	49	88	51	68	50	61	0	19	0	5	30	7	0	0
2	294	64	32	30	32	23	50	31	32	22	0	0	0	0	22	0	0	0
3	104	32	0	14	16	1	10	31	0	59	0	0	14	5	1	8	31	0
4	103	0	32	0	22	0	17	0	32	38	0	0	0	22	0	16	0	0
5	44	0	32	0	4	0	8	0	0	44	0	32	0	4	0	8	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2326	400	139	310	256	371	309	213	328
1	1368	84	94	224	167	285	159	204	151	606	50	128	44	92	22	142	96	32
2	1112	224	128	104	112	92	200	124	128	208	32	32	14	16	1	50	31	32
3	351	128	0	28	43	4	24	124	0	120	64	0	0	22	0	34	0	0
4	365	0	128	0	75	0	66	0	96	44	0	32	0	4	0	8	0	0
5	108	0	64	0	12	0	32	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	192	0	0	16	20	36	6	65	49	2153	148	171	210	192	245	314	231	132
2	64	32	0	16	16	0	0	0	0	716	160	32	58	64	64	80	65	96
3	0	0	0	0	0	0	0	0	0	254	96	96	0	11	1	19	31	0
4	32	0	0	0	0	0	0	0	32	165	0	32	0	53	0	16	0	64
5	0	0	0	0	0	0	0	0	0	16	0	0	0	8	0	8	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	32	36	36	6	65	81	0	0	32	0	32	36	36	6	65	81
1	192	32	51	72	65	66	44	97	83	2153	110	0	100	62	79	99	9	51
2	64	0	32	16	16	5	0	28	0	716	32	0	0	0	5	7	4	49
3	0	0	0	0	0	0	0	0	0	254	0	0	0	0	0	0	0	0
4	32	0	0	0	0	0	0	0	0	165	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	16	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (508 480 316 108 90 25 0 0 21 5 4 2 0 1 0 0 0 6 0 1 0 0 1 0 0 0 0 0 0 0 2 0 12 0 0 0 1 0, 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (32 90 32 16 0 16 0 0 4 4 0 0 0 0 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (51 109 23 0 0 0 0 0 8 1 2 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 3: (46 92 30 14 14 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (68 47 50 14 7 9 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1)
Cluster 5: (89 28 55 0 21 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 6: (45 51 11 31 44 0 0 0 9 0 2 1 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 7: (96 31 65 1 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (81 32 50 32 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	32	46	32	0	0	0	32	32	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32	14	0	39	15	0	0	0	0	0	32	0	0	0	0	0
0	5	42	0	15	0	0	0	0	0	0	36	0	0	0	0
0	0	0	10	0	35	24	15	0	0	0	0	36	0	0	0
0	0	0	0	26	0	46	34	0	0	0	0	0	6	0	0
0	0	0	0	8	3	0	2	0	0	0	0	0	0	65	0
0	32	0	0	7	6	55	0	0	0	0	0	0	0	0	81

des

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1847	225	192	192	277	235	237	276	213
Number of PI	256	28	33	20	5	25	27	53	65
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1591	197	159	172	272	210	210	223	148
Number of PO	245	0	27	19	44	2	4	51	98
Number of Edges	5865	840	629	690	1149	892	871	1047	637
Number of Intra-Cluster Edges	4975	696	471	439	773	758	736	712	390
Number of Inter-Cluster Input Edges	1780	33	100	179	226	28	42	127	155
Number of Inter-Cluster Output Edges	1780	111	58	72	150	106	93	208	92
Wirelength Approx	2.49e+06	216371	275542	287123	558819	245843	226176	440763	239394
Scaled Cost	1.09								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.1 ± 12	3.5 ± 5	2.7 ± 5	2.6 ± 5	3.3 ± 21	3.6 ± 6	3.4 ± 5	3.3 ± 17	2.2 ± 13
Avg. Comb. Fanout	2.3 ± 12	2.3 ± 3.2	1.9 ± 3.4	1.6 ± 2.0	3.3 ± 21	2.3 ± 3.2	2.3 ± 3.0	2.5 ± 17	1.1 ± 9
Avg. PI Fanout	9 ± 14	12 ± 7	6 ± 7	11 ± 9	5 ± 0	15 ± 9	12 ± 8	7 ± 15	5 ± 19
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.6 ± 0.5	3.7 ± 0.6	3.5 ± 0.6	3.5 ± 0.6	3.6 ± 0.4	3.7 ± 0.5	3.7 ± 0.6	3.7 ± 0.4	3.6 ± 0.5
Max Fanout	226	25	28	34	226	29	32	225	154

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	256	28	33	20	5	25	27	53	65	0	0	0	0	0	0	0	0	0
1	224	57	26	30	1	52	51	3	4	1	0	0	0	0	0	0	0	1
2	633	81	77	49	3	94	91	136	102	93	0	11	3	0	0	0	23	56
3	440	31	35	50	182	32	36	56	18	30	0	12	1	0	0	0	0	17
4	133	16	10	24	42	21	19	0	1	1	0	0	0	0	0	0	0	1
5	97	12	7	16	44	9	9	0	0	56	0	0	12	44	0	0	0	0
6	64	0	4	3	0	2	4	28	23	64	0	4	3	0	2	4	28	23

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2186	337	214	228	25	373	335	358	316
1	791	204	92	108	4	184	180	8	11	1920	299	189	144	224	303	304	338	119
2	2408	305	287	173	9	361	346	521	406	1063	85	68	48	450	99	99	168	46
3	1690	111	120	197	728	121	133	224	56	467	42	34	58	182	45	49	56	1
4	446	61	35	79	126	76	67	0	2	165	28	16	25	42	28	26	0	0
5	332	48	28	52	132	36	36	0	0	64	16	8	8	0	16	16	0	0
6	198	0	9	9	0	8	16	86	70	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	3851	594	372	331	487	599	591	419	127
2	0	0	0	0	0	0	0	0	0	1405	75	73	73	266	122	113	236	198
3	0	0	0	0	0	0	0	0	0	406	14	19	27	20	20	21	0	35
4	0	0	0	0	0	0	0	0	0	62	1	0	4	0	10	0	0	18
5	0	0	0	0	0	0	0	0	0	91	12	7	4	0	5	7	28	0
6	0	0	0	0	0	0	0	0	0	50	0	0	0	0	2	4	29	12

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	21	46	105	54	19	22	34	30	3851	34	25	30	93	29	19	72	29
2	0	3	30	51	10	3	9	36	107	1405	18	4	15	52	18	15	90	37
3	0	0	13	17	162	0	1	56	1	406	59	28	27	5	59	59	0	13
4	0	9	10	3	0	3	4	0	0	62	0	1	0	0	0	0	18	10
5	0	0	1	3	0	2	4	1	17	91	0	0	0	0	0	0	27	1
6	0	0	0	0	0	1	2	0	0	50	0	0	0	0	0	0	1	2

Fanout Distribution
Circuit: (244 1096 168 50 43 63 11 14 11 15 13 10 12 10 13 16 7 5 6 1 3 6 4 3 2 3 3 0 1 2 0 0 1 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1)
Cluster 1: (0 137 26 10 9 4 2 2 2 4 4 1 3 1 3 4 4 1 1 0 1 2 3 0 0 1)
Cluster 2: (27 97 28 11 6 1 0 1 2 1 3 0 1 5 1 1 2 0 1 0 0 0 1 2 0 0 0 0 1)
Cluster 3: (19 123 11 8 3 5 1 3 3 3 0 3 0 0 2 2 1 0 0 1 0 2 0 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 4: (44 224 0 0 0 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 5: (2 148 24 9 6 1 6 4 3 2 4 2 4 2 1 4 0 0 3 0 1 2 0 1 2 1 1 0 0 2)
Cluster 6: (4 142 32 11 4 4 0 2 1 5 2 4 4 2 6 5 0 4 1 0 1 0 0 0 0 0 2 0 0 0 0 0 1)
Cluster 7: (51 169 1 0 15 36 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (97 56 46 1 0 7 2 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	18	23	34	0	0	24	12	0	0	0	0	0	0	0	0
13	0	5	19	9	0	10	2	0	0	0	0	0	0	0	0
9	2	0	22	0	21	16	2	0	0	0	0	0	0	0	0
3	10	121	0	6	3	5	2	0	0	0	0	0	0	0	0
0	8	0	48	0	8	26	16	0	0	0	0	0	0	0	0
0	0	0	48	7	0	25	13	0	0	0	0	0	0	0	0
8	14	18	49	4	7	0	108	0	0	0	0	0	0	0	0
0	48	12	6	2	3	21	0	0	0	0	0	0	0	0	0

diffeq

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1934	201	268	267	267	214	247	256	214
Number of PI	63	11	27	0	25	0	0	0	0
Number of DFF	377	38	49	58	73	49	38	45	27
Number of Combinational Nodes	1871	190	241	267	242	214	247	256	214
Number of PO	39	12	2	0	25	0	0	0	0
Number of Edges	5631	611	1248	1033	905	760	953	968	801
Number of Intra-Cluster Edges	3967	328	628	592	424	347	578	528	531
Number of Inter-Cluster Input Edges	3312	209	117	206	200	273	233	255	144
Number of Inter-Cluster Output Edges	3312	74	492	235	281	140	142	185	126
Wirelength Approx	1.79e+06	162271	257006	212282	198210	212134	272850	266134	212157
Scaled Cost	1.55								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.9 ± 14	2 ± 1.9	4 ± 32	3.0 ± 8	2.6 ± 15	2.2 ± 3.8	2.9 ± 8	2.7 ± 9	3.0 ± 5
Avg. Comb. Fanout	1.7 ± 3.8	1.4 ± 1.3	1.2 ± 2.5	2.1 ± 6	1.0 ± 0.0	1.5 ± 2.1	1.9 ± 2.1	1.6 ± 5	2.5 ± 5
Avg. PI Fanout	9 ± 62	1 ± 0	19 ± 93	N/A	1 ± 0	N/A	N/A	N/A	N/A
Avg. DFF Fanout	7 ± 18	5 ± 2.2	7 ± 21	7 ± 11	7 ± 29	5 ± 6	8 ± 19	8 ± 17	7 ± 3.3
Avg. Comb. Fanin	3.5 ± 0.6	3.2 ± 0.8	3.5 ± 0.6	3.4 ± 0.6	3.4 ± 0.7	3.5 ± 0.5	3.6 ± 0.5	3.5 ± 0.5	3.6 ± 0.5
Max Fanout	496	8	496	87	195	42	117	73	48

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	440	49	76	58	98	49	38	45	27	3	1	2	0	0	0	0	0	0
1	718	80	135	80	135	60	83	130	15	36	11	0	0	25	0	0	0	0
2	277	25	56	59	25	40	21	27	24	0	0	0	0	0	0	0	0	0
3	119	7	1	35	1	14	22	5	34	0	0	0	0	0	0	0	0	0
4	38	2	0	9	0	0	16	0	11	0	0	0	0	0	0	0	0	0
5	46	9	0	4	1	1	15	1	15	0	0	0	0	0	0	0	0	0
6	112	3	0	4	2	14	22	48	19	0	0	0	0	0	0	0	0	0
7	61	6	0	3	1	7	11	0	33	0	0	0	0	0	0	0	0	0
8	39	6	0	5	1	2	4	0	21	0	0	0	0	0	0	0	0	0
9	32	2	0	4	1	6	5	0	14	0	0	0	0	0	0	0	0	0
10	19	3	0	5	0	6	5	0	0	0	0	0	0	0	0	0	0	0
11	15	4	0	1	1	5	4	0	0	0	0	0	0	0	0	0	0	0
12	9	2	0	0	1	5	1	0	0	0	0	0	0	0	0	0	0	0
13	5	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0
14	4	2	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3090	183	888	385	535	226	310	374	189
1	2476	257	526	237	501	189	288	432	46	1122	82	169	214	99	101	138	170	149
2	895	54	158	216	50	136	83	108	90	332	21	1	106	0	29	84	35	56
3	466	28	3	140	3	56	87	20	129	150	12	0	39	0	23	28	5	43
4	140	8	0	36	0	0	58	0	38	95	16	0	14	0	0	31	0	34
5	175	34	0	15	3	4	58	4	57	157	14	0	6	0	7	27	73	30
6	433	10	0	16	5	54	84	192	72	112	7	0	5	0	7	26	0	67
7	229	23	0	12	3	28	39	0	124	87	13	0	6	0	7	16	0	45
8	137	23	0	18	3	8	15	0	70	39	5	0	5	0	7	6	0	16
9	111	8	0	15	2	23	18	0	45	24	4	0	5	0	10	5	0	0
10	71	11	0	17	0	24	19	0	0	20	4	0	2	0	8	6	0	0
11	55	16	0	3	2	20	14	0	0	13	4	0	0	0	7	2	0	0
12	33	7	0	0	3	20	3	0	0	8	2	0	0	0	6	0	0	0
13	20	4	0	0	0	16	0	0	0	5	2	0	0	0	3	0	0	0
14	13	5	0	0	0	4	0	0	4	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	11	0	0	0	0	0	0
1	53	2	6	1	37	1	2	4	0	3813	258	615	408	415	201	348	402	236
2	133	22	55	1	25	25	1	4	0	568	27	11	89	1	39	91	30	101
3	39	0	1	22	1	3	11	0	1	170	2	2	40	0	8	52	0	36
4	4	0	0	4	0	0	0	0	0	98	10	0	12	1	2	17	0	51
5	5	1	0	1	1	0	1	0	1	218	1	0	13	2	27	43	96	27
6	81	1	0	2	2	12	13	48	3	162	1	0	8	1	14	10	0	43
7	9	1	0	0	1	0	4	0	3	90	13	0	9	1	9	5	0	18
8	11	1	0	3	1	0	1	0	5	47	1	0	6	1	10	4	0	17
9	20	1	0	1	1	0	3	0	14	26	1	0	5	0	13	3	0	0
10	7	1	0	4	0	1	1	0	0	27	5	0	2	1	11	3	0	0
11	7	1	0	1	1	1	3	0	0	17	6	0	0	1	5	2	0	0
12	3	0	0	0	1	1	1	0	0	12	2	0	0	0	5	0	0	2
13	1	0	0	0	0	1	0	0	0	4	0	0	0	0	3	0	0	0
14	4	2	0	0	0	1	0	0	1	2	1	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	49	58	73	49	38	45	27	0	0	33	62	40	71	46	41	56	28
1	53	142	59	84	145	142	137	164	57	3813	26	306	153	195	49	73	103	25
2	133	0	0	45	1	58	31	14	30	568	15	73	13	13	11	11	26	17
3	39	0	0	3	0	9	0	0	18	170	0	1	10	0	5	13	0	1
4	4	1	0	1	1	0	0	1	1	98	0	1	2	0	1	0	0	1
5	5	2	0	0	1	1	1	1	3	218	0	5	3	0	0	1	0	0
6	81	2	0	0	1	13	13	48	8	162	0	9	3	0	25	1	0	47
7	9	2	0	0	1	4	1	0	27	90	0	28	3	0	3	0	0	1
8	11	2	0	0	0	4	2	0	0	47	0	1	2	1	0	2	0	2
9	20	2	0	0	0	1	1	0	0	26	0	1	2	0	0	0	0	1
10	7	2	0	0	0	1	2	0	0	27	0	1	2	1	0	0	0	1
11	7	1	0	0	1	1	0	0	0	17	0	1	1	0	0	0	0	1
12	3	2	0	0	0	1	0	0	0	12	0	1	1	0	0	0	0	1
13	1	1	0	0	0	0	0	0	0	4	0	1	0	0	0	0	0	0
14	4	1	0	0	0	0	0	0	0	2	0	1	0	0	0	0	0	0

Fanout Distribution
Circuit: (374 954 286 94 49 33 33 31 12 7 5 6 15 9 0 0 0 0 0 0 0 0 0 0 4 0 0 0 1 0 0 1 1 0 0 0 2 0, 0 0 0 1 1 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 1: (33 112 19 1 8 5 9 7 7)
Cluster 2: (60 154 43 1 3 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 1)
Cluster 3: (40 123 22 25 14 15 7 10 2 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (70 124 60 11 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 1)
Cluster 5: (46 89 41 14 6 3 3 3 0 0 0 1 5 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 6: (41 101 39 32 6 1 8 5 3 1 3 0 3 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (56 138 48 0 0 0 1 0 0 0 0 0 4 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 0 0 0 1)
Cluster 8: (28 113 14 10 12 9 4 6 0 2 2 5 2 2 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	22	16	0	1	0	0	2	33	0	0	0	0	0	0	0
71	0	57	110	49	43	57	43	1	49	11	0	1	0	0	0
15	11	0	32	27	54	42	14	4	0	36	0	0	0	0	0
74	25	53	0	11	42	4	1	0	0	0	71	0	0	0	0
0	1	6	0	0	26	46	15	0	0	0	0	46	0	0	0
0	0	1	9	43	0	36	12	0	0	0	2	1	38	0	0
0	0	0	0	57	15	0	57	0	0	11	0	1	0	44	0
0	0	0	0	47	8	43	0	0	0	0	0	0	0	1	27

display_chip

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	2417	289	294	296	295	300	276	362	305
Number of PI	33	8	0	0	1	13	6	2	3
Number of DFF	603	109	139	90	84	20	51	68	42
Number of Combinational Nodes	2384	281	294	296	294	287	270	360	302
Number of PO	134	32	51	4	6	4	1	31	5
Number of Edges	6515	789	724	984	827	1056	926	2171	976
Number of Intra-Cluster Edges	4524	379	343	465	445	725	537	894	708
Number of Inter-Cluster Input Edges	3929	316	251	312	217	222	296	113	183
Number of Inter-Cluster Output Edges	3929	94	130	182	165	108	93	1162	85
Wirelength Approx	1.91e+06	205376	190226	257854	186390	292585	256449	258536	268219
Scaled Cost	1.39								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.6 ± 26	1.6 ± 2.1	1.6 ± 5	2.1 ± 6	2.0 ± 7	2.7 ± 6	2.2 ± 2.4	6 ± 66	2.6 ± 3.4
Avg. Comb. Fanout	1.7 ± 4	1.3 ± 1.9	1.4 ± 7	1.1 ± 0.9	1.7 ± 8	2.1 ± 2.5	1.9 ± 1.8	1.6 ± 2.7	1.9 ± 3.1
Avg. PI Fanout	40 ± 215	4 ± 0	N/A	N/A	2 ± 0	1 ± 0	1 ± 0	628 ± 627	3.6 ± 3.0
Avg. DFF Fanout	3.5 ± 6	1.9 ± 2.2	1.7 ± 0.9	5 ± 9	2.9 ± 0.9	13 ± 17	4 ± 3.7	5 ± 5	6 ± 2.4
Avg. Comb. Fanin	3.3 ± 0.8	3.2 ± 0.8	3.2 ± 0.9	3.3 ± 0.8	3.0 ± 0.9	3.3 ± 0.8	3.4 ± 0.7	3.3 ± 0.8	3.4 ± 0.7
Max Fanout	1255	19	65	67	88	72	19	1255	40

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	636	117	139	90	85	33	57	70	45	0	0	0	0	0	0	0	0	0
1	557	63	53	107	60	79	56	93	46	132	32	51	4	6	4	1	30	4
2	282	28	102	8	12	41	29	40	22	1	0	0	0	0	0	0	1	0
3	144	7	0	2	0	40	26	45	24	1	0	0	0	0	0	0	0	1
4	165	18	0	2	1	25	15	58	46	0	0	0	0	0	0	0	0	0
5	205	24	0	39	49	21	9	33	30	0	0	0	0	0	0	0	0	0
6	159	5	0	25	47	18	6	21	37	0	0	0	0	0	0	0	0	0
7	142	27	0	23	41	9	14	1	27	0	0	0	0	0	0	0	0	0
8	41	0	0	0	0	7	17	1	16	0	0	0	0	0	0	0	0	0
9	34	0	0	0	0	7	16	0	11	0	0	0	0	0	0	0	0	0
10	16	0	0	0	0	5	10	0	1	0	0	0	0	0	0	0	0	0
11	16	0	0	0	0	7	9	0	0	0	0	0	0	0	0	0	0	0
12	12	0	0	0	0	6	6	0	0	0	0	0	0	0	0	0	0	0
13	6	0	0	0	0	2	4	0	0	0	0	0	0	0	0	0	0	0
14	2	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3475	248	241	413	248	268	213	1565	279
1	1540	166	110	362	155	213	161	241	132	627	19	130	34	14	164	89	101	76
2	1012	109	394	23	24	138	100	146	78	318	8	0	6	12	87	47	99	59
3	527	27	0	7	0	146	97	169	81	364	39	0	0	0	88	43	117	77
4	587	51	0	7	4	97	57	208	163	374	34	0	16	71	56	21	81	95
5	752	89	0	148	189	71	30	113	112	334	6	0	23	129	51	37	23	65
6	601	17	0	100	188	66	20	82	128	219	28	0	23	41	35	40	1	51
7	411	97	0	46	82	34	55	4	93	66	0	0	0	0	14	20	1	31
8	153	0	0	0	0	27	61	2	63	51	0	0	0	0	12	23	0	16
9	125	0	0	0	0	27	61	0	37	26	0	0	0	0	10	13	0	3
10	64	0	0	0	0	20	40	0	4	24	0	0	0	0	11	13	0	0
11	64	0	0	0	0	28	36	0	0	20	0	0	0	0	10	10	0	0
12	45	0	0	0	0	22	23	0	0	12	0	0	0	0	6	6	0	0
13	23	0	0	0	0	7	16	0	0	2	0	0	0	0	1	1	0	0
14	8	0	0	0	0	0	8	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	25	0	1	0	2	0
1	198	16	0	87	41	19	17	14	4	3237	204	153	315	247	463	302	534	399
2	136	26	102	2	0	0	6	0	0	997	74	190	29	41	122	71	147	101
3	13	0	0	2	0	0	4	6	1	337	19	0	3	0	47	37	78	63
4	20	2	0	0	0	0	4	12	2	328	19	0	12	13	29	24	90	61
5	60	20	0	16	7	0	1	15	1	413	17	0	60	75	26	28	14	28
6	32	0	0	2	6	0	1	20	3	328	5	0	46	69	13	13	29	30
7	109	27	0	23	41	0	1	0	17	128	41	0	0	0	4	16	1	13
8	8	0	0	0	0	0	3	1	4	59	0	0	0	0	12	21	1	8
9	15	0	0	0	0	0	7	0	8	38	0	0	0	0	4	10	0	5
10	4	0	0	0	0	0	3	0	1	27	0	0	0	0	4	8	0	0
11	2	0	0	0	0	0	2	0	0	10	0	0	0	0	1	3	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	4	0	0	0	0	1	3	0	0	6	0	0	0	0	0	2	0	0
14	2	0	0	0	0	0	2	0	0	4	0	0	0	0	0	2	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	139	90	84	20	51	68	42	0	0	91	102	132	95	20	54	68	41
1	198	90	59	154	71	57	95	38	56	3237	2	26	24	68	53	13	414	20
2	136	28	102	4	1	28	39	3	17	997	0	1	0	0	16	1	202	2
3	13	6	0	2	0	31	33	1	17	337	0	1	0	0	11	0	77	1
4	20	9	0	2	2	5	13	9	40	328	0	0	0	2	3	6	63	6
5	60	15	0	41	63	13	5	13	15	413	1	0	13	0	0	0	136	15
6	32	3	0	25	60	12	5	7	11	328	0	0	13	0	0	7	103	0
7	109	26	0	0	0	7	5	0	15	128	0	0	0	0	1	3	49	0
8	8	0	0	0	0	5	9	0	3	59	0	0	0	0	1	3	13	0
9	15	0	0	0	0	2	9	0	8	38	0	0	0	0	1	0	18	0
10	4	0	0	0	0	8	6	0	1	27	0	0	0	0	1	5	9	0
11	2	0	0	0	0	2	4	0	0	10	0	0	0	0	1	1	4	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	4	0	0	0	0	1	3	0	0	6	0	0	0	0	0	0	4	0
14	2	0	0	0	0	0	2	0	0	4	0	0	0	0	0	0	2	0

Fanout Distribution

Circuit: (723 988 136 238 116 48 43 36 30 13 12 6 0 3 1 2 1 1 1 3 1 1 0 1 0 0 1 0 1 0 0 0 0 0 1 0,
0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 2 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 1: (121 103 15 22 11 4 5 2 1 2 0 0 0 0 0 2 0 0 0 1)

Cluster 2: (153 88 0 51 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)

Cluster 3: (136 61 18 50 23 2 1 0 2 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)

Cluster 4: (101 119 7 41 25 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 5: (22 151 39 28 20 11 9 4 10 0 1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0,
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 6: (55 128 21 16 18 9 6 11 2 2 4 2 0 1 0 0 0 0 0 1)

Cluster 7: (92 181 15 14 9 11 10 8 6 1 4 3 0 1 0 0 1 1 0 0 1 0 0 1 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 8: (43 157 21 16 10 11 12 11 9 8 2 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 1)

Inter-Cluster Connectivity Matricies

Comb								Latched							
0	0	0	1	0	0	1	1	81	0	2	6	0	0	2	0
26	0	0	0	0	0	2	0	14	88	0	0	0	0	0	0
0	0	0	47	0	0	3	0	0	23	83	25	0	0	1	0
1	0	52	0	0	0	17	0	13	28	0	53	0	0	0	1
0	0	0	0	0	85	3	0	0	0	0	0	19	1	0	0
0	0	0	0	17	0	22	0	0	0	2	0	1	50	0	1
143	161	164	148	153	143	0	182	1	0	0	0	0	0	65	2
7	0	12	1	1	0	23	0	0	0	3	0	0	0	0	38

dsip

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1814	211	272	228	233	213	213	232	212
Number of PI	228	12	3	20	19	30	31	71	42
Number of DFF	224	35	31	35	36	29	32	1	25
Number of Combinational Nodes	1586	199	269	208	214	183	182	161	170
Number of PO	193	33	26	29	31	25	27	1	21
Number of Edges	5664	770	2842	793	801	707	675	1259	658
Number of Intra-Cluster Edges	2788	262	765	290	300	271	266	383	251
Number of Inter-Cluster Input Edges	5717	422	219	438	441	377	335	280	329
Number of Inter-Cluster Output Edges	5717	86	1858	65	60	59	74	596	78
Wirelength Approx	2.88e+06	346087	591678	362205	376942	302865	295090	315686	292071
Scaled Cost	3.17								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.1 ± 34	1.6 ± 1.4	10 ± 82	1.5 ± 1.0	1.5 ± 1.0	1.5 ± 1.0	1.5 ± 1.0	4 ± 33	1.5 ± 0.9
Avg. Comb. Fanout	1.8 ± 18	0.9 ± 0.2	2.8 ± 29	1 ± 0	1 ± 0	1 ± 0	1 ± 0	5 ± 39	1 ± 0
Avg. PI Fanout	10 ± 84	3.7 ± 2.7	605 ± 426	2.1 ± 0.4	2 ± 0	2 ± 0	2 ± 0	2.0 ± 0.2	2 ± 0
Avg. DFF Fanout	4 ± 0	4 ± 0	4 ± 0	4 ± 0	4 ± 0	4 ± 0	4 ± 0	4 ± 0	4 ± 0
Avg. Comb. Fanin	3.9 ± 0.0	3.9 ± 0.1	3.9 ± 0.1	4 ± 0	4 ± 0	4 ± 0	4 ± 0	3.9 ± 0.1	4 ± 0
Max Fanout	907	9	907	4	4	4	4	449	4

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	452	47	34	55	55	59	63	72	67	188	29	25	29	31	25	27	1	21
1	236	14	5	19	19	30	31	78	40	2	1	1	0	0	0	0	0	0
2	900	113	203	119	123	94	87	81	80	1	1	0	0	0	0	0	0	0
3	226	37	30	35	36	30	32	1	25	2	2	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3185	185	1938	182	182	176	190	148	184
1	938	55	17	76	76	120	124	310	160	1356	16	452	19	19	30	31	749	40
2	3599	451	812	476	492	376	348	324	320	899	112	203	119	123	94	87	81	80
3	903	147	120	140	144	120	128	4	100	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	3192	150	270	173	177	180	179	381	182
2	0	0	0	0	0	0	0	0	0	2245	111	495	117	123	91	87	2	69
3	224	35	30	35	36	30	32	1	25	3	1	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	31	35	36	29	32	1	25	0	0	35	30	35	36	30	32	1	25
1	0	188	70	202	210	214	222	172	222	3192	17	853	7	3	4	1	593	22
2	0	201	114	200	202	131	112	83	107	2245	34	973	23	21	25	41	2	31
3	224	2	0	0	0	0	0	0	0	3	0	2	0	0	0	0	0	0

Fanout Distribution
Circuit: (229 1128 221 1 227 0 0 0 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 1: (39 123 9 1 36 0 0 0 2 1)
Cluster 2: (31 206 1 0 31 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 3: (35 138 19 0 36)
Cluster 4: (36 142 19 0 36)
Cluster 5: (30 124 30 0 29)
Cluster 6: (32 118 31 0 32)
Cluster 7: (1 157 70 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 8: (25 120 42 0 25)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	16	0	4	0	0	27	4	35	0	0	0	0	0	0	0
300	0	310	309	254	235	187	233	0	30	0	0	0	0	0	0
0	9	0	3	0	0	18	0	0	0	35	0	0	0	0	0
1	5	2	0	0	0	16	0	0	0	0	36	0	0	0	0
0	24	0	0	0	3	2	0	0	1	0	0	29	0	0	0
0	37	0	0	3	0	0	2	0	0	0	0	0	32	0	0
83	60	90	92	88	92	0	90	0	0	0	0	0	0	1	0
7	33	0	4	0	4	5	0	0	0	0	0	0	0	0	25

elliptic

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	4854	621	591	593	727	589	590	552	591
Number of PI	130	16	0	48	49	1	0	0	16
Number of DFF	1122	135	96	148	178	146	155	131	133
Number of Combinational Nodes	4724	605	591	545	678	588	590	552	575
Number of PO	114	0	0	48	48	2	0	0	16
Number of Edges	13640	2010	2335	1896	3565	2124	2138	1924	2029
Number of Intra-Cluster Edges	9124	1121	1157	1019	1488	1129	1174	963	1073
Number of Inter-Cluster Input Edges	8897	586	764	496	396	502	566	595	476
Number of Inter-Cluster Output Edges	8897	303	414	381	1681	493	398	366	480
Wirelength Approx	9.24e+06	1.27e+06	1.25e+06	929783	1.35e+06	1.01e+06	1.23e+06	1.05e+06	1.12e+06
Scaled Cost	1.56								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.8 ± 24	2.2 ± 16	2.6 ± 7	2.3 ± 13	4 ± 55	2.7 ± 10	2.6 ± 8	2.4 ± 7	2.6 ± 10
Avg. Comb. Fanout	1.6 ± 6	1.7 ± 12	1.8 ± 3.4	1.1 ± 1.3	1.5 ± 3.4	1.6 ± 6	1.9 ± 7	1.2 ± 1.1	1.5 ± 2.7
Avg. PI Fanout	12 ± 128	1 ± 0	N/A	1 ± 0	31 ± 208	5 ± 0	N/A	N/A	1 ± 0
Avg. DFF Fanout	6 ± 19	4 ± 25	7 ± 16	6 ± 26	5 ± 19	6 ± 15	5 ± 9	6 ± 15	7 ± 19
Avg. Comb. Fanin	3.4 ± 0.6	3.4 ± 0.8	3.5 ± 0.6	3.3 ± 0.7	3.4 ± 0.7	3.3 ± 0.6	3.6 ± 0.5	3.3 ± 0.5	3.5 ± 0.6
Max Fanout	1470	291	83	195	1470	128	140	87	147

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1252	151	96	196	227	147	155	131	149	2	0	0	0	0	2	0	0	0
1	1644	20	192	301	301	188	162	233	247	112	0	0	48	48	0	0	0	16
2	809	314	93	48	49	110	35	99	61	0	0	0	0	0	0	0	0	0
3	253	130	45	0	2	26	29	8	13	0	0	0	0	0	0	0	0	0
4	53	0	26	0	5	8	3	2	9	0	0	0	0	0	0	0	0	0
5	66	1	5	6	31	9	5	4	5	0	0	0	0	0	0	0	0	0
6	199	1	18	3	9	15	106	22	25	0	0	0	0	0	0	0	0	0
7	102	0	9	6	6	28	27	7	19	0	0	0	0	0	0	0	0	0
8	80	1	6	3	7	23	11	7	22	0	0	0	0	0	0	0	0	0
9	60	0	6	6	26	5	6	5	6	0	0	0	0	0	0	0	0	0
10	59	1	17	3	12	6	7	6	7	0	0	0	0	0	0	0	0	0
11	59	0	9	6	25	4	6	4	5	0	0	0	0	0	0	0	0	0
12	59	1	19	3	11	5	7	6	7	0	0	0	0	0	0	0	0	0
13	59	0	24	6	6	5	7	7	4	0	0	0	0	0	0	0	0	0
14	58	1	19	3	7	6	7	7	8	0	0	0	0	0	0	0	0	0
15	31	0	7	3	3	4	6	4	4	0	0	0	0	0	0	0	0	0
16	5	0	0	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0
17	4	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0
18	2	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	7858	581	634	957	2381	883	720	816	886
1	5741	67	642	1097	1095	631	588	759	862	2546	391	280	295	329	361	324	268	298
2	2848	1256	372	96	100	366	104	345	209	696	313	118	0	1	76	31	93	64
3	684	264	159	0	7	65	113	32	44	202	4	75	0	4	32	58	8	21
4	208	0	104	0	20	28	12	8	36	318	0	113	0	132	13	5	4	51
5	251	4	20	21	122	30	20	15	19	210	0	34	0	20	8	147	1	0
6	746	4	60	9	30	48	422	82	91	149	0	26	0	0	63	32	0	28
7	373	0	34	18	20	110	87	28	76	124	0	1	0	1	37	36	3	46
8	270	4	18	9	24	81	41	20	73	62	0	0	0	28	1	7	0	26
9	227	0	24	18	100	19	24	20	22	61	0	8	0	46	0	7	0	0
10	190	4	56	9	40	16	26	18	21	61	0	26	0	28	0	7	0	0
11	224	0	34	18	96	16	24	16	20	61	0	34	0	20	0	7	0	0
12	190	4	66	9	32	14	26	18	21	61	0	54	0	0	0	7	0	0
13	224	0	94	18	20	20	28	28	16	60	0	46	0	1	2	8	3	0
14	186	4	64	9	24	16	26	20	23	33	0	26	0	0	0	7	0	0
15	112	0	26	6	8	16	24	16	16	7	0	0	0	0	0	7	0	0
16	20	0	0	0	0	0	20	0	0	6	0	0	0	0	0	6	0	0
17	16	0	0	0	0	0	16	0	0	3	0	0	0	0	0	3	0	0
18	8	0	0	0	0	0	8	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	157	0	7	52	52	7	5	10	24	9007	654	783	938	1200	839	587	763	809
2	253	1	0	48	48	69	17	51	19	1425	455	131	0	0	93	72	52	58
3	128	128	0	0	0	0	0	0	0	82	0	0	0	0	16	27	0	19
4	0	0	0	0	0	0	0	0	0	134	1	3	12	18	38	13	3	21
5	32	1	3	6	11	2	1	3	5	438	2	16	6	67	22	210	41	44
6	175	1	11	3	9	7	98	22	24	287	1	28	9	18	20	121	10	12
7	38	0	8	6	5	6	4	4	5	203	1	23	6	33	21	29	14	20
8	67	1	6	3	6	22	7	7	15	150	1	25	9	18	21	17	8	14
9	34	0	5	6	5	5	2	5	6	163	1	39	6	34	12	15	14	15
10	47	1	10	3	11	6	3	6	7	126	1	25	9	24	6	14	7	9
11	33	0	7	6	5	4	2	4	5	132	1	20	6	35	11	16	13	15
12	47	1	11	3	11	5	3	6	7	110	1	19	9	16	7	13	10	7
13	33	0	9	6	5	3	2	4	4	129	1	22	6	12	11	13	14	16
14	47	1	12	3	7	6	3	7	8	78	1	13	3	11	6	12	7	7
15	27	0	7	3	3	4	2	4	4	45	0	10	0	2	6	6	7	7
16	1	0	0	0	0	0	1	0	0	6	0	0	0	0	0	6	0	0
17	1	0	0	0	0	0	1	0	0	3	0	0	0	0	0	3	0	0
18	2	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	96	148	178	146	155	131	133	0	0	135	96	148	178	146	153	133	133
1	157	175	463	306	187	232	340	359	372	9007	142	247	217	915	273	192	199	249
2	253	309	59	0	0	71	47	50	28	1425	16	20	1	398	64	5	2	58
3	128	0	1	3	3	6	4	3	0	82	0	0	0	0	1	4	2	13
4	0	0	0	0	20	3	2	0	0	134	1	8	0	0	2	4	5	5
5	32	1	10	3	3	3	2	4	4	438	0	2	3	20	0	1	1	3
6	175	1	6	0	3	8	3	19	28	287	1	7	0	26	1	32	1	0
7	38	0	4	3	0	5	17	4	23	203	1	3	3	43	1	1	3	1
8	67	1	3	0	15	2	5	3	8	150	1	5	0	21	2	1	4	3
9	34	0	7	3	4	4	3	5	1	163	1	16	3	2	0	1	2	2
10	47	1	5	0	15	2	2	3	3	126	1	5	0	15	2	1	4	3
11	33	0	9	0	0	2	2	1	1	132	1	2	3	3	0	1	3	2
12	47	1	17	0	0	2	2	3	3	110	1	0	0	21	0	0	1	5
13	33	0	23	0	0	3	3	4	1	129	1	1	3	22	1	1	3	2
14	47	1	7	0	0	2	2	3	3	78	0	0	0	17	0	0	1	0
15	27	0	2	0	0	2	1	1	1	45	1	2	0	0	0	1	2	1
16	1	0	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0
17	1	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0
18	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (1120 2264 1095 178 11 10 6 13 10 1 2 22 2 3 10 0 26 10 1 0 6 0 0 0 1 0 11 0 5 0 0 0 0 0, 5 2 0 0 0 0 0 0 0 0 0 0 0 0 0 3 2 0 0 1 7 0 0 0 0 0 0 0 0 0 0 0 0 0 6 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1, 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (135 340 130 6 0 0 0 0 0 0 0 1 0 0 0 0 7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 2: (96 304 138 17 0 0 0 6 6 0 0 5 0 0 0 0 3 0 0 0 4 0 0 0 0 0 4 0 1 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (147 295 128 16 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0, 0 0 0 0 0 1)
Cluster 4: (178 353 145 31 0 0 0 0 0 0 0 5 0 0 0 0 2 0 0 0 0 0 0 0 0 0 5 0 3 0 0 0 0 0 0 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (145 230 143 31 2 7 6 6 2 1 1 2 0 1 0 0 1 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (153 213 162 15 9 3 0 0 0 0 1 3 2 2 10 0 6 6 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 7: (133 251 123 30 0 0 0 0 0 0 0 3 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (133 278 126 32 0 0 0 1 2 0 0 3 0 0 0 0 3 1 0 0 2 0 0 0 0 0 2 0 1 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	123	0	8	6	0	0	31	135	0	0	0	0	0	0	0
31	0	27	76	57	13	34	80	0	96	0	0	0	0	0	0
50	47	0	53	5	2	39	37	0	0	148	0	0	0	0	0
337	189	263	0	155	171	185	203	0	0	0	178	0	0	0	0
17	55	0	10	0	142	70	53	0	0	0	0	146	0	0	0
2	27	0	39	62	0	49	66	0	0	0	0	0	153	0	0
11	41	16	27	33	99	0	6	0	0	0	0	0	2	131	0
42	134	12	37	29	8	85	0	0	0	0	0	0	0	0	133

ex5p

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1072	129	130	129	130	130	160	134	130
Number of PI	8	3	0	0	0	0	2	0	3
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1064	126	130	129	130	130	158	134	127
Number of PO	63	14	10	12	4	3	8	3	9
Number of Edges	3939	530	585	529	595	730	1345	637	727
Number of Intra-Cluster Edges	2200	225	245	221	245	240	469	285	270
Number of Inter-Cluster Input Edges	3478	238	231	259	229	238	129	211	204
Number of Inter-Cluster Output Edges	3478	67	109	49	121	252	747	141	253
Wirelength Approx	1.12e+06	122214	130915	116356	121833	139817	203941	140234	147057
Scaled Cost	3.63								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.6 ± 15	2.2 ± 2.9	2.7 ± 6	2.0 ± 1.8	2.8 ± 6	3.7 ± 10	8 ± 36	3.1 ± 6	4 ± 10
Avg. Comb. Fanout	3.0 ± 7	1.9 ± 2.1	2.7 ± 6	2.0 ± 1.8	2.8 ± 6	3.7 ± 10	3.6 ± 9	3.1 ± 6	3.8 ± 10
Avg. PI Fanout	90 ± 134	15 ± 0	N/A	N/A	N/A	N/A	323 ± 0	N/A	10 ± 0
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.7 ± 0.5	3.6 ± 0.5	3.6 ± 0.5	3.7 ± 0.5	3.6 ± 0.5	3.6 ± 0.5	3.7 ± 0.4	3.7 ± 0.5	3.7 ± 0.5
Max Fanout	323	17	61	9	69	74	323	50	67

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	8	3	0	0	0	0	2	0	3	0	0	0	0	0	0	0	0	0
1	24	0	1	0	2	6	5	2	8	0	0	0	0	0	0	0	0	0
2	357	13	33	11	32	60	98	48	62	23	0	1	1	3	2	8	3	5
3	317	28	41	31	50	44	39	47	37	5	0	2	0	0	1	0	0	2
4	214	32	35	38	35	16	13	28	17	2	0	0	0	0	0	0	0	2
5	106	31	11	36	10	4	3	8	3	1	0	1	0	0	0	0	0	0
6	28	12	5	10	0	0	0	1	0	14	4	2	8	0	0	0	0	0
7	18	10	4	3	1	0	0	0	0	18	10	4	3	1	0	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	721	45	0	0	0	0	646	0	30
1	65	0	3	0	5	16	14	6	21	971	0	61	0	76	235	220	94	285
2	1423	52	132	44	127	239	390	192	247	1123	59	135	39	140	177	268	183	122
3	1089	95	139	108	171	151	133	164	128	666	73	100	116	93	60	63	101	60
4	793	117	129	140	131	58	51	101	66	323	62	45	76	47	16	16	38	23
5	393	116	39	137	36	14	10	29	12	117	41	10	37	10	4	3	9	3
6	110	47	20	39	0	0	0	4	0	18	12	3	2	0	0	0	1	0
7	66	36	14	12	4	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	2707	138	185	184	206	220	229	247	221
2	0	0	0	0	0	0	0	0	0	1168	60	54	34	38	20	230	37	49
3	0	0	0	0	0	0	0	0	0	62	26	6	3	1	0	10	1	0
4	0	0	0	0	0	0	0	0	0	2	1	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	168	127	181	134	124	124	100	119	2707	57	83	38	99	212	251	122	215
2	0	63	102	73	93	114	5	111	85	1168	10	23	9	22	40	490	18	34
3	0	7	2	4	2	0	0	0	0	62	0	3	2	0	0	5	1	4
4	0	0	0	1	0	0	0	0	0	2	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (45 543 144 120 64 53 33 20 7 9 5 0 1 1 1 5 0 1 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1, 2 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 2 0 0 1 1 1 1 0 2 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 1: (14 66 14 13 4 8 3 2 0 1 0 0 0 0 0 3 0 1)
Cluster 2: (9 66 13 14 10 4 3 4 2 3 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (11 68 9 13 11 5 10 1 0 1)
Cluster 4: (1 71 18 10 9 13 1 3 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (1 69 19 15 8 8 2 2 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0, 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 6: (3 67 31 30 9 3 4 4 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 7: (0 62 20 17 10 11 6 3 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1 0 0 0 0 0 1)
Cluster 8: (6 74 20 8 3 1 4 1 3 0 3 0 0 0 0 1 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	12	15	9	8	8	11	4	0	0	0	0	0	0	0	0
35	0	27	19	7	8	4	9	0	0	0	0	0	0	0	0
16	9	0	12	5	4	1	2	0	0	0	0	0	0	0	0
24	30	31	0	9	12	6	9	0	0	0	0	0	0	0	0
41	27	38	38	0	44	30	34	0	0	0	0	0	0	0	0
73	99	81	107	156	0	120	111	0	0	0	0	0	0	0	0
29	14	32	12	9	10	0	35	0	0	0	0	0	0	0	0
20	40	35	32	44	43	39	0	0	0	0	0	0	0	0	0

ex1010

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	4608	541	560	542	541	691	541	508	684
Number of PI	10	0	0	0	0	7	0	3	0
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	4598	541	560	542	541	684	541	505	684
Number of PO	10	2	0	2	1	0	2	3	0
Number of Edges	16068	1984	2024	1986	1972	5512	1968	1877	3271
Number of Intra-Cluster Edges	11542	1260	1370	1301	1278	2146	1264	1184	1739
Number of Inter-Cluster Input Edges	9052	627	578	590	595	302	609	572	653
Number of Inter-Cluster Output Edges	9052	97	76	95	99	3064	95	121	879
Wirelength Approx	1.39e+07	1.51e+06	1.57e+06	1.60e+06	1.47e+06	2.44e+06	1.65e+06	1.45e+06	2.21e+06
Scaled Cost	2.11								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.4 ± 16	2.5 ± 8	2.5 ± 7	2.5 ± 7	2.5 ± 7	8 ± 33	2.5 ± 7	2.5 ± 8	3.8 ± 18
Avg. Comb. Fanout	3.4 ± 15	2.5 ± 8	2.5 ± 7	2.5 ± 7	2.5 ± 7	7 ± 32	2.5 ± 7	2.4 ± 8	3.8 ± 18
Avg. PI Fanout	43 ± 87	N/A	N/A	N/A	N/A	54 ± 101	N/A	16 ± 0	N/A
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.4 ± 0.5	3.4 ± 0.5	3.4 ± 0.5	3.4 ± 0.5	3.4 ± 0.5	3.5 ± 0.5	3.4 ± 0.5	3.4 ± 0.5	3.4 ± 0.5
Max Fanout	302	140	137	136	132	302	135	144	259

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	10	0	0	0	0	7	0	3	0	0	0	0	0	0	0	0	0	0
1	41	2	2	2	2	21	2	2	8	0	0	0	0	0	0	0	0	0
2	1864	208	209	197	199	376	198	189	288	0	0	0	0	0	0	0	0	0
3	1748	211	234	219	223	196	213	197	255	0	0	0	0	0	0	0	0	0
4	605	76	74	72	78	65	81	70	89	0	0	0	0	0	0	0	0	0
5	220	27	30	33	27	19	30	25	29	0	0	0	0	0	0	0	0	0
6	76	10	9	10	10	5	9	12	11	0	0	0	0	0	0	0	0	0
7	34	5	2	7	1	2	6	7	4	0	0	0	0	0	0	0	0	0
8	10	2	0	2	1	0	2	3	0	10	2	0	2	1	0	2	3	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	425	0	0	0	0	377	0	48	0
1	140	7	7	7	7	69	7	7	29	6378	250	239	228	232	3664	239	246	1280
2	6441	709	705	662	668	1390	663	646	998	6447	754	846	802	795	878	756	687	929
3	5856	708	790	744	749	639	720	660	846	1883	235	246	244	234	200	238	210	276
4	2316	292	288	280	296	251	302	261	346	605	76	74	72	78	65	81	70	89
5	854	105	114	125	107	72	118	99	114	220	27	30	33	27	19	30	25	29
6	294	40	36	39	38	19	33	45	44	76	10	9	10	10	5	9	12	11
7	130	18	8	28	4	8	22	27	15	34	5	2	7	1	2	6	7	4
8	37	8	0	6	4	0	8	11	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	14208	1081	1185	1125	1124	1911	1100	1030	1574
2	0	0	0	0	0	0	0	0	0	1829	175	183	172	152	231	164	152	156
3	0	0	0	0	0	0	0	0	0	31	4	2	4	2	4	0	2	9
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	554	525	529	548	289	537	494	602	14208	88	69	80	89	2715	86	118	833
2	0	73	53	60	47	13	70	78	50	1829	9	7	15	10	346	9	2	46
3	0	0	0	1	0	0	2	0	1	31	0	0	0	0	3	0	1	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution

Circuit: (10 3215 205 291 249 189 155 113 89 32 13 0 0 0 0 0 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 3 0 1 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 1,
1 2 2 0 2 2 0 0 0 1 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 0 0,
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0,
1 0 0 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0 2 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 1: (2 375 28 30 34 27 12 11 15 4 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 1)

Cluster 2: (0 386 28 35 20 22 30 16 13 6 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 3: (2 381 22 19 24 26 28 19 13 5 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 4: (1 375 25 31 37 24 7 11 17 6 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 5: (0 504 25 48 30 22 14 13 9 1 1 0 0 0 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0,
2 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 1 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0,
0 0 0 1 0 0 0 0 0 1 0 1 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 6: (2 368 21 45 28 24 26 15 8 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 7: (3 351 26 33 29 17 19 14 5 4 2 0 0 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 1)

Cluster 8: (0 475 30 50 47 27 19 14 9 4 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0,
0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	24	3	41	22	2	3	2	0	0	0	0	0	0	0	0
35	0	3	3	27	3	5	0	0	0	0	0	0	0	0	0
2	0	0	34	15	36	4	4	0	0	0	0	0	0	0	0
27	2	31	0	24	2	6	7	0	0	0	0	0	0	0	0
426	419	388	403	0	435	413	580	0	0	0	0	0	0	0	0
1	1	34	0	47	0	9	3	0	0	0	0	0	0	0	0
7	7	10	6	25	9	0	57	0	0	0	0	0	0	0	0
129	125	121	108	142	122	132	0	0	0	0	0	0	0	0	0

ex_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	3925	476	476	496	530	463	510	475	499
Number of PI	805	48	135	11	75	151	201	43	141
Number of DFF	363	187	76	32	0	35	0	33	0
Number of Combinational Nodes	3120	428	341	485	455	312	309	432	358
Number of PO	358	81	12	1	32	6	125	68	33
Number of Edges	10323	1236	1171	1783	1625	1222	1197	2187	1425
Number of Intra-Cluster Edges	8615	764	961	1375	1233	976	906	1297	1102
Number of Inter-Cluster Input Edges	3231	134	56	232	351	62	248	212	227
Number of Inter-Cluster Output Edges	3231	337	154	176	41	184	43	678	96
Wirelength Approx	5.71e+06	421322	465688	958605	892653	574771	621283	923752	858340
Scaled Cost	0.83								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.6 ± 6	2.3 ± 5	2.3 ± 5	3.1 ± 8	2.4 ± 7	2.5 ± 6	1.8 ± 4	4 ± 8	2.4 ± 6
Avg. Comb. Fanout	2.4 ± 5	2.0 ± 4	1.8 ± 5	2.3 ± 5	2.0 ± 5	2.5 ± 5	1.6 ± 3.9	4 ± 7	2.2 ± 5
Avg. PI Fanout	3.2 ± 9	2.5 ± 9	3.2 ± 6	31 ± 33	5 ± 13	2.1 ± 6	2.1 ± 5	5 ± 11	2.7 ± 8
Avg. DFF Fanout	2.7 ± 3.9	2.5 ± 4	2.5 ± 3.4	5 ± 0.5	N/A	3.6 ± 2.6	N/A	2.0 ± 6	N/A
Avg. Comb. Fanin	3.6 ± 0.5	3.4 ± 0.5	3.7 ± 0.6	3.5 ± 0.5	3.4 ± 0.5	3.7 ± 0.5	3.6 ± 0.5	3.7 ± 0.4	3.7 ± 0.4
Max Fanout	81	66	39	81	70	69	36	57	62

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1168	235	211	43	75	186	201	76	141	62	48	11	0	0	3	0	0	0
1	306	112	71	10	3	53	38	9	10	32	32	0	0	0	0	0	0	0
2	273	69	66	18	3	41	12	33	31	0	0	0	0	0	0	0	0	0
3	161	32	95	0	6	21	6	1	0	0	0	0	0	0	0	0	0	0
4	154	1	32	1	15	33	4	67	1	67	1	1	1	0	0	0	64	0
5	581	0	1	130	38	25	95	137	155	64	0	0	0	32	0	32	0	0
6	232	0	0	33	0	2	61	71	65	32	0	0	0	0	0	32	0	0
7	139	0	0	66	0	34	3	4	32	1	0	0	0	0	1	0	0	0
8	106	0	0	64	0	35	1	4	2	4	0	0	0	0	1	1	1	1
9	96	0	0	71	1	18	2	2	2	3	0	0	0	0	1	1	0	1
10	89	0	0	60	6	15	3	3	2	3	0	0	0	0	0	2	0	1
11	72	1	0	0	64	0	3	2	2	3	0	0	0	0	0	2	0	1
12	75	1	0	0	66	0	3	3	2	3	0	0	0	0	0	2	0	1
13	77	1	0	0	69	0	3	2	2	3	0	0	0	0	0	2	0	1
14	94	1	0	0	85	0	3	3	2	3	0	0	0	0	0	2	0	1
15	15	1	0	0	7	0	3	2	2	3	0	0	0	0	0	2	0	1
16	16	1	0	0	7	0	3	3	2	3	0	0	0	0	0	2	0	1
17	11	1	0	0	3	0	3	2	2	3	0	0	0	0	0	2	0	1
18	13	1	0	0	4	0	3	3	2	3	0	0	0	0	0	2	0	1
19	12	1	0	0	4	0	3	2	2	3	0	0	0	0	0	2	0	1
20	13	1	0	0	4	0	3	3	2	3	0	0	0	0	0	2	0	1
21	12	1	0	0	4	0	3	2	2	3	0	0	0	0	0	2	0	1
22	13	1	0	0	4	0	3	3	2	3	0	0	0	0	0	2	0	1
23	12	1	0	0	4	0	3	2	2	3	0	0	0	0	0	2	0	1
24	13	1	0	0	4	0	3	3	2	3	0	0	0	0	0	2	0	1
25	12	1	0	0	4	0	3	2	2	3	0	0	0	0	0	2	0	1
26	13	1	0	0	4	0	3	3	2	3	0	0	0	0	0	2	0	1
27	11	1	0	0	3	0	3	2	2	3	0	0	0	0	0	2	0	1
28	12	1	0	0	3	0	3	3	2	3	0	0	0	0	0	2	0	1
29	12	1	0	0	4	0	3	2	2	3	0	0	0	0	0	2	0	1
30	12	1	0	0	3	0	3	3	2	3	0	0	0	0	0	2	0	1
31	11	1	0	0	3	0	3	2	2	3	0	0	0	0	0	2	0	1
32	12	1	0	0	3	0	3	3	2	3	0	0	0	0	0	2	0	1
33	11	1	0	0	3	0	3	2	2	3	0	0	0	0	0	2	0	1
34	12	1	0	0	3	0	3	3	2	3	0	0	0	0	0	2	0	1
35	11	1	0	0	3	0	3	2	2	3	0	0	0	0	0	2	0	1
36	12	1	0	0	3	0	3	3	2	4	0	0	0	0	0	2	1	1
37	11	1	0	0	3	0	3	2	2	4	0	0	0	0	0	2	1	1
38	9	0	0	0	3	0	3	1	2	5	0	0	0	0	0	3	1	1
39	5	0	0	0	3	0	0	0	2	2	0	0	0	0	0	0	0	2
40	3	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0
41	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
42	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3652	600	634	483	349	458	442	300	386
1	1013	334	277	29	8	165	145	27	28	1698	262	192	226	99	289	85	264	281
2	1080	275	262	68	11	162	47	131	124	543	101	127	48	38	83	16	68	62
3	564	128	316	0	20	73	23	4	0	425	33	65	0	192	64	68	3	0
4	575	4	127	4	60	131	12	235	2	1113	0	1	13	15	49	67	938	30
5	2226	0	3	487	120	100	348	548	620	644	0	0	161	6	53	96	144	184
6	836	0	0	131	0	6	212	256	231	378	0	0	98	0	25	57	101	97
7	518	0	0	231	0	134	9	16	128	236	0	0	126	0	36	5	5	64
8	401	0	0	240	0	137	3	13	8	162	0	0	120	0	36	0	3	3
9	327	0	0	229	4	71	7	8	8	156	0	0	129	1	18	2	3	3
10	295	0	0	188	20	59	11	11	6	150	0	0	114	12	14	4	3	3
11	222	3	0	0	194	0	11	8	6	136	0	0	0	126	0	4	3	3
12	232	3	0	0	203	0	9	11	6	137	0	0	0	127	0	4	3	3
13	248	3	0	0	220	0	11	8	6	135	0	0	0	125	0	4	3	3
14	371	3	0	0	340	0	11	11	6	95	0	0	0	85	0	4	3	3
15	55	3	0	0	27	0	11	8	6	16	0	0	0	6	0	4	3	3
16	53	3	0	0	22	0	11	11	6	12	0	0	0	2	0	4	3	3
17	40	3	0	0	12	0	11	8	6	13	0	0	0	3	0	4	3	3
18	46	3	0	0	15	0	11	11	6	13	0	0	0	3	0	4	3	3
19	43	3	0	0	15	0	11	8	6	13	0	0	0	3	0	4	3	3
20	46	3	0	0	15	0	11	11	6	13	0	0	0	3	0	4	3	3
21	43	3	0	0	15	0	11	8	6	13	0	0	0	3	0	4	3	3
22	46	3	0	0	15	0	11	11	6	13	0	0	0	3	0	4	3	3
23	43	3	0	0	15	0	11	8	6	13	0	0	0	3	0	4	3	3
24	46	3	0	0	15	0	11	11	6	13	0	0	0	3	0	4	3	3
25	43	3	0	0	15	0	11	8	6	13	0	0	0	3	0	4	3	3
26	44	3	0	0	13	0	11	11	6	12	0	0	0	2	0	4	3	3
27	38	3	0	0	10	0	11	8	6	12	0	0	0	2	0	4	3	3
28	43	3	0	0	12	0	11	11	6	13	0	0	0	3	0	4	3	3
29	41	3	0	0	13	0	11	8	6	12	0	0	0	2	0	4	3	3
30	41	3	0	0	10	0	11	11	6	12	0	0	0	2	0	4	3	3
31	38	3	0	0	10	0	11	8	6	12	0	0	0	2	0	4	3	3
32	41	3	0	0	10	0	11	11	6	12	0	0	0	2	0	4	3	3
33	38	3	0	0	10	0	11	8	6	12	0	0	0	2	0	4	3	3
34	41	3	0	0	10	0	11	11	6	12	0	0	0	2	0	4	3	3
35	38	3	0	0	10	0	11	8	6	12	0	0	0	2	0	4	3	3
36	42	3	0	0	10	0	11	12	6	14	0	0	0	2	0	4	5	3
37	38	3	0	0	10	0	11	8	6	9	0	0	0	2	0	3	1	3
38	29	0	0	0	10	0	9	4	6	5	0	0	0	2	0	0	0	3
39	16	0	0	0	10	0	0	0	6	3	0	0	0	2	0	0	0	1
40	10	0	0	0	10	0	0	0	0	2	0	0	0	2	0	0	0	0
41	6	0	0	0	6	0	0	0	0	1	0	0	0	1	0	0	0	0
42	4	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	137	73	32	0	0	32	0	0	0	4487	502	533	528	448	399	385	554	308
2	4	4	0	0	0	0	0	0	0	1184	175	195	138	32	137	128	137	95
3	32	0	32	0	0	0	0	0	0	606	32	199	70	26	95	11	71	33
4	95	1	31	1	0	0	0	62	0	651	1	33	176	39	101	6	78	165
5	33	0	1	32	0	0	0	0	0	1019	0	1	149	74	66	165	239	284
6	0	0	0	0	0	0	0	0	0	285	0	0	34	6	3	94	40	99
7	0	0	0	0	0	0	0	0	0	180	0	0	85	4	68	5	6	10
8	1	0	0	0	0	1	0	0	0	129	0	0	49	5	48	4	7	8
9	1	0	0	0	0	1	0	0	0	176	0	0	87	14	44	4	6	6
10	1	0	0	0	0	1	0	0	0	161	0	0	59	41	15	4	7	4
11	1	1	0	0	0	0	0	0	0	202	2	0	0	182	0	4	6	4
12	1	1	0	0	0	0	0	0	0	110	2	0	0	84	0	4	7	4
13	1	1	0	0	0	0	0	0	0	134	2	0	0	113	0	4	6	4
14	1	1	0	0	0	0	0	0	0	71	2	0	0	17	0	4	7	4
15	2	1	0	0	1	0	0	0	0	31	2	0	0	9	0	4	6	4
16	6	1	0	0	5	0	0	0	0	31	2	0	0	8	0	4	7	4
17	1	1	0	0	0	0	0	0	0	30	2	0	0	9	0	4	6	4
18	2	1	0	0	1	0	0	0	0	33	2	0	0	9	0	4	7	4
19	2	1	0	0	1	0	0	0	0	31	2	0	0	9	0	4	6	4
20	2	1	0	0	1	0	0	0	0	30	2	0	0	8	0	4	7	4
21	2	1	0	0	1	0	0	0	0	30	2	0	0	9	0	4	6	4
22	2	1	0	0	1	0	0	0	0	32	2	0	0	10	0	4	7	4
23	2	1	0	0	1	0	0	0	0	30	2	0	0	10	0	4	6	4
24	2	1	0	0	1	0	0	0	0	29	2	0	0	8	0	4	7	4
25	2	1	0	0	1	0	0	0	0	27	2	0	0	8	0	4	6	4
26	3	1	0	0	2	0	0	0	0	31	2	0	0	8	0	4	7	4
27	2	1	0	0	1	0	0	0	0	25	2	0	0	5	0	4	6	4
28	1	1	0	0	0	0	0	0	0	28	2	0	0	7	0	4	7	4
29	3	1	0	0	2	0	0	0	0	21	2	0	0	3	0	4	4	4
30	2	1	0	0	1	0	0	0	0	25	2	0	0	4	0	5	6	4
31	2	1	0	0	1	0	0	0	0	28	2	0	0	3	0	5	10	4
32	2	1	0	0	1	0	0	0	0	22	2	0	0	3	0	2	6	4
33	2	1	0	0	1	0	0	0	0	12	2	0	0	3	0	2	3	2
34	2	1	0	0	1	0	0	0	0	9	2	0	0	3	0	2	2	0
35	2	1	0	0	1	0	0	0	0	10	2	0	0	3	0	2	3	0
36	2	1	0	0	1	0	0	0	0	7	2	0	0	3	0	2	0	0
37	2	1	0	0	1	0	0	0	0	10	2	0	0	3	0	4	1	0
38	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
39	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
40	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
41	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
42	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	76	32	0	35	0	33	0	0	0	105	96	33	32	35	0	62	0
1	137	57	1	142	196	37	99	107	191	4487	74	56	131	0	13	33	493	30
2	4	0	2	33	5	4	2	67	34	1184	70	0	4	0	0	3	65	5
3	32	1	20	16	7	16	2	5	2	606	20	2	6	0	0	6	32	3
4	95	0	0	1	16	1	2	32	0	651	32	0	1	0	15	1	0	3
5	33	0	1	32	3	0	5	0	0	1019	1	0	0	0	36	0	0	4
6	0	0	0	0	5	0	3	1	0	285	0	0	1	0	6	0	0	2
7	0	0	0	0	0	0	2	0	0	180	0	0	0	0	2	0	0	0
8	1	0	0	0	2	2	4	0	0	129	1	0	0	1	3	0	1	2
9	1	0	0	0	10	1	4	0	0	176	2	0	0	0	3	0	8	2
10	1	0	0	8	18	1	4	0	0	161	1	0	0	8	3	0	17	2
11	1	0	0	0	2	0	2	0	0	202	0	0	0	0	2	0	0	2
12	1	0	0	0	5	0	4	0	0	110	0	0	0	0	7	0	0	2
13	1	0	0	0	1	0	4	0	0	134	0	0	0	0	3	0	0	2
14	1	0	0	0	33	0	4	0	0	71	31	0	0	0	4	0	0	2
15	2	0	0	0	2	0	4	0	0	31	0	0	0	0	4	0	0	2
16	6	0	0	0	2	0	4	0	0	31	0	0	0	0	4	0	0	2
17	1	0	0	0	1	0	4	0	0	30	0	0	0	0	3	0	0	2
18	2	0	0	0	1	0	6	0	0	33	0	0	0	0	5	0	0	2
19	2	0	0	0	2	0	4	0	0	31	0	0	0	0	4	0	0	2
20	2	0	0	0	1	0	4	0	0	30	0	0	0	0	3	0	0	2
21	2	0	0	0	1	0	4	0	0	30	0	0	0	0	3	0	0	2
22	2	0	0	0	1	0	4	0	0	32	0	0	0	0	3	0	0	2
23	2	0	0	0	0	0	4	0	0	30	0	0	0	0	2	0	0	2
24	2	0	0	0	0	0	4	0	0	29	0	0	0	0	2	0	0	2
25	2	0	0	0	1	0	2	0	0	27	0	0	0	0	1	0	0	2
26	3	0	0	0	0	0	6	0	0	31	0	0	0	0	4	0	0	2
27	2	0	0	0	0	0	4	0	0	25	0	0	0	0	2	0	0	2
28	1	0	0	0	0	0	4	0	0	28	0	0	0	0	2	0	0	2
29	3	0	0	0	0	0	4	0	0	21	0	0	0	0	2	0	0	2
30	2	0	0	0	0	0	4	0	0	25	0	0	0	0	2	0	0	2
31	2	0	0	0	0	0	4	0	0	28	0	0	0	0	2	0	0	2
32	2	0	0	0	1	0	4	0	0	22	0	0	0	0	4	0	0	1
33	2	0	0	0	0	0	0	0	0	12	0	0	0	0	0	0	0	0
34	2	0	0	0	0	0	0	0	0	9	0	0	0	0	0	0	0	0
35	2	0	0	0	0	0	0	0	0	10	0	0	0	0	0	0	0	0
36	2	0	0	0	0	0	0	0	0	7	0	0	0	0	0	0	0	0
37	2	0	0	0	0	0	0	0	0	10	0	0	0	0	0	0	0	0
38	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
39	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
41	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
42	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (370 2047 1033 203 42 28 4 14 3 2 0 4 15 17 4 2 18 9 9 5 2 0 1 0 1 0 1 0 0 1 9 5 44 5 3 0, 6 0 1 1 0 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 1 2 0 0 1 3 0 0 1 1 0 1 0 0 1 0 0 0 0 0 1)
Cluster 1: (73 198 133 57 3 2 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6 1 0 0 1 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (96 190 132 43 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4 6 0 1 0 1 0 0 1)
Cluster 3: (32 182 199 24 19 17 1 0 0 0 0 0 0 1 0 0 9 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 4 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1)
Cluster 4: (64 227 221 1 2 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 9 1 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1)
Cluster 5: (35 293 77 8 12 4 1 11 3 2 0 0 0 1 2 1 1 2 0 0 0 0 0 0 0 0 0 0 0 1 2 1 4 0 0 0 0 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (65 304 90 35 2 3 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 4 2 0 0 2)
Cluster 7: (4 333 53 4 2 1 0 0 0 0 0 3 14 15 2 1 8 6 8 5 2 0 1 0 0 0 1 0 0 0 0 0 5 1 0 0 2 0 0 0 0, 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (1 320 128 31 2 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 5 0 6 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	24	3	35	3	0	167	0	103	1	0	0	0	0	1	0
22	0	0	0	0	0	36	0	21	75	0	0	0	0	0	0
0	0	0	136	0	0	5	2	1	0	32	0	0	0	0	0
0	0	8	0	1	0	0	0	32	0	0	0	0	0	0	0
5	0	32	50	0	62	0	0	0	0	0	0	35	0	0	0
27	0	0	0	1	0	4	11	0	0	0	0	0	0	0	0
4	0	189	63	52	94	0	214	30	0	0	0	0	0	32	0
0	0	0	32	5	59	0	0	0	0	0	0	0	0	0	0

exponent_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	644	86	88	87	81	71	82	78	71
Number of PI	85	14	2	8	25	6	4	15	11
Number of DFF	64	12	13	9	0	14	2	2	12
Number of Combinational Nodes	559	72	86	79	56	65	78	63	60
Number of PO	86	14	22	16	0	14	14	0	6
Number of Edges	1839	286	354	360	267	214	323	271	277
Number of Intra-Cluster Edges	1322	160	176	177	184	114	199	195	113
Number of Inter-Cluster Input Edges	1030	63	89	72	39	63	78	39	66
Number of Inter-Cluster Output Edges	1030	62	89	111	44	37	46	34	98
Wirelength Approx	170992	18236	28002	22786	17712	15287	29795	24455	14719
Scaled Cost	1.64								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.8 ± 3.7	2.5 ± 2.9	3.0 ± 3.4	3.3 ± 5	2.8 ± 2.9	2.1 ± 3.1	2.9 ± 5	2.9 ± 3.0	2.9 ± 3.7
Avg. Comb. Fanout	2.0 ± 2.7	1.9 ± 2.9	1.6 ± 0.6	2.3 ± 4	2.5 ± 3.3	2.1 ± 3.6	1.7 ± 0.4	2.8 ± 3.0	1.3 ± 1.0
Avg. PI Fanout	4 ± 6	1.9 ± 0.5	17 ± 0.5	2 ± 0.5	3.3 ± 1.8	2 ± 1.4	25 ± 8	2.4 ± 2.3	6 ± 6
Avg. DFF Fanout	7 ± 3.5	7 ± 1.6	9 ± 2.7	12 ± 0.4	N/A	2 ± 0	8 ± 0	8 ± 0	7 ± 2.2
Avg. Comb. Fanin	3.5 ± 0.6	3.5 ± 0.7	3.5 ± 0.5	3.5 ± 0.6	3.7 ± 0.5	3.4 ± 0.8	3.6 ± 0.5	3.6 ± 0.5	3.7 ± 0.6
Max Fanout	32	17	17	25	16	16	32	12	20

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	149	26	15	17	25	20	6	17	23	48	12	11	9	0	14	0	0	2
1	106	11	19	7	10	0	33	10	16	0	0	0	0	0	0	0	0	0
2	56	7	2	3	12	0	14	9	9	3	1	1	1	0	0	0	0	0
3	55	15	4	3	13	3	0	12	5	5	1	0	1	0	0	0	0	3
4	30	12	2	3	4	2	1	4	2	2	0	0	1	0	0	0	0	1
5	24	9	1	3	3	2	2	4	0	2	0	0	1	0	0	1	0	0
6	16	1	1	3	1	0	2	8	0	2	0	0	1	0	0	1	0	0
7	22	1	2	5	1	0	2	11	0	2	0	1	0	0	0	1	0	0
8	45	1	4	22	7	0	2	3	6	2	0	1	0	0	0	1	0	0
9	17	1	5	7	2	0	2	0	0	2	0	1	0	0	0	1	0	0
10	12	1	5	2	2	0	2	0	0	2	0	0	1	0	0	1	0	0
11	8	1	2	3	0	0	2	0	0	2	0	0	1	0	0	1	0	0
12	8	0	3	3	0	0	2	0	0	2	0	1	0	0	0	1	0	0
13	8	0	3	2	1	0	2	0	0	2	0	1	0	0	0	1	0	0
14	8	0	4	2	0	0	2	0	0	3	0	2	0	0	0	1	0	0
15	7	0	4	1	0	0	2	0	0	2	0	1	0	0	0	1	0	0
16	6	0	4	0	0	0	2	0	0	2	0	1	0	0	0	1	0	0
17	6	0	3	1	0	0	2	0	0	2	0	1	0	0	0	1	0	0
18	6	0	3	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0
19	32	0	1	0	0	25	1	0	5	1	0	0	0	0	0	1	0	0
20	17	0	0	0	0	14	0	0	3	0	0	0	0	0	0	0	0	0
21	6	0	1	0	0	3	0	0	2	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	811	105	147	122	83	40	114	53	147
1	395	43	73	26	29	0	130	31	63	244	13	32	12	45	0	47	76	19
2	218	27	8	9	46	0	56	36	36	165	41	4	6	43	0	28	27	16
3	197	59	16	9	52	10	0	38	13	114	24	4	6	15	20	0	35	10
4	110	44	8	9	16	7	3	16	7	51	12	1	6	7	16	2	5	2
5	68	19	2	9	10	8	6	14	0	30	9	0	7	3	2	4	5	0
6	57	3	3	10	4	0	6	31	0	44	1	2	21	4	0	4	12	0
7	79	3	6	16	4	0	6	44	0	97	1	4	63	16	0	4	9	0
8	171	3	13	85	28	0	6	12	24	42	1	8	22	7	0	4	0	0
9	61	3	16	28	8	0	6	0	0	19	1	10	2	2	0	4	0	0
10	41	3	17	7	8	0	6	0	0	17	1	8	3	1	0	4	0	0
11	25	3	7	9	0	0	6	0	0	11	1	3	3	0	0	4	0	0
12	27	0	9	12	0	0	6	0	0	11	0	5	2	0	0	4	0	0
13	26	0	9	7	4	0	6	0	0	11	0	5	1	1	0	4	0	0
14	26	0	14	6	0	0	6	0	0	10	0	5	1	0	0	4	0	0
15	23	0	14	3	0	0	6	0	0	10	0	6	0	0	0	4	0	0
16	19	0	13	0	0	0	6	0	0	8	0	4	0	0	0	4	0	0
17	21	0	11	4	0	0	6	0	0	8	0	4	1	0	0	3	0	0
18	23	0	11	0	0	8	4	0	0	34	0	2	0	0	31	1	0	0
19	127	0	3	0	0	100	4	0	20	32	0	0	0	0	25	2	0	5
20	48	0	0	0	0	36	0	0	12	6	0	0	0	0	3	0	0	3
21	13	0	3	0	0	6	0	0	4	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	3	0
1	0	0	0	0	0	0	0	0	0	902	94	95	78	82	55	112	86	59
2	0	0	0	0	0	0	0	0	0	253	24	2	26	54	4	29	47	17
3	5	1	4	0	0	0	0	0	0	119	15	9	11	19	2	3	19	3
4	6	3	1	0	0	0	0	1	1	79	19	2	11	6	2	4	19	1
5	10	8	1	0	0	0	0	1	0	35	2	1	10	1	3	4	4	0
6	0	0	0	0	0	0	0	0	0	45	1	3	7	8	0	4	11	0
7	2	0	0	0	0	0	0	2	0	38	1	4	9	2	0	4	7	0
8	9	0	0	0	0	0	0	3	6	83	1	11	17	7	0	4	2	18
9	5	0	0	5	0	0	0	0	0	23	1	6	4	2	0	4	0	0
10	1	0	0	0	1	0	0	0	0	23	1	6	3	1	0	4	0	0
11	1	0	0	1	0	0	0	0	0	17	1	4	1	1	0	4	0	0
12	1	0	0	1	0	0	0	0	0	13	0	6	0	0	0	4	0	0
13	1	0	0	1	0	0	0	0	0	16	0	7	0	1	0	4	0	0
14	1	0	0	1	0	0	0	0	0	13	0	6	0	0	0	4	0	0
15	1	0	0	1	0	0	0	0	0	29	0	4	0	0	16	4	0	1
16	1	0	1	0	0	0	0	0	0	24	0	5	0	0	10	2	0	4
17	1	0	1	0	0	0	0	0	0	12	0	3	0	0	3	2	0	0
18	1	0	1	0	0	0	0	0	0	13	0	2	0	0	4	1	0	2
19	1	0	1	0	0	0	0	0	0	32	0	0	0	0	15	2	0	5
20	11	0	0	0	0	11	0	0	0	6	0	0	0	0	0	0	0	3
21	6	0	1	0	0	3	0	0	2	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	13	9	0	14	2	2	12	0	0	12	11	10	1	14	0	7	9
1	0	22	42	32	10	6	61	16	52	902	39	57	47	14	5	20	17	42
2	0	7	7	6	6	4	14	3	3	253	4	2	8	4	13	6	1	12
3	5	13	8	5	1	7	0	2	2	119	2	3	16	5	0	3	4	5
4	6	2	2	5	0	4	0	2	0	79	0	2	3	4	0	2	0	4
5	10	0	0	7	0	3	0	0	0	35	1	2	0	3	0	1	1	2
6	0	1	1	5	1	2	0	1	0	45	0	1	3	6	0	1	0	0
7	2	1	4	2	0	2	0	2	0	38	2	1	2	3	0	2	0	1
8	9	1	5	7	7	2	0	1	0	83	2	1	6	2	0	2	2	8
9	5	1	2	1	0	2	0	0	0	23	0	1	4	0	0	1	0	0
10	1	1	4	1	0	2	0	0	0	23	0	3	3	1	0	1	0	0
11	1	1	3	0	0	2	0	0	0	17	0	2	3	0	0	1	0	0
12	1	0	0	1	0	2	0	0	0	13	0	1	0	0	0	1	0	1
13	1	0	0	0	0	1	0	0	3	16	0	0	2	1	0	1	0	0
14	1	0	1	0	0	2	0	0	0	13	0	0	1	0	0	1	0	1
15	1	0	1	0	0	1	0	0	2	29	0	0	1	0	2	1	0	0
16	1	0	0	0	0	2	0	0	1	24	0	0	1	0	0	0	0	2
17	1	0	0	0	0	1	0	0	3	12	0	0	1	0	2	0	0	1
18	1	0	0	0	0	3	1	0	0	13	0	0	0	0	1	0	0	3
19	1	0	0	0	0	10	0	0	0	32	0	2	0	0	0	2	0	6
20	11	0	0	0	0	3	0	0	0	6	0	0	0	0	0	0	2	1
21	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (54 272 176 27 19 7 20 0 21 3 5 6 14 3 0 2 6 4 1 0 1 0 0 0 0 1 0 0 0 0 0 0 2)
Cluster 1: (2 56 9 3 0 0 11 0 1 0 0 1 1 1 0 0 0 1)
Cluster 2: (9 25 36 2 1 1 4 0 2 1 0 1 3 1 0 0 1 1)
Cluster 3: (10 35 25 2 1 1 0 0 0 0 0 2 7 0 0 1 2 0 0 0 0 0 0 0 0 1)
Cluster 4: (1 40 12 8 8 2 2 0 2 1 2 1 0 1 0 0 1)
Cluster 5: (14 35 14 1 2 0 0 0 2 0 0 0 0 0 0 1 2)
Cluster 6: (0 21 55 0 0 0 0 0 2 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 7: (7 30 14 9 5 3 0 0 2 1 3 1 3)
Cluster 8: (11 30 11 2 2 0 3 0 10 0 0 0 0 0 0 0 0 0 0 1 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	18	5	1	0	3	13	10	11	1	0	0	0	0	0	0
16	0	16	3	12	18	2	11	0	11	0	0	0	0	0	0
26	33	0	7	4	17	2	12	0	1	9	0	0	0	0	0
3	4	32	0	0	0	1	3	1	0	0	0	0	0	0	0
0	0	0	0	0	14	0	9	0	0	0	0	14	0	0	0
0	6	8	3	16	0	2	11	0	0	0	0	0	0	0	0
0	6	4	0	3	4	0	10	0	0	0	0	0	2	2	3
5	13	7	11	26	20	7	0	0	0	0	0	0	0	0	9

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Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	4444	464	666	463	665	495	515	514	662
Number of PI	19	0	0	0	0	0	1	1	17
Number of DFF	886	63	24	115	152	129	74	105	224
Number of Combinational Nodes	4425	464	666	463	665	495	514	513	645
Number of PO	116	30	2	16	0	2	32	18	16
Number of Edges	13525	1896	3120	1766	2535	1782	1870	1917	2531
Number of Intra-Cluster Edges	9572	892	1782	899	1340	1025	1169	1114	1350
Number of Inter-Cluster Input Edges	7845	568	705	497	590	353	505	539	134
Number of Inter-Cluster Output Edges	7845	436	633	370	605	403	196	264	1047
Wirelength Approx	1.44e+07	1.72e+06	2.96e+06	1.35e+06	2.11e+06	1.49e+06	1.78e+06	1.41e+06	1.56e+06
Scaled Cost	1.56								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.0 ± 18	2.8 ± 7	3.6 ± 28	2.7 ± 5	2.9 ± 14	2.8 ± 5	2.6 ± 9	2.6 ± 6	3.6 ± 30
Avg. Comb. Fanout	2.5 ± 15	2.0 ± 6	3.5 ± 29	2.7 ± 5	2.7 ± 15	2.1 ± 3.9	2.5 ± 10	1.9 ± 5	2.2 ± 6
Avg. PI Fanout	42 ± 172	N/A	N/A	N/A	N/A	N/A	2 ± 0	4 ± 0	46 ± 182
Avg. DFF Fanout	4 ± 6	8 ± 6	5 ± 2.4	2.6 ± 2.5	3.5 ± 7	5 ± 8	3.4 ± 3.2	6 ± 8	2.8 ± 4
Avg. Comb. Fanin	3.5 ± 0.6	3.5 ± 0.5	3.6 ± 0.5	3.5 ± 0.6	3.5 ± 0.7	3.5 ± 0.5	3.5 ± 0.6	3.5 ± 0.6	3.5 ± 0.6
Max Fanout	773	84	598	42	334	40	123	56	773

Node Shape										PO Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	905	63	24	115	152	129	75	106	241	100	30	2	16	0	2	32	18	0	
1	530	10	4	18	59	143	36	140	120	16	0	0	0	0	0	0	0	16	
2	294	8	22	0	16	23	49	95	81	0	0	0	0	0	0	0	0	0	
3	58	2	3	1	4	4	18	26	0	0	0	0	0	0	0	0	0	0	
4	14	0	0	0	0	0	0	14	0	0	0	0	0	0	0	0	0	0	
5	55	4	1	0	2	6	0	42	0	0	0	0	0	0	0	0	0	0	
6	329	55	12	12	190	9	5	4	42	0	0	0	0	0	0	0	0	0	
7	841	127	458	27	56	11	8	41	113	0	0	0	0	0	0	0	0	0	
8	513	108	110	71	6	8	134	28	48	0	0	0	0	0	0	0	0	0	
9	258	39	12	30	5	42	111	2	17	0	0	0	0	0	0	0	0	0	
10	135	21	7	41	7	8	49	2	0	0	0	0	0	0	0	0	0	0	
11	49	2	1	13	7	8	17	1	0	0	0	0	0	0	0	0	0	0	
12	44	2	1	21	10	8	1	1	0	0	0	0	0	0	0	0	0	0	
13	49	2	1	21	15	8	1	1	0	0	0	0	0	0	0	0	0	0	
14	58	3	1	12	32	8	1	1	0	0	0	0	0	0	0	0	0	0	
15	46	2	1	12	21	8	1	1	0	0	0	0	0	0	0	0	0	0	
16	56	2	1	15	28	8	1	1	0	0	0	0	0	0	0	0	0	0	
17	41	3	1	7	20	8	1	1	0	0	0	0	0	0	0	0	0	0	
18	52	2	1	25	14	8	1	1	0	0	0	0	0	0	0	0	0	0	
19	39	2	1	12	14	8	1	1	0	0	0	0	0	0	0	0	0	0	
20	26	2	0	6	7	9	1	1	0	0	0	0	0	0	0	0	0	0	
21	14	2	1	1	0	8	1	1	0	0	0	0	0	0	0	0	0	0	
22	14	1	1	1	0	9	1	1	0	0	0	0	0	0	0	0	0	0	
23	24	2	2	2	0	14	2	2	0	0	0	0	0	0	0	0	0	0	

Input Shape										Output Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	0	0	0	0	0	0	0	0	0	4378	503	109	303	536	635	258	596	1438	
1	1854	28	12	70	209	503	122	469	441	1460	10	108	32	90	218	240	318	444	
2	987	32	86	0	64	71	180	310	244	939	238	542	0	16	39	33	70	1	
3	181	5	12	2	8	12	54	88	0	279	18	3	3	179	5	16	55	0	
4	51	0	0	0	0	0	0	51	0	132	0	0	0	0	0	0	132	0	
5	218	16	4	0	7	24	0	167	0	457	4	35	0	369	6	0	43	0	
6	1305	217	48	47	758	35	20	15	165	1917	87	1018	175	308	92	33	10	194	
7	3011	439	1701	85	149	40	26	164	407	1348	244	453	176	25	11	328	45	66	
8	1906	397	389	246	24	31	517	110	192	806	122	110	162	57	78	240	5	32	
9	899	142	46	120	20	164	366	6	35	248	18	9	64	0	46	110	1	0	
10	484	64	22	145	23	28	196	6	0	88	2	0	42	0	12	32	0	0	
11	137	7	4	43	16	28	36	3	0	63	2	0	49	0	12	0	0	0	
12	161	7	4	82	33	28	4	3	0	82	2	0	28	40	12	0	0	0	
13	168	7	4	78	44	28	4	3	0	87	2	0	32	41	12	0	0	0	
14	202	11	4	41	111	28	4	3	0	65	3	0	7	43	12	0	0	0	
15	159	7	4	41	72	28	4	3	0	75	2	0	23	38	12	0	0	0	
16	189	7	4	49	94	28	4	3	0	45	2	0	5	26	12	0	0	0	
17	140	10	4	23	68	28	4	3	0	53	2	0	15	24	12	0	0	0	
18	177	7	4	92	39	28	4	3	0	39	2	0	25	0	12	0	0	0	
19	126	7	4	41	39	28	4	3	0	26	2	0	12	0	12	0	0	0	
20	92	7	0	23	23	32	4	3	0	14	2	0	0	0	12	0	0	0	
21	50	7	4	4	0	28	4	3	0	14	2	0	0	0	12	0	0	0	
22	51	4	4	4	0	32	4	3	0	24	0	0	0	0	24	0	0	0	
23	91	8	8	8	0	52	8	7	0	0	0	0	0	0	0	0	0	0	

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	40	0	0	1	2	12	7	5	13	7130	375	1211	429	652	655	857	764	900
2	147	0	0	0	0	1	16	50	80	656	42	69	68	66	8	80	66	37
3	4	0	0	0	0	1	2	1	0	407	4	2	33	190	7	3	75	0
4	2	0	0	0	0	0	0	2	0	292	56	4	29	10	9	2	40	1
5	0	0	0	0	0	0	0	0	0	817	139	404	20	27	14	6	42	16
6	15	2	0	2	5	2	2	0	2	756	100	14	14	152	13	4	39	140
7	139	0	5	0	35	0	0	5	94	996	62	42	26	24	18	68	42	176
8	41	0	0	0	1	1	0	23	16	583	64	4	85	41	17	66	16	80
9	64	22	3	8	5	7	1	1	17	231	5	3	15	27	65	51	2	0
10	82	20	7	22	7	7	17	2	0	98	5	3	34	24	17	3	2	0
11	40	1	1	6	7	7	17	1	0	71	5	3	14	16	17	3	2	0
12	24	1	1	6	7	7	1	1	0	91	5	3	25	22	17	3	2	0
13	24	1	1	6	7	7	1	1	0	88	5	3	22	25	17	3	2	0
14	36	1	1	11	14	7	1	1	0	78	6	1	20	18	17	3	2	0
15	24	1	1	6	7	7	1	1	0	54	4	3	10	10	17	3	2	0
16	36	1	1	11	14	7	1	1	0	59	4	4	13	8	19	4	2	0
17	24	2	1	5	7	7	1	1	0	68	5	4	11	8	25	4	2	0
18	36	1	1	11	14	7	1	1	0	41	1	1	12	10	12	1	2	0
19	36	1	1	11	14	7	1	1	0	38	1	1	11	8	12	1	2	0
20	24	1	0	6	7	8	1	1	0	28	1	0	5	2	15	1	2	0
21	12	1	1	1	0	7	1	1	0	20	1	1	1	0	12	1	2	0
22	12	1	1	1	0	7	1	1	0	29	1	1	1	0	19	1	4	0
23	24	2	2	2	0	14	2	2	0	8	1	1	1	0	3	1	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	24	115	152	129	74	105	224	0	0	59	28	116	153	130	75	103	222
1	40	299	76	178	136	168	148	226	56	7130	55	296	129	227	139	35	67	339
2	147	79	32	38	7	6	37	21	0	656	1	120	6	4	8	2	70	9
3	4	3	0	11	7	5	35	3	29	407	9	27	4	38	0	1	5	9
4	2	24	2	20	46	16	6	19	8	292	13	66	0	8	1	40	3	10
5	0	35	34	13	38	8	8	12	1	817	48	47	1	0	11	0	5	37
6	15	24	19	24	189	10	4	2	8	756	59	22	2	10	3	8	9	167
7	139	46	412	15	5	3	16	25	16	996	65	1	50	120	90	27	2	183
8	41	32	14	12	9	6	115	6	16	583	39	20	44	30	16	8	0	53
9	64	0	0	8	5	20	30	0	0	231	48	4	5	2	0	0	0	4
10	82	0	0	3	4	3	0	0	0	98	4	0	4	1	0	0	0	1
11	40	1	0	3	4	3	0	0	0	71	3	0	5	2	0	0	0	1
12	24	0	0	9	2	3	0	0	0	91	5	0	0	8	0	0	0	1
13	24	0	0	3	5	3	0	0	0	88	9	0	1	0	0	0	0	1
14	36	0	0	2	2	7	0	0	0	78	7	2	1	0	0	0	0	1
15	24	0	0	2	1	2	0	0	0	54	3	0	1	0	0	0	0	1
16	36	0	0	1	1	3	0	0	0	59	3	0	1	0	0	0	0	1
17	24	1	1	3	0	2	1	1	0	68	1	0	0	2	5	0	0	1
18	36	0	0	0	0	2	0	0	0	41	1	0	0	0	0	0	0	1
19	36	0	0	0	0	2	0	0	0	38	1	0	0	0	0	0	0	1
20	24	0	0	0	0	2	0	0	0	28	1	0	0	0	0	0	0	1
21	12	0	0	0	0	2	0	0	0	20	1	0	0	0	0	0	0	1
22	12	0	0	0	0	2	0	0	0	29	1	0	0	0	0	0	0	1
23	24	0	0	0	0	1	0	0	0	8	0	0	0	0	0	0	0	1

Fanout Distribution

Circuit: (869 2376 631 137 106 30 8 6 11 13 6 1 30 18 17 6 56 32 5 8 2 5 3 3 4 3 0 4 0 0 1 0 4 0 3,
4 3 6 3 3 2 0 2 0 0 0 0 1 2 1 2 0 2 0 0 1 3 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1,
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 1: (59 292 49 2 0 14 1 0 8 8 2 0 0 8 1 3 7 2 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0,
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 2: (28 589 5 0 15 2 0 0 0 2 0 1 0 2 0 0 3 1 0 1 0 1 0 0 0 0 0 4 0 0 0 0 0 0 1 2 1 2 1 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 3: (114 168 112 7 19 2 2 3 0 0 0 0 7 3 8 1 7 2 0 2 0 0 1 0 0 1 0 0 0 0 0 0 2 0 1 0 0 0 0 0,
0 0 1)

Cluster 4: (150 313 127 33 4 1 2 0 1 1 0 0 5 1 7 0 7 2 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 2,
0 0 0 0 0 0 0 0 0 1 2 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 5: (128 203 53 34 35 2 0 0 0 0 0 0 17 0 1 1 11 0 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 1 0 0 3 1,
1 1)

Cluster 6: (71 362 3 34 16 0 1 2 1 0 0 0 0 0 0 13 5 1 0 1 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)

Cluster 7: (101 259 67 27 17 7 2 1 1 2 4 0 1 4 0 1 4 3 2 1 0 2 1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0,
1 0 1 0 0 0 0 1 0 0 0 0 0 0 0 1 1)

Cluster 8: (218 190 215 0 0 2 0 0 0 0 0 0 0 0 0 4 17 0 4 0 1 0 2 3 0 0 0 0 0 0 0 1 0 0 0 2 0 0 0,
0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies

Comb								Latched							
0	90	48	68	69	52	13	37	59	0	0	0	0	0	0	0
312	0	100	52	24	61	49	7	4	24	0	0	0	0	0	0
55	48	0	123	1	21	5	1	0	0	115	0	0	0	0	1
61	124	119	0	10	44	11	83	0	0	0	150	0	0	1	2
27	90	21	0	0	100	31	4	0	0	0	0	129	1	0	0
31	26	0	0	36	0	26	2	0	0	0	2	0	73	0	0
22	60	8	9	18	44	0	0	0	0	0	0	0	0	103	0
36	152	49	209	121	78	180	0	0	0	0	0	0	0	1	221

icu_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	3813	465	497	456	457	465	413	496	564
Number of PI	275	79	20	57	93	9	7	0	10
Number of DFF	355	10	0	89	63	0	36	75	82
Number of Combinational Nodes	3538	386	477	399	364	456	406	496	554
Number of PO	267	33	0	64	85	0	19	31	35
Number of Edges	12236	1859	2292	1404	1199	2204	1634	1772	2672
Number of Intra-Cluster Edges	9426	1369	1509	905	1027	1375	802	867	1572
Number of Inter-Cluster Input Edges	5610	61	379	238	15	403	692	807	205
Number of Inter-Cluster Output Edges	5610	429	404	261	157	426	140	98	895
Wirelength Approx	4.49e+06	488255	607458	402386	385154	646519	592326	636061	732238
Scaled Cost	1.48								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.2 ± 10	3.8 ± 9	3.8 ± 7	2.5 ± 5	2.5 ± 6	3.8 ± 9	2.2 ± 3.7	1.9 ± 2.1	4 ± 19
Avg. Comb. Fanout	2.8 ± 9	3.2 ± 7	3.2 ± 6	2.3 ± 5	1.8 ± 4	3.2 ± 8	2.0 ± 3.2	1.9 ± 2.3	4 ± 19
Avg. PI Fanout	7 ± 18	6 ± 16	19 ± 11	3.2 ± 6	4 ± 11	35 ± 24	15 ± 11	N/A	22 ± 54
Avg. DFF Fanout	2.7 ± 3.0	10 ± 9	N/A	2.8 ± 3.9	3.8 ± 2.3	N/A	1.8 ± 0.3	1.9 ± 0.1	1.9 ± 0.2
Avg. Comb. Fanin	3.7 ± 0.5	3.8 ± 0.4	3.7 ± 0.5	3.4 ± 0.7	3.4 ± 0.7	3.8 ± 0.4	3.8 ± 0.4	3.7 ± 0.4	3.7 ± 0.4
Max Fanout	184	134	41	38	96	100	27	8	184

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	630	89	20	146	156	9	43	75	92	117	1	0	0	32	0	18	31	35
1	251	59	34	71	71	4	7	0	5	50	13	0	33	3	0	1	0	0
2	249	109	40	25	57	4	10	0	4	19	19	0	0	0	0	0	0	0
3	112	32	53	17	6	0	1	0	3	5	0	0	4	1	0	0	0	0
4	217	32	119	33	5	16	11	0	1	4	0	0	3	1	0	0	0	0
5	232	54	64	35	7	56	16	0	0	4	0	0	3	1	0	0	0	0
6	325	38	47	36	10	130	57	4	3	5	0	0	3	2	0	0	0	0
7	222	30	29	23	10	86	27	8	9	5	0	0	3	2	0	0	0	0
8	219	9	16	13	10	41	19	60	51	5	0	0	3	2	0	0	0	0
9	384	7	18	14	10	26	48	144	117	5	0	0	3	2	0	0	0	0
10	227	4	17	14	10	25	31	72	54	5	0	0	3	2	0	0	0	0
11	153	1	16	10	10	21	26	38	31	5	0	0	3	2	0	0	0	0
12	122	1	15	11	11	26	37	11	10	5	0	0	2	3	0	0	0	0
13	104	0	7	7	12	14	46	14	4	5	0	0	1	4	0	0	0	0
14	111	0	2	1	12	6	22	46	22	4	0	0	0	4	0	0	0	0
15	97	0	0	0	12	1	10	14	60	4	0	0	0	4	0	0	0	0
16	79	0	0	0	12	0	2	10	55	4	0	0	0	4	0	0	0	0
17	41	0	0	0	12	0	0	0	29	4	0	0	0	4	0	0	0	0
18	23	0	0	0	11	0	0	0	12	4	0	0	0	4	0	0	0	0
19	10	0	0	0	8	0	0	0	2	4	0	0	0	4	0	0	0	0
20	4	0	0	0	4	0	0	0	0	3	0	0	0	3	0	0	0	0
21	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3006	564	378	435	617	313	168	149	382
1	783	210	101	216	207	12	21	0	16	1657	303	398	73	234	184	101	0	364
2	959	416	153	96	228	14	37	0	15	1338	151	371	73	55	96	120	0	472
3	415	128	188	65	20	0	4	0	10	991	62	295	254	5	0	12	0	363
4	794	112	454	104	15	64	42	0	3	727	460	132	66	8	16	33	0	12
5	908	206	255	134	25	224	64	0	0	797	124	72	36	11	538	16	0	0
6	1229	152	187	137	35	462	228	16	12	493	56	56	36	11	214	64	32	24
7	861	120	108	85	36	344	107	28	33	324	30	47	34	11	98	36	32	36
8	830	36	60	46	36	152	73	232	195	787	23	51	13	11	87	79	292	231
9	1508	28	71	49	36	104	190	568	462	512	7	46	25	11	74	53	164	132
10	869	14	66	49	36	100	121	276	207	236	4	27	35	11	27	34	56	42
11	534	4	63	34	36	82	95	120	100	181	13	16	8	12	81	28	13	10
12	438	4	59	38	39	102	133	35	28	188	1	15	9	13	51	90	9	0
13	399	0	27	23	42	56	183	52	16	199	0	7	3	13	15	52	88	21
14	428	0	7	4	42	23	85	184	83	182	0	2	1	13	6	18	45	97
15	365	0	0	0	42	3	31	53	236	149	0	0	0	13	1	2	10	123
16	291	0	0	0	42	0	5	28	216	70	0	0	0	13	0	0	0	57
17	146	0	0	0	42	0	0	0	104	29	0	0	0	12	0	0	0	17
18	75	0	0	0	39	0	0	0	36	10	0	0	0	8	0	0	0	2
19	33	0	0	0	28	0	0	0	5	4	0	0	0	4	0	0	0	0
20	13	0	0	0	13	0	0	0	0	1	0	0	0	1	0	0	0	0
21	3	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	2	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	92	0	0	32	60	0	0	0	0	5186	710	629	470	489	603	319	562	613
2	5	0	0	1	4	0	0	0	0	1812	443	258	111	131	209	107	144	176
3	4	0	0	2	2	0	0	0	0	912	101	278	75	12	106	66	24	43
4	3	0	0	2	1	0	0	0	0	615	60	130	50	14	107	63	1	6
5	4	0	0	3	1	0	0	0	0	310	31	55	39	20	72	53	0	12
6	5	0	0	3	2	0	0	0	0	405	18	18	21	25	66	10	4	81
7	13	0	0	3	2	0	1	4	3	549	4	36	33	25	59	39	8	126
8	5	0	0	3	2	0	0	0	0	499	0	14	21	25	20	26	40	121
9	13	0	0	3	2	0	1	4	3	243	0	22	22	25	24	27	20	44
10	37	0	0	3	2	0	4	16	12	295	2	41	25	25	35	29	28	41
11	62	0	0	3	2	0	8	28	21	231	0	16	20	25	32	22	10	21
12	30	0	0	3	2	0	7	8	10	198	0	8	12	26	22	23	2	24
13	5	0	0	3	2	0	0	0	0	198	0	3	5	29	14	9	12	69
14	9	0	0	0	2	0	4	1	2	178	0	1	1	28	6	9	6	99
15	17	0	0	0	2	0	8	4	3	108	0	0	0	28	0	0	6	56
16	18	0	0	0	2	0	2	10	4	57	0	0	0	29	0	0	0	27
17	14	0	0	0	2	0	0	0	12	42	0	0	0	29	0	0	0	13
18	12	0	0	0	2	0	0	0	10	22	0	0	0	22	0	0	0	0
19	4	0	0	0	2	0	0	0	2	13	0	0	0	13	0	0	0	0
20	1	0	0	0	1	0	0	0	0	6	0	0	0	5	0	0	0	0
21	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	2	0	89	63	0	36	75	82	0	0	0	0	65	97	0	36	75	82
1	92	32	181	104	7	113	209	65	80	5186	254	141	56	28	266	38	5	3
2	5	21	30	21	4	87	45	13	12	1812	79	67	38	1	39	4	5	0
3	4	8	47	10	0	57	57	16	12	912	54	22	82	2	38	7	0	2
4	3	0	17	13	0	53	44	31	26	615	33	113	0	2	19	10	0	7
5	4	0	1	3	0	5	4	12	3	310	1	1	0	3	0	3	0	20
6	5	0	0	3	0	28	34	89	8	405	0	16	0	3	0	6	4	133
7	13	0	1	3	0	14	45	153	3	549	6	8	1	3	0	0	4	197
8	5	0	3	3	0	4	39	153	30	499	0	16	9	3	30	22	4	148
9	13	0	4	3	0	0	11	38	3	243	0	0	1	3	10	2	0	43
10	37	0	4	3	0	4	30	28	0	295	2	3	1	3	2	1	1	56
11	62	0	2	3	0	0	48	31	1	231	0	1	0	3	2	1	0	78
12	30	0	0	3	1	1	34	41	1	198	0	3	2	3	6	1	0	66
13	5	0	0	3	0	1	10	41	2	198	0	7	1	3	4	3	0	39
14	9	0	0	0	1	0	7	8	12	178	0	4	2	0	4	3	0	15
15	17	0	0	0	1	0	0	6	11	108	0	2	2	0	5	3	0	6
16	18	0	0	0	0	0	0	0	1	57	0	0	0	0	1	0	0	0
17	14	0	0	0	0	0	0	0	0	42	0	0	0	0	0	0	0	0
18	12	0	0	0	0	0	0	0	0	22	0	0	0	0	0	0	0	0
19	4	0	0	0	0	0	0	0	0	13	0	0	0	0	0	0	0	0
20	1	0	0	0	1	0	0	0	0	6	0	0	1	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (424 2287 459 79 84 88 32 13 117 9 5 7 40 24 4 3 5 1 1 2 0 2 3 1 21 10 4 6 6 5 11 6 16 0, 4 5 6 2 1 0 0 2 0 0 0 1 0 0 0 0 0 1 0 0 0 1 1 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0, 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0, 1)
Cluster 1: (32 256 49 24 20 38 5 1 5 3 0 0 2 2 0 0 0 0 0 0 0 0 1 0 3 5 0 0 2 2 4 2 6 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (0 386 16 5 7 7 0 0 3 4 5 6 11 6 3 2 2 1 0 2 0 2 1 1 5 2 2 4 0 3 3 3 0 0 2 1 0 0 0 0 0, 2)
Cluster 3: (100 191 85 26 27 2 0 0 1 0 0 0 9 0 0 0 2 0 0 0 0 0 1 0 2 0 0 1 1 0 0 1 3 0 0 2 1 0 1)
Cluster 4: (99 194 102 1 6 28 13 0 0 0 0 1 0 1 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 2 0 5 0 1 0 1 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 1)
Cluster 5: (0 366 24 12 12 0 2 0 0 2 0 0 1 14 1 0 0 0 0 0 0 0 0 0 7 2 2 0 3 0 2 0 2 0 1 2 4 2 0 0, 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (36 296 30 2 2 2 2 2 18 0 0 0 15 1 0 1 0 0 0 0 0 0 0 0 4 1 0 1)
Cluster 7: (75 285 74 1 1 5 5 5 45)
Cluster 8: (82 313 79 8 9 6 5 5 45 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0, 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	142	56	11	174	46	0	0	0	0	0	0	0	0	0	0
39	0	28	0	90	117	65	65	0	0	0	0	0	0	0	0
8	60	0	4	64	40	10	10	8	0	57	0	0	0	0	0
12	0	48	0	0	0	0	0	2	0	32	63	0	0	0	0
2	78	36	0	0	157	72	81	0	0	0	0	0	0	0	0
0	10	7	0	3	0	37	47	0	0	0	0	0	36	0	0
0	0	0	0	8	13	0	2	0	0	0	0	0	0	75	0
0	0	0	0	28	244	541	0	0	0	0	0	0	0	0	82

imdr_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1577	203	220	190	189	183	188	215	189
Number of PI	167	1	5	38	37	36	7	7	36
Number of DFF	170	26	24	2	3	15	36	30	34
Number of Combinational Nodes	1410	202	215	152	152	147	181	208	153
Number of PO	79	0	0	1	5	2	7	60	4
Number of Edges	4785	804	1026	710	613	691	644	901	617
Number of Intra-Cluster Edges	3546	462	657	435	305	405	355	547	376
Number of Inter-Cluster Input Edges	2460	197	100	155	243	144	169	121	88
Number of Inter-Cluster Output Edges	2460	141	269	120	65	142	120	233	153
Wirelength Approx	965946	125087	149445	122710	123136	101051	101722	146433	96362
Scaled Cost	1.62								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.0 ± 7	2.9 ± 6	4 ± 11	2.9 ± 9	1.9 ± 5	2.9 ± 6	2.5 ± 4	3.6 ± 6	2.7 ± 5
Avg. Comb. Fanout	2.2 ± 5	2.2 ± 6	2.1 ± 5	2.2 ± 5	1.5 ± 0.5	2.3 ± 5	2.4 ± 4	2.8 ± 5	2.3 ± 6
Avg. PI Fanout	5 ± 15	10 ± 0	49 ± 41	5 ± 17	3.5 ± 11	2.5 ± 7	7 ± 11	17 ± 14	2.1 ± 6
Avg. DFF Fanout	6 ± 3.9	8 ± 2.1	11 ± 0.8	18 ± 15	4 ± 2.9	10 ± 2.7	1.9 ± 0.4	5 ± 0.1	5 ± 0.3
Avg. Comb. Fanin	3.7 ± 0.6	3.6 ± 0.7	3.9 ± 0.2	3.9 ± 0.3	3.5 ± 0.8	3.8 ± 0.4	3.4 ± 0.8	3.5 ± 0.5	3.8 ± 0.3
Max Fanout	99	33	98	99	53	40	33	34	35

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	337	27	29	40	40	51	43	37	70	37	0	0	1	2	1	1	30	2
1	196	32	75	6	34	6	4	32	7	4	0	0	0	1	0	2	1	0
2	278	69	58	32	3	41	1	39	35	1	0	0	0	1	0	0	0	0
3	162	63	33	33	1	9	8	9	6	2	0	0	0	0	0	0	2	0
4	112	12	21	36	3	12	8	11	9	3	0	0	0	0	0	0	3	0
5	78	0	4	5	30	11	10	8	10	3	0	0	0	0	0	0	3	0
6	54	0	0	7	11	6	14	5	11	3	0	0	0	0	0	0	2	1
7	40	0	0	3	3	9	11	7	7	4	0	0	0	0	1	0	2	1
8	29	0	0	2	3	5	8	7	4	2	0	0	0	0	0	0	2	0
9	27	0	0	2	3	4	7	7	4	2	0	0	0	0	0	0	2	0
10	28	0	0	3	2	4	7	8	4	2	0	0	0	0	0	0	2	0
11	28	0	0	2	4	4	7	7	4	2	0	0	0	0	0	0	2	0
12	30	0	0	4	2	4	8	8	4	2	0	0	0	0	0	0	2	0
13	28	0	0	4	2	4	7	7	4	2	0	0	0	0	0	0	2	0
14	26	0	0	4	1	4	5	8	4	2	0	0	0	0	0	0	2	0
15	21	0	0	4	0	4	4	7	2	2	0	0	0	0	0	0	2	0
16	16	0	0	2	3	3	3	4	1	1	0	0	0	0	0	0	1	0
17	8	0	0	0	3	1	1	2	1	0	0	0	0	0	0	0	0	0
18	4	0	0	0	2	0	1	1	0	0	0	0	0	0	0	0	0	0
19	4	0	0	0	2	0	1	1	0	0	0	0	0	0	0	0	0	0
20	4	0	0	0	2	0	2	0	0	1	0	0	0	0	0	1	0	0
21	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
22	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
23	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
24	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
25	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
26	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
27	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
28	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
29	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
30	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
31	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
32	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
33	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
34	3	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
35	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
36	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
37	3	0	0	0	2	0	1	0	0	0	0	0	0	0	0	0	0	0
38	3	0	0	0	2	0	1	0	0	1	0	0	0	1	0	0	0	0
39	2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
40	2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
41	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
42	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
43	2	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
44	3	0	0	0	0	1	2	0	0	1	0	0	0	0	0	1	0	0
45	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0
46	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1958	213	513	215	144	239	117	269	248
1	710	123	291	19	129	17	10	99	22	1088	246	280	130	35	71	73	194	59
2	1106	276	232	128	11	163	4	154	138	547	69	75	33	3	121	32	86	128
3	582	188	132	132	4	36	32	34	24	194	33	33	64	0	21	12	25	6
4	437	48	84	144	10	48	26	41	36	151	12	21	50	4	21	13	25	5
5	296	0	16	20	113	44	34	29	40	122	0	4	8	53	16	12	15	14
6	179	0	0	20	26	24	48	18	43	87	0	0	13	20	3	25	8	18
7	141	0	0	12	10	30	36	26	27	51	0	0	5	4	3	19	17	3
8	102	0	0	8	10	20	24	24	16	44	0	0	3	4	2	16	17	2
9	96	0	0	8	10	16	22	24	16	43	0	0	3	4	2	15	17	2
10	100	0	0	12	6	16	22	28	16	43	0	0	2	4	2	15	18	2
11	98	0	0	8	12	16	22	24	16	45	0	0	2	6	2	16	17	2
12	106	0	0	16	4	16	26	28	16	46	0	0	4	4	2	16	18	2
13	99	0	0	16	4	16	23	24	16	42	0	0	5	4	2	12	17	2
14	95	0	0	16	2	16	16	29	16	34	0	0	6	2	2	5	17	2
15	77	0	0	16	0	16	11	26	8	22	0	0	4	0	2	4	12	0
16	54	0	0	8	8	12	9	13	4	14	0	0	1	6	1	3	2	1
17	26	0	0	0	10	4	4	6	2	6	0	0	0	4	0	1	1	0
18	15	0	0	0	8	0	4	3	0	5	0	0	0	2	0	1	2	0
19	16	0	0	0	8	0	4	4	0	4	0	0	0	2	0	1	1	0
20	15	0	0	0	8	0	7	0	0	4	0	0	0	2	0	2	0	0
21	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
22	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
23	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
24	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
25	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
26	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
27	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
28	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
29	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
30	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
31	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
32	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
33	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
34	12	0	0	4	4	0	4	0	0	3	0	0	0	2	0	1	0	0
35	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
36	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
37	12	0	0	0	8	0	4	0	0	3	0	0	0	2	0	1	0	0
38	12	0	0	0	8	0	4	0	0	2	0	0	0	1	0	1	0	0
39	8	0	0	0	0	0	4	0	4	2	0	0	0	0	0	1	0	1
40	8	0	0	0	0	0	4	0	4	1	0	0	0	0	0	1	0	0
41	4	0	0	0	0	0	4	0	0	1	0	0	0	0	0	1	0	0
42	4	0	0	0	0	0	4	0	0	2	0	0	0	0	0	2	0	0
43	8	0	0	0	0	0	8	0	0	3	0	0	0	0	0	3	0	0
44	10	0	0	0	0	3	7	0	0	2	0	0	0	0	0	2	0	0
45	3	0	0	0	0	0	3	0	0	1	0	0	0	0	0	1	0	0
46	4	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	2082	285	441	126	132	106	110	243	94
2	1	0	0	0	1	0	0	0	0	883	132	142	72	6	94	34	87	123
3	31	30	0	0	1	0	0	0	0	482	45	71	133	7	43	22	31	20
4	10	0	0	0	0	2	3	0	5	204	0	3	12	32	32	15	18	25
5	10	0	0	0	0	4	3	0	3	113	0	0	8	5	25	20	14	24
6	10	0	0	0	1	3	3	0	3	103	0	0	12	15	14	13	17	12
7	12	0	0	0	1	5	3	0	3	77	0	0	11	0	14	12	18	12
8	9	0	0	0	1	3	3	0	2	71	0	0	12	2	10	10	18	10
9	7	0	0	0	1	2	2	0	2	71	0	0	12	2	10	12	16	10
10	7	0	0	1	0	2	2	0	2	67	0	0	7	3	10	10	16	10
11	7	0	0	0	1	2	2	0	2	65	0	0	8	4	10	8	14	10
12	7	0	0	1	0	2	2	0	2	68	0	0	7	6	10	10	15	10
13	7	0	0	1	0	2	2	0	2	55	0	0	5	0	10	5	16	6
14	7	0	0	1	0	2	2	0	2	52	0	0	4	8	9	5	11	4
15	8	0	0	1	0	2	3	0	2	24	0	0	3	4	5	1	8	0
16	6	0	0	1	0	2	2	1	0	17	0	0	1	6	1	2	2	1
17	4	0	0	0	1	1	0	1	1	12	0	0	0	8	0	2	1	0
18	1	0	0	0	1	0	0	0	0	8	0	0	0	2	0	1	1	0
19	1	0	0	0	1	0	0	0	0	13	0	0	0	6	0	2	1	0
20	2	0	0	0	1	0	1	0	0	13	0	0	1	6	0	4	0	0
21	1	0	0	0	1	0	0	0	0	5	0	0	0	4	0	1	0	0
22	1	0	0	0	1	0	0	0	0	9	0	0	0	2	0	6	0	0
23	1	0	0	0	1	0	0	0	0	4	0	0	0	2	0	2	0	0
24	1	0	0	0	1	0	0	0	0	5	0	0	0	4	0	1	0	0
25	1	0	0	0	1	0	0	0	0	13	0	0	0	6	0	4	0	0
26	1	0	0	0	1	0	0	0	0	8	0	0	0	2	0	5	0	0
27	1	0	0	0	1	0	0	0	0	9	0	0	0	6	0	1	0	0
28	1	0	0	0	1	0	0	0	0	8	0	0	0	3	0	3	0	0
29	1	0	0	0	1	0	0	0	0	8	0	0	0	2	0	3	0	0
30	1	0	0	0	1	0	0	0	0	8	0	0	1	4	0	2	0	0
31	1	0	0	0	1	0	0	0	0	4	0	0	0	2	0	2	0	0
32	1	0	0	0	1	0	0	0	0	6	0	0	0	4	0	2	0	0
33	1	0	0	0	1	0	0	0	0	5	0	0	0	2	0	2	0	0
34	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0
35	1	0	0	0	1	0	0	0	0	4	0	0	0	2	0	2	0	0
36	1	0	0	0	1	0	0	0	0	7	0	0	0	4	0	2	0	0
37	1	0	0	0	1	0	0	0	0	4	0	0	0	2	0	1	0	1
38	1	0	0	0	1	0	0	0	0	6	0	0	0	0	0	1	0	2
39	0	0	0	0	0	0	0	0	0	5	0	0	0	0	0	2	0	2
40	1	0	0	0	0	0	0	0	1	3	0	0	0	0	0	3	0	0
41	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
42	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	2	0	0
43	0	0	0	0	0	0	0	0	0	3	0	0	0	0	0	3	0	0
44	2	0	0	0	0	1	1	0	0	4	0	0	0	0	2	2	0	0
45	1	0	0	0	0	0	1	0	0	2	0	0	0	0	0	2	0	0
46	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	24	2	3	15	36	30	34	0	0	30	0	7	28	35	36	2	32
1	1	112	55	40	121	42	55	45	75	2082	48	109	59	23	68	32	161	45
2	1	43	22	37	32	42	6	9	2	883	27	66	2	1	13	5	41	38
3	31	18	11	34	30	12	1	1	3	482	10	46	5	1	2	13	2	31
4	10	0	10	33	1	11	5	6	1	204	26	5	1	4	9	14	5	3
5	10	0	0	0	1	1	9	4	2	113	0	3	1	0	2	3	7	1
6	10	0	0	2	3	0	9	3	3	103	0	7	3	2	0	2	5	1
7	12	0	0	0	2	0	5	2	1	77	0	5	2	0	0	1	1	1
8	9	0	0	0	2	0	5	2	0	71	0	5	2	0	0	2	0	0
9	7	0	0	0	2	0	5	2	0	71	0	5	2	0	0	2	0	0
10	7	0	0	1	2	0	6	2	0	67	0	5	2	1	0	2	1	0
11	7	0	0	0	2	0	7	2	0	65	0	5	2	0	1	2	1	0
12	7	0	0	0	3	0	6	1	0	68	0	5	3	0	1	1	0	0
13	7	0	0	2	3	0	6	2	0	55	0	3	3	2	0	2	3	0
14	7	0	0	2	6	0	1	2	0	52	0	0	6	2	0	2	1	0
15	8	0	0	0	0	0	0	3	0	24	0	0	1	0	0	1	0	1
16	6	0	0	0	2	0	1	1	0	17	0	0	3	0	1	0	0	0
17	4	0	0	0	0	0	1	0	0	12	0	0	0	0	1	0	0	0
18	1	0	0	0	4	0	0	0	0	8	0	0	4	0	0	0	0	0
19	1	0	0	0	4	0	0	0	0	13	0	0	4	0	0	0	0	0
20	2	0	0	0	1	0	1	0	0	13	0	0	1	0	1	0	0	0
21	1	0	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0
22	1	0	0	0	0	0	1	0	0	9	0	0	0	0	1	0	0	0
23	1	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
24	1	0	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0
25	1	0	0	0	0	0	3	0	0	13	0	0	0	0	2	0	1	0
26	1	0	0	0	0	0	1	0	0	8	0	0	0	0	1	0	0	0
27	1	0	0	0	2	0	0	0	0	9	0	0	2	0	0	0	0	0
28	1	0	0	1	0	0	1	0	0	8	0	0	0	1	1	0	0	0
29	1	0	0	0	2	0	1	0	0	8	0	0	2	0	0	0	1	0
30	1	0	0	0	1	0	0	0	0	8	0	0	1	0	0	0	0	0
31	1	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
32	1	0	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0
33	1	0	0	0	0	0	1	0	0	5	0	0	0	0	1	0	0	0
34	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
35	1	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
36	1	0	0	0	0	0	1	0	0	7	0	0	0	0	1	0	0	0
37	1	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
38	1	0	0	0	2	0	1	0	0	6	0	0	2	0	1	0	0	0
39	0	0	0	0	0	0	0	0	1	5	0	0	0	0	0	0	1	0
40	1	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0
41	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
42	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
43	0	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0
44	2	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
45	1	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
46	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (172 831 263 44 43 73 35 6 13 6 19 13 14 1 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 1 4 17 10 1 1, 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 1: (30 126 8 5 2 2 2 2 8 2 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 5)
Cluster 2: (0 140 33 13 0 0 0 0 2 0 7 8 8 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 3 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 3: (7 108 66 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4 1 0 0 0 0 0 0 0 1, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1)
Cluster 4: (29 77 79 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (36 101 11 0 14 0 0 1 1 3 2 5 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4 0 0 0 0 0 0 0 1)
Cluster 6: (4 108 41 9 21 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1)
Cluster 7: (32 71 19 15 2 36 27 3 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 4 0 1)
Cluster 8: (34 100 6 0 3 35 6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 3 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	51	28	26	0	0	6	0	26	4	0	0	0	0	0	0
100	0	12	75	37	43	2	0	0	0	0	0	0	0	0	0
0	2	0	108	0	0	3	0	0	0	0	0	0	0	7	0
7	9	15	0	0	2	1	3	0	0	0	3	0	0	23	2
0	36	1	13	0	38	4	15	0	18	2	0	15	0	0	0
0	0	0	1	37	0	27	19	0	0	0	0	0	36	0	0
63	0	29	4	31	53	0	51	0	2	0	0	0	0	0	0
3	0	67	1	3	3	44	0	0	0	0	0	0	0	0	32

img_interp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	3424	513	412	409	408	415	437	410	420
Number of PI	41	9	0	9	5	2	3	13	0
Number of DFF	718	113	77	81	126	74	84	63	100
Number of Combinational Nodes	3383	504	412	400	403	413	434	397	420
Number of PO	193	151	3	0	0	2	1	3	33
Number of Edges	9404	2663	1325	1291	1178	1618	1486	1346	1200
Number of Intra-Cluster Edges	6684	997	929	789	625	887	824	834	751
Number of Inter-Cluster Input Edges	5423	119	315	376	372	393	418	369	293
Number of Inter-Cluster Output Edges	5423	1531	73	125	181	338	244	120	156
Wirelength Approx	5.82e+06	745993	723344	640158	681129	746881	936700	618887	736138
Scaled Cost	1.39								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.7 ± 30	5 ± 77	2.4 ± 2.3	2.2 ± 2.7	1.9 ± 3.7	2.9 ± 16	2.4 ± 10	2.3 ± 2.9	2.1 ± 5
Avg. Comb. Fanout	1.7 ± 5	0.7 ± 0.5	1.9 ± 1.4	1.7 ± 1.9	1.6 ± 3.8	1.6 ± 2.1	2.4 ± 11	1.8 ± 2.0	1.9 ± 5
Avg. PI Fanout	43 ± 267	194 ± 545	N/A	1 ± 0	1 ± 0	1 ± 0	1 ± 0	1 ± 0	N/A
Avg. DFF Fanout	4 ± 13	4 ± 10	5 ± 3.8	4 ± 4	2.8 ± 3.5	9 ± 36	2.3 ± 1.1	5 ± 5	2.8 ± 7
Avg. Comb. Fanin	3.2 ± 0.8	2.6 ± 0.7	3.4 ± 0.7	3.2 ± 0.8	3.3 ± 0.7	3.5 ± 0.6	3.3 ± 0.7	3.3 ± 0.8	3.2 ± 0.8
Max Fanout	1734	1734	19	22	42	314	121	27	73

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	759	122	77	90	131	76	87	76	100	0	0	0	0	0	0	0	0	0
1	985	289	48	124	131	117	74	114	88	190	149	3	0	0	1	1	3	33
2	171	50	17	59	0	24	0	21	0	2	2	0	0	0	0	0	0	0
3	136	15	16	51	0	22	0	32	0	1	0	0	0	0	1	0	0	0
4	113	3	20	34	0	15	2	39	0	0	0	0	0	0	0	0	0	0
5	109	3	19	19	0	18	1	46	3	0	0	0	0	0	0	0	0	0
6	199	6	22	10	1	37	79	43	1	0	0	0	0	0	0	0	0	0
7	130	5	27	8	1	36	35	17	1	0	0	0	0	0	0	0	0	0
8	161	6	32	4	5	23	51	8	32	0	0	0	0	0	0	0	0	0
9	322	3	43	4	96	15	70	6	85	0	0	0	0	0	0	0	0	0
10	119	3	27	2	24	15	20	2	26	0	0	0	0	0	0	0	0	0
11	132	6	24	2	19	9	14	4	54	0	0	0	0	0	0	0	0	0
12	63	2	20	1	0	6	3	2	29	0	0	0	0	0	0	0	0	0
13	17	0	13	0	0	2	1	0	1	0	0	0	0	0	0	0	0	0
14	4	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	2	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	2	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	4789	2225	348	349	358	676	203	349	281
1	2629	698	122	344	379	361	218	301	206	648	116	57	155	1	136	0	129	54
2	605	167	59	209	0	92	0	78	0	324	48	28	129	0	41	0	78	0
3	509	60	61	187	0	85	0	116	0	222	0	34	93	0	27	0	68	0
4	412	9	71	119	0	55	8	150	0	380	4	44	46	0	24	175	87	0
5	393	11	73	61	0	71	4	165	8	333	5	46	20	0	42	118	60	42
6	757	20	86	35	3	142	312	156	3	301	6	40	8	34	75	83	55	0
7	423	16	101	30	4	127	76	66	3	375	9	60	4	24	44	151	21	62
8	614	21	117	16	19	87	204	22	128	534	5	69	4	120	25	141	9	161
9	1134	10	147	16	384	55	215	19	288	355	3	70	3	96	24	70	4	85
10	461	10	103	8	96	58	74	8	104	241	1	49	2	24	20	33	8	104
11	457	12	80	8	38	33	54	16	216	131	0	50	3	0	13	7	4	54
12	204	5	70	4	0	22	12	6	85	38	0	31	0	0	4	3	0	0
13	62	0	49	0	0	8	2	0	3	10	0	10	0	0	0	0	0	0
14	14	0	14	0	0	0	0	0	0	3	0	3	0	0	0	0	0	0
15	8	0	8	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
16	4	0	2	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1	1	0	0	0	0	0	0	0	0	16	8	1	0	0	0	23	0
1	468	73	19	60	130	40	73	42	31	5447	862	515	547	408	562	565	515	485
2	9	0	3	4	0	0	0	2	0	868	62	117	130	25	84	85	122	49
3	37	15	2	5	0	7	0	8	0	385	16	59	55	24	35	2	83	29
4	15	1	2	8	0	3	0	1	0	239	6	22	8	0	25	51	39	5
5	17	0	4	4	0	1	0	6	2	204	9	32	25	0	29	0	44	2
6	31	2	2	4	0	5	0	17	1	366	8	25	15	0	45	41	19	3
7	14	1	3	6	0	2	0	2	0	124	6	41	2	0	30	0	0	0
8	15	2	6	2	0	5	0	0	0	213	11	32	3	0	23	0	4	0
9	12	1	4	2	0	3	0	2	0	499	5	43	0	168	18	80	8	100
10	9	2	4	1	0	2	0	0	0	115	4	16	0	0	18	0	0	50
11	41	6	4	0	19	2	10	0	0	149	6	17	4	0	14	0	0	26
12	38	2	2	1	0	2	0	2	29	56	2	6	0	0	4	0	0	1
13	7	0	3	0	0	2	1	0	1	15	0	3	0	0	0	0	0	1
14	2	0	2	0	0	0	0	0	0	4	0	1	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	2	0	1	1	0	0	0	0	0	2	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1	77	81	126	74	84	63	100	0	0	106	61	98	149	74	84	82	64
1	468	32	39	116	218	151	148	120	164	5447	592	10	14	14	205	108	16	29
2	9	1	16	68	26	32	9	30	12	868	92	1	1	18	13	39	6	24
3	37	1	9	20	0	18	3	27	4	385	60	0	0	0	7	3	4	8
4	15	0	14	19	5	11	12	19	3	239	62	0	0	0	1	9	0	11
5	17	0	14	6	0	14	0	24	5	204	55	0	0	0	5	1	2	0
6	31	4	18	3	1	35	112	36	1	366	159	1	8	0	26	0	6	10
7	14	4	19	7	0	11	0	2	2	124	39	0	4	0	0	0	2	0
8	15	0	26	4	5	17	51	2	35	213	135	0	0	0	3	0	0	2
9	12	0	33	3	24	5	0	1	11	499	71	0	0	0	4	0	2	0
10	9	0	13	2	0	10	0	2	0	115	25	0	0	0	0	0	0	2
11	41	0	10	1	19	4	18	4	26	149	76	0	0	0	0	0	0	6
12	38	0	10	0	0	0	2	2	29	56	43	0	0	0	0	0	0	0
13	7	0	9	0	0	1	0	0	1	15	11	0	0	0	0	0	0	0
14	2	0	3	0	0	0	0	0	0	4	3	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	2	0	1	1	0	0	0	0	0	2	2	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (851 1488 436 266 132 62 29 28 33 13 15 8 10 6 3 2 5 4 1 6 0 1 1 0 9 0 0 1 0 0 0 0 1 0 1,
0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0,
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Cluster 1: (224 173 48 12 52 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0,
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Cluster 2: (59 140 84 52 22 21 13 7 7 1 0 0 2 0 0 1 1 0 1 1)
Cluster 3: (87 185 63 12 14 10 5 9 7 3 3 4 0 3 0 0 1 1 0 1 0 0 1)
Cluster 4: (149 134 48 69 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0,
0 0 1)
Cluster 5: (75 231 45 9 2 11 6 4 9 2 7 1 3 1 1 0 2 3 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (85 243 50 40 2 0 2 0 5 0 1 0 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 7: (78 166 73 29 14 19 3 8 5 2 4 3 0 2 0 0 1 0 0 0 0 0 0 0 0 2 0 0 1)
Cluster 8: (94 216 25 43 26 1 0 0 0 5 0 0 0 0 2 1 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	232	216	180	221	223	191	162	79	16	1	0	1	0	4	5
11	0	1	0	0	0	0	0	0	53	8	0	0	0	0	0
14	2	0	0	0	6	5	0	4	8	72	1	2	1	5	5
5	0	10	0	1	12	0	4	19	0	0	125	0	5	0	0
4	0	17	77	0	85	31	50	0	0	0	0	70	0	0	4
2	0	0	16	58	0	22	62	10	0	0	0	0	74	0	0
4	0	6	0	5	8	0	15	0	0	0	0	1	4	54	23
2	0	0	25	24	21	20	0	1	0	0	0	0	0	0	63

incmod

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1007	105	122	119	128	131	138	132	132
Number of PI	150	20	22	24	15	41	22	5	1
Number of DFF	72	0	2	2	0	2	2	4	60
Number of Combinational Nodes	857	85	100	95	113	90	116	127	131
Number of PO	68	0	0	2	1	8	15	41	1
Number of Edges	2846	345	399	461	541	371	507	608	386
Number of Intra-Cluster Edges	2078	210	285	272	303	213	286	261	246
Number of Inter-Cluster Input Edges	1540	85	59	50	82	100	152	226	16
Number of Inter-Cluster Output Edges	1540	50	53	139	156	58	69	121	124
Wirelength Approx	537063	57271	61977	67920	77890	59864	87229	76128	48784
Scaled Cost	1.60								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.8 ± 6	2.4 ± 1.8	2.7 ± 2.6	3.4 ± 6	3.5 ± 7	2.0 ± 3.9	2.5 ± 7	2.8 ± 11	2.8 ± 5
Avg. Comb. Fanout	2.3 ± 7	1.7 ± 0.8	1.6 ± 1.1	2.8 ± 6	3.3 ± 8	1.6 ± 0.6	1.9 ± 6	2.7 ± 11	2.6 ± 7
Avg. PI Fanout	4 ± 2.6	6 ± 1.7	7 ± 2.5	6 ± 1.7	6 ± 0.9	1.4 ± 0.8	2.8 ± 0.4	7 ± 1.9	3 ± 0
Avg. DFF Fanout	5 ± 7	N/A	7 ± 0	6 ± 1.5	N/A	33 ± 0	33 ± 0	1 ± 0	2.9 ± 1.1
Avg. Comb. Fanin	3.5 ± 0.7	3.4 ± 0.7	3.4 ± 0.7	3.4 ± 0.7	3.3 ± 0.8	3.5 ± 0.4	3.8 ± 0.3	3.4 ± 0.8	3.6 ± 0.7
Max Fanout	66	8	12	33	56	33	65	66	36

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	222	20	24	26	15	43	24	9	61	1	0	0	0	0	0	0	0	1
1	98	5	18	2	3	42	23	5	0	0	0	0	0	0	0	0	0	0
2	23	2	13	2	0	0	3	0	3	0	0	0	0	0	0	0	0	0
3	50	11	14	15	4	0	3	0	3	1	0	0	0	0	0	1	0	0
4	106	11	11	15	4	0	2	0	63	0	0	0	0	0	0	0	0	0
5	38	10	9	7	10	0	2	0	0	0	0	0	0	0	0	0	0	0
6	8	6	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
7	7	5	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
8	7	4	0	0	1	0	2	0	0	0	0	0	0	0	0	0	0	0
9	6	2	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
10	6	2	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
11	6	2	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
12	6	2	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
13	6	2	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0
14	6	0	2	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0
15	6	0	2	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0
16	6	0	2	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0
17	5	0	1	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0
18	5	0	1	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0
19	6	0	0	0	4	0	2	0	0	0	0	0	0	0	0	0	0	0
20	6	0	0	0	4	0	2	0	0	0	0	0	0	0	0	0	0	0
21	6	0	0	0	4	0	2	0	0	0	0	0	0	0	0	0	0	0
22	6	0	0	0	4	1	1	0	0	0	0	0	0	0	0	0	0	0
23	6	0	0	1	3	2	0	0	0	0	0	0	0	0	0	0	0	0
24	6	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
25	6	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
26	6	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
27	6	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
28	6	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0	0	0
29	6	0	0	3	1	2	0	0	0	0	0	0	0	0	0	0	0	0
30	7	0	0	5	0	2	0	0	0	0	0	0	0	0	0	0	0	0
31	6	0	0	4	0	2	0	0	0	1	0	0	1	0	0	0	0	0
32	4	0	0	2	0	2	0	0	0	0	0	0	0	0	0	0	0	0
33	4	0	0	2	1	1	0	0	0	0	0	0	0	0	0	0	0	0
34	2	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
35	2	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36	2	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
37	5	0	0	2	3	0	0	0	0	2	0	0	1	1	0	0	0	0
38	6	0	1	0	1	0	0	2	2	0	0	0	0	0	0	0	0	0
39	67	0	0	0	2	16	34	15	0	0	0	0	0	0	0	0	0	0
40	62	6	4	6	15	8	14	9	0	31	0	0	0	0	8	14	9	0
41	33	7	6	6	14	0	0	0	0	0	0	0	0	0	0	0	0	0
42	33	7	4	6	14	0	0	2	0	0	0	0	0	0	0	0	0	0
43	58	1	0	0	0	0	0	57	0	1	0	0	0	0	0	0	1	0
44	31	0	0	0	0	0	0	31	0	29	0	0	0	0	0	0	29	0
45	2	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0	2	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	988	110	172	147	85	127	129	38	180
1	328	18	46	6	10	138	91	19	0	495	10	47	34	68	84	109	143	0
2	87	6	52	8	0	0	11	0	10	127	3	18	64	0	0	5	0	37
3	193	41	56	58	16	0	10	0	12	170	15	15	44	4	0	4	0	88
4	399	41	44	59	16	0	7	0	232	54	18	10	17	4	0	4	0	1
5	91	22	28	14	20	0	7	0	0	102	32	15	21	30	0	4	0	0
6	29	22	0	0	0	0	7	0	0	13	9	0	0	0	0	4	0	0
7	25	18	0	0	0	0	7	0	0	12	8	0	0	0	0	4	0	0
8	24	14	0	0	3	0	7	0	0	15	7	0	0	4	0	4	0	0
9	21	8	6	0	0	0	7	0	0	11	4	3	0	0	0	4	0	0
10	21	8	6	0	0	0	7	0	0	11	4	3	0	0	0	4	0	0
11	21	8	6	0	0	0	7	0	0	11	4	3	0	0	0	4	0	0
12	21	8	6	0	0	0	7	0	0	11	4	3	0	0	0	4	0	0
13	21	8	6	0	0	0	7	0	0	11	4	3	0	0	0	4	0	0
14	21	0	8	0	6	0	7	0	0	11	0	4	0	3	0	4	0	0
15	21	0	8	0	6	0	7	0	0	11	0	4	0	3	0	4	0	0
16	21	0	8	0	6	0	7	0	0	12	0	5	0	3	0	4	0	0
17	17	0	4	0	6	0	7	0	0	10	0	3	0	3	0	4	0	0
18	17	0	4	0	6	0	7	0	0	9	0	2	0	3	0	4	0	0
19	21	0	0	0	14	0	7	0	0	11	0	0	0	7	0	4	0	0
20	21	0	0	0	14	0	7	0	0	11	0	0	0	7	0	4	0	0
21	21	0	0	0	14	0	7	0	0	11	0	0	0	7	0	4	0	0
22	21	0	0	0	14	3	4	0	0	11	0	0	0	7	2	2	0	0
23	21	0	0	3	11	7	0	0	0	11	0	0	2	5	4	0	0	0
24	21	0	0	6	8	7	0	0	0	11	0	0	3	4	4	0	0	0
25	21	0	0	6	8	7	0	0	0	11	0	0	3	4	4	0	0	0
26	21	0	0	6	8	7	0	0	0	11	0	0	3	4	4	0	0	0
27	21	0	0	6	8	7	0	0	0	11	0	0	3	4	4	0	0	0
28	21	0	0	6	8	7	0	0	0	11	0	0	3	4	4	0	0	0
29	21	0	0	10	4	7	0	0	0	12	0	0	6	2	4	0	0	0
30	24	0	0	17	0	7	0	0	0	11	0	0	7	0	4	0	0	0
31	21	0	0	14	0	7	0	0	0	10	0	0	6	0	4	0	0	0
32	15	0	0	8	0	7	0	0	0	8	0	0	4	0	4	0	0	0
33	15	0	0	8	3	4	0	0	0	11	0	0	4	5	2	0	0	0
34	8	0	0	8	0	0	0	0	0	4	0	0	4	0	0	0	0	0
35	8	0	0	8	0	0	0	0	0	4	0	0	4	0	0	0	0	0
36	8	0	0	4	4	0	0	0	0	7	0	0	4	3	0	0	0	0
37	19	0	0	7	12	0	0	0	0	37	0	0	4	33	0	0	0	0
38	22	0	4	0	4	0	0	6	8	129	0	1	0	2	0	0	126	0
39	268	0	0	0	8	64	136	60	0	129	0	0	0	64	16	34	15	0
40	248	24	16	24	60	32	56	36	0	62	6	4	6	46	0	0	0	0
41	132	28	24	24	56	0	0	0	0	34	7	7	6	14	0	0	0	0
42	76	16	10	12	30	0	0	8	0	62	13	8	12	27	0	0	2	0
43	231	3	0	0	0	0	0	228	0	58	2	0	0	0	0	0	56	0
44	66	0	0	0	0	0	0	66	0	2	0	0	0	0	0	0	2	0
45	4	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1143	67	125	83	89	140	137	104	93
2	0	0	0	0	0	0	0	0	0	244	23	44	48	30	0	4	3	32
3	1	0	1	0	0	0	0	0	0	130	23	25	28	23	0	3	0	0
4	65	0	3	0	0	0	0	0	62	215	23	20	24	10	0	3	3	116
5	4	0	4	0	0	0	0	0	0	87	10	9	3	0	0	3	57	0
6	0	0	0	0	0	0	0	0	0	27	8	0	3	2	0	3	3	0
7	0	0	0	0	0	0	0	0	0	19	8	0	2	0	1	3	0	0
8	0	0	0	0	0	0	0	0	0	17	6	0	2	0	2	3	0	0
9	0	0	0	0	0	0	0	0	0	21	4	6	2	0	1	3	0	0
10	0	0	0	0	0	0	0	0	0	22	4	6	2	0	1	3	0	0
11	0	0	0	0	0	0	0	0	0	20	2	6	2	1	1	3	0	0
12	0	0	0	0	0	0	0	0	0	19	4	5	1	2	1	3	0	0
13	0	0	0	0	0	0	0	0	0	16	0	4	1	2	2	3	0	0
14	0	0	0	0	0	0	0	0	0	21	0	3	1	8	2	3	0	0
15	0	0	0	0	0	0	0	0	0	21	0	3	1	8	2	3	0	0
16	0	0	0	0	0	0	0	0	0	19	0	2	0	8	2	3	0	0
17	0	0	0	0	0	0	0	0	0	18	0	2	0	9	0	4	0	0
18	0	0	0	0	0	0	0	0	0	18	0	0	0	11	0	5	0	0
19	0	0	0	0	0	0	0	0	0	20	0	0	0	11	0	5	0	0
20	0	0	0	0	0	0	0	0	0	20	0	0	0	11	0	7	0	0
21	0	0	0	0	0	0	0	0	0	20	0	0	0	11	1	4	0	0
22	0	0	0	0	0	0	0	0	0	20	0	1	0	10	4	1	0	0
23	0	0	0	0	0	0	0	0	0	18	0	0	1	8	4	2	0	0
24	0	0	0	0	0	0	0	0	0	23	0	5	5	5	4	2	0	0
25	0	0	0	0	0	0	0	0	0	20	0	2	6	5	4	2	0	0
26	0	0	0	0	0	0	0	0	0	20	0	1	6	5	4	1	0	0
27	0	0	0	0	0	0	0	0	0	20	1	0	6	4	4	2	0	0
28	0	0	0	0	0	0	0	0	0	19	1	0	6	3	4	2	0	0
29	0	0	0	0	0	0	0	0	0	24	2	2	7	3	4	2	0	0
30	0	0	0	0	0	0	0	0	0	21	2	0	10	0	4	2	0	0
31	0	0	0	0	0	0	0	0	0	18	2	1	6	0	4	1	0	0
32	0	0	0	0	0	0	0	0	0	17	2	1	3	1	2	1	0	0
33	0	0	0	0	0	0	0	0	0	10	2	1	2	0	0	1	0	0
34	0	0	0	0	0	0	0	0	0	8	0	0	2	0	0	1	0	1
35	0	0	0	0	0	0	0	0	0	10	1	1	2	1	0	2	0	1
36	0	0	0	0	0	0	0	0	0	44	7	6	7	14	0	2	0	2
37	0	0	0	0	0	0	0	0	0	14	3	1	0	2	0	1	4	0
38	2	0	0	0	0	0	0	0	2	71	1	1	0	4	0	20	11	1
39	0	0	0	0	0	0	0	0	0	104	1	2	0	2	15	33	11	0
40	0	0	0	0	0	0	0	0	0	33	1	0	0	0	0	0	4	0
41	0	0	0	0	0	0	0	0	0	3	0	0	0	0	0	0	2	0
42	0	0	0	0	0	0	0	0	0	61	2	0	0	0	0	0	57	0
43	0	0	0	0	0	0	0	0	0	57	0	0	0	0	0	0	2	0
44	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	2	2	0	2	2	4	60	0	0	0	8	0	0	0	0	0	64
1	0	36	25	15	31	52	66	71	9	1143	29	28	66	76	5	29	72	0
2	0	23	14	5	14	0	4	0	0	244	0	0	39	17	2	0	1	1
3	1	10	4	6	0	0	2	0	6	130	0	7	2	16	2	1	0	0
4	65	0	5	8	1	0	2	0	0	215	2	2	1	7	3	1	0	0
5	4	0	2	0	1	0	2	0	0	87	1	0	1	0	3	0	0	0
6	0	3	0	0	1	0	2	2	0	27	0	0	1	3	4	0	0	0
7	0	2	0	0	0	0	2	1	0	19	0	0	0	2	3	0	0	0
8	0	2	0	0	0	0	2	0	0	17	0	0	0	2	2	0	0	0
9	0	2	0	0	0	0	2	1	0	21	0	0	0	2	3	0	0	0
10	0	2	0	0	1	0	2	1	0	22	0	0	1	2	3	0	0	0
11	0	2	0	0	0	0	2	1	0	20	0	0	0	2	3	0	0	0
12	0	0	0	0	0	0	2	1	0	19	0	0	0	0	3	0	0	0
13	0	0	2	0	0	0	2	0	0	16	0	0	0	2	2	0	0	0
14	0	0	2	0	0	0	2	0	0	21	0	0	0	2	2	0	0	0
15	0	0	2	0	0	0	2	0	0	21	0	0	0	2	2	0	0	0
16	0	0	1	0	1	0	2	0	0	19	0	0	1	1	2	0	0	0
17	0	0	0	0	0	1	2	0	0	18	0	0	0	0	2	1	0	0
18	0	0	0	0	0	0	2	0	0	18	0	0	0	0	2	0	0	0
19	0	0	0	0	2	0	2	0	0	20	0	0	2	0	2	0	0	0
20	0	0	0	0	2	0	0	0	0	20	0	0	2	0	0	0	0	0
21	0	0	0	0	2	1	1	0	0	20	0	0	2	0	1	1	0	0
22	0	0	0	0	2	1	0	1	0	20	0	0	2	0	0	2	0	0
23	0	0	0	1	1	1	0	0	0	18	0	0	1	1	0	1	0	0
24	0	0	0	0	1	1	0	0	0	23	0	0	1	0	0	1	0	0
25	0	0	0	0	0	1	0	0	0	20	0	0	0	0	0	1	0	0
26	0	1	0	0	0	1	0	1	0	20	0	1	0	0	0	2	0	0
27	0	0	0	0	2	1	0	0	0	20	1	1	0	0	0	1	0	0
28	0	0	0	1	1	1	0	0	0	19	1	0	0	1	0	1	0	0
29	0	0	0	2	1	1	0	0	0	24	0	0	1	2	0	1	0	0
30	0	0	0	2	0	1	0	0	0	21	0	0	0	2	0	1	0	0
31	0	0	0	2	0	1	0	1	0	18	0	0	0	2	0	2	0	0
32	0	0	0	2	3	1	0	1	0	17	0	0	1	2	2	2	0	0
33	0	0	0	2	1	0	0	1	0	10	1	0	0	2	0	1	0	0
34	0	0	0	2	1	0	0	1	0	8	1	0	0	2	0	1	0	0
35	0	0	0	1	1	0	0	0	0	10	1	0	0	1	0	0	0	0
36	0	0	0	1	5	0	0	0	0	44	2	0	2	0	0	0	2	0
37	0	0	0	0	2	0	0	0	1	14	0	1	1	0	0	0	1	0
38	2	0	0	0	0	16	14	3	0	71	0	0	0	0	0	11	22	0
39	0	0	0	0	1	9	15	15	0	104	2	0	2	0	5	7	22	2
40	0	0	0	0	1	8	14	5	0	33	0	0	0	0	0	1	0	27
41	0	0	0	0	1	0	0	0	0	3	0	0	0	0	0	0	1	0
42	0	0	0	0	0	0	0	2	0	61	0	1	0	0	0	0	0	1
43	0	0	0	0	0	0	0	55	0	57	8	4	10	5	0	0	0	28
44	0	0	0	0	0	0	0	2	0	2	1	0	0	0	0	0	0	1
45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (138 356 290 67 48 32 4 37 8 1 0 2 2 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 2 2 3 6 0 0 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 2 0 1 2)
Cluster 1: (0 39 37 4 9 7 0 8 1)
Cluster 2: (8 50 27 8 3 7 1 10 3 1 0 2 2)
Cluster 3: (1 49 32 9 3 7 1 12 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1)
Cluster 4: (1 48 44 11 1 11 2 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (8 47 64 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 6: (15 36 64 20 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (41 80 0 2 0 0 0 2 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 2)
Cluster 8: (64 7 22 3 32 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	4	1	11	1	9	24	0	0	0	0	0	0	0	0	0
8	0	2	7	0	5	15	8	0	2	2	0	2	2	0	0
35	21	0	47	8	0	26	2	0	0	0	0	0	0	0	0
40	28	46	0	3	7	32	0	0	0	0	0	0	0	0	0
0	2	0	3	0	42	11	0	0	0	0	0	0	0	0	0
0	2	0	1	45	0	21	0	0	0	0	0	0	0	0	0
0	0	1	11	33	70	0	6	0	0	0	0	0	0	0	0
0	0	0	0	8	15	37	0	0	0	0	0	0	0	4	60

input_chip

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1104	134	144	134	133	153	121	133	152
Number of PI	33	4	0	0	0	15	2	10	2
Number of DFF	291	51	27	37	42	39	24	43	28
Number of Combinational Nodes	1071	130	144	134	133	138	119	123	150
Number of PO	35	21	0	0	0	8	5	0	1
Number of Edges	2911	319	493	442	442	394	410	342	927
Number of Intra-Cluster Edges	2008	151	333	216	216	266	244	179	400
Number of Inter-Cluster Input Edges	1761	114	113	154	136	94	121	104	19
Number of Inter-Cluster Output Edges	1761	54	46	70	90	34	45	59	508
Wirelength Approx	452466	38321	65533	57160	59765	57982	62237	45871	65597
Scaled Cost	1.32								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.6 ± 17	1.5 ± 2.2	2.6 ± 2.5	2.1 ± 3.3	2.3 ± 3.4	1.9 ± 3.5	2.3 ± 3.0	1.7 ± 1.4	6 ± 45
Avg. Comb. Fanout	1.5 ± 1.7	0.8 ± 0.7	1.5 ± 0.9	1.7 ± 2.4	1.6 ± 2.6	1.5 ± 1.4	1.6 ± 1.8	1.3 ± 0.9	1.6 ± 1.4
Avg. PI Fanout	19 ± 95	2 ± 1.2	N/A	N/A	N/A	2.6 ± 1.3	1.5 ± 0.5	1 ± 0	282 ± 276
Avg. DFF Fanout	3.7 ± 4	2.5 ± 3.2	7 ± 1.7	3.1 ± 5	3.7 ± 4	2.7 ± 7	6 ± 5	2.7 ± 1.8	5 ± 3.2
Avg. Comb. Fanin	3.3 ± 0.8	3.0 ± 0.9	3.4 ± 0.6	3.3 ± 0.8	3.4 ± 0.7	3.3 ± 0.8	3.3 ± 0.8	3.1 ± 0.8	3.4 ± 0.8
Max Fanout	558	18	12	28	27	42	18	8	558

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	324	55	27	37	42	54	26	53	30	0	0	0	0	0	0	0	0	0
1	350	68	53	30	33	48	38	40	40	35	21	0	0	0	8	5	0	1
2	111	2	24	15	6	24	18	8	14	0	0	0	0	0	0	0	0	0
3	137	5	22	28	26	6	12	10	28	0	0	0	0	0	0	0	0	0
4	97	3	15	24	25	5	3	11	11	0	0	0	0	0	0	0	0	0
5	18	1	3	0	1	3	0	5	5	0	0	0	0	0	0	0	0	0
6	8	0	0	0	0	2	3	2	1	0	0	0	0	0	0	0	0	0
7	15	0	0	0	0	3	9	2	1	0	0	0	0	0	0	0	0	0
8	22	0	0	0	0	8	10	2	2	0	0	0	0	0	0	0	0	0
9	5	0	0	0	0	0	2	0	3	0	0	0	0	0	0	0	0	0
10	3	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0
11	5	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0	0
12	5	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0	0
13	3	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0
14	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1724	137	199	115	158	145	137	129	704
1	1076	197	188	86	99	158	120	108	120	305	11	60	48	22	63	37	23	41
2	390	8	80	60	24	76	67	28	47	272	8	40	59	58	26	20	11	50
3	489	18	80	100	87	24	36	40	104	164	8	36	26	24	13	9	16	32
4	352	12	50	82	100	16	9	39	44	37	3	9	0	1	9	3	7	5
5	61	3	11	0	3	12	0	16	16	12	0	6	0	0	3	0	2	1
6	30	0	0	0	0	6	12	8	4	36	0	0	0	0	6	27	2	1
7	59	0	0	0	0	12	35	8	4	29	0	0	0	0	8	17	2	2
8	82	0	0	0	0	32	35	8	7	10	0	0	0	0	0	4	0	6
9	20	0	0	0	0	0	8	0	12	5	0	0	0	0	0	0	0	5
10	11	0	0	0	0	0	0	0	11	8	0	0	0	0	0	0	0	8
11	16	0	0	0	0	0	0	0	16	9	0	0	0	0	0	0	0	9
12	19	0	0	0	0	0	0	0	19	8	0	0	0	0	0	0	0	8
13	11	0	0	0	0	0	0	0	11	1	0	0	0	0	0	0	0	1
14	4	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	1	2	0	0	0	0	0
1	145	37	11	11	15	17	15	26	13	1750	141	269	151	116	210	167	116	232
2	20	0	5	1	1	0	8	4	1	358	6	36	45	50	34	39	15	60
3	22	0	6	2	2	0	3	3	6	210	4	17	14	26	1	14	20	43
4	65	0	6	24	24	0	0	5	6	158	0	11	6	24	2	5	12	17
5	11	1	1	0	1	0	0	4	4	25	0	0	0	0	0	5	4	7
6	1	0	0	0	0	0	0	1	0	24	0	0	0	0	9	4	4	4
7	3	0	0	0	0	2	0	1	0	36	0	0	0	0	10	2	4	13
8	17	0	0	0	0	8	7	2	0	33	0	0	0	0	0	8	4	3
9	2	0	0	0	0	0	2	0	0	6	0	0	0	0	0	0	0	3
10	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	2
11	1	0	0	0	0	0	0	0	1	10	0	0	0	0	0	0	0	8
12	1	0	0	0	0	0	0	0	1	5	0	0	0	0	0	0	0	5
13	2	0	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0	2
14	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	27	37	42	39	24	43	28	0	0	38	29	38	43	27	35	46	35
1	145	77	40	36	52	48	43	41	11	1750	11	17	16	12	6	5	11	270
2	20	4	20	13	7	4	15	8	2	358	0	0	6	9	1	0	2	55
3	22	1	9	29	11	3	8	10	0	210	3	0	8	16	0	0	0	44
4	65	4	7	34	26	3	0	6	1	158	0	0	2	10	0	1	0	68
5	11	1	0	0	1	0	0	5	2	25	0	0	0	0	0	2	0	7
6	1	0	0	0	0	1	0	2	0	24	0	0	0	0	0	0	0	3
7	3	0	0	0	0	3	2	2	0	36	0	0	0	0	0	1	0	6
8	17	0	0	0	0	8	8	2	0	33	0	0	0	0	0	0	0	18
9	2	0	0	0	0	0	2	0	1	6	0	0	0	0	0	1	0	2
10	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
11	1	0	0	0	0	0	0	0	2	10	2	0	0	0	0	0	0	0
12	1	0	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0
13	2	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
14	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (312 452 113 65 25 30 35 17 25 9 5 2 1 0 1 1 2 3 2 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (59 39 23 2 7 0 1 1 0 0 0 0 0 0 0 0 0 1 1)
Cluster 2: (27 55 20 8 3 8 4 7 8 1 1 1 1)
Cluster 3: (37 75 3 0 0 1 7 1 4 3 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (42 65 0 1 0 8 9 1 3 0 1 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (29 68 28 20 3 0 0 1 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 6: (38 46 9 5 4 7 1 1 2 4 1 0 0 0 1 0 0 1 1)
Cluster 7: (46 39 22 15 3 2 2 2 2)
Cluster 8: (34 65 8 14 5 4 11 3 5 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	0	4	6	0	4	0	2	37	0	1	0	0	0	0	0
3	0	1	7	0	6	0	0	0	27	1	1	0	0	0	0
10	3	0	19	0	0	0	0	6	0	30	2	0	0	0	0
8	3	36	0	0	0	0	0	6	0	0	37	0	0	0	0
0	0	0	0	0	5	1	1	0	0	0	0	27	0	0	0
1	0	0	0	5	0	0	4	0	0	0	0	12	23	0	0
0	0	1	0	0	0	0	12	0	0	2	1	0	0	43	0
65	70	70	65	65	63	75	0	2	0	3	1	0	1	0	28

mantissa_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1284	158	158	174	157	157	143	158	179
Number of PI	246	59	56	2	40	28	15	31	15
Number of DFF	192	2	0	54	10	29	38	12	47
Number of Combinational Nodes	1038	99	102	172	117	129	128	127	164
Number of PO	228	2	0	54	10	30	39	13	80
Number of Edges	3384	509	565	550	523	529	459	606	587
Number of Intra-Cluster Edges	2438	256	310	351	231	302	264	292	432
Number of Inter-Cluster Input Edges	1890	118	138	109	190	82	92	187	28
Number of Inter-Cluster Output Edges	1890	135	117	90	102	145	103	127	127
Wirelength Approx	557439	57976	69831	92011	64474	57106	58715	70993	86333
Scaled Cost	1.43								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.6 ± 5	2.4 ± 5	2.7 ± 4	2.5 ± 8	2.1 ± 4	2.8 ± 4	2.5 ± 5	2.6 ± 5	3.1 ± 5
Avg. Comb. Fanout	2.4 ± 6	2.6 ± 6	2.5 ± 6	2.9 ± 10	2.5 ± 5	2.2 ± 5	2.3 ± 7	2.4 ± 6	1.7 ± 6
Avg. PI Fanout	2.8 ± 3.1	2.1 ± 1.0	2.9 ± 1.0	18 ± 15	1.3 ± 0.5	5 ± 2.5	2.5 ± 1.5	2.8 ± 1.2	4 ± 8
Avg. DFF Fanout	3.2 ± 2.0	3.5 ± 2.5	N/A	1 ± 0	1.3 ± 0.9	2.9 ± 0.3	3.0 ± 0.2	5 ± 0.5	6 ± 1.0
Avg. Comb. Fanin	3.7 ± 0.5	3.8 ± 0.4	3.8 ± 0.4	3.8 ± 0.4	3.6 ± 0.5	3.4 ± 0.8	3.8 ± 0.5	3.7 ± 0.6	3.9 ± 0.3
Max Fanout	64	32	32	64	32	32	54	34	34

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	438	61	56	56	50	57	53	43	62	192	2	0	54	10	29	38	12	47
1	48	2	0	0	0	13	11	4	18	0	0	0	0	0	0	0	0	0
2	97	7	3	0	2	10	6	3	66	0	0	0	0	0	0	0	0	0
3	157	24	9	2	31	47	7	4	33	36	0	0	0	0	1	1	1	33
4	135	18	38	3	21	29	15	11	0	0	0	0	0	0	0	0	0	0
5	109	33	24	0	8	1	21	22	0	0	0	0	0	0	0	0	0	0
6	77	1	25	7	21	0	21	2	0	0	0	0	0	0	0	0	0	0
7	96	1	0	53	9	0	3	30	0	0	0	0	0	0	0	0	0	0
8	63	1	0	31	1	0	3	27	0	0	0	0	0	0	0	0	0	0
9	43	10	3	8	7	0	3	12	0	0	0	0	0	0	0	0	0	0
10	21	0	0	14	7	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1327	134	166	89	65	223	155	142	353
1	173	6	0	0	0	46	43	14	64	253	3	0	0	0	79	26	5	140
2	388	28	12	0	8	40	24	12	264	426	102	51	0	64	69	38	36	66
3	616	96	32	8	122	188	26	12	132	414	35	89	69	81	46	59	35	0
4	482	71	152	9	84	69	53	44	0	334	49	38	160	21	1	21	44	0
5	432	132	95	0	32	3	84	86	0	141	44	44	0	9	0	21	23	0
6	275	3	94	23	63	0	84	8	0	118	2	29	12	42	0	0	33	0
7	382	4	0	212	36	0	12	118	0	115	1	0	52	9	0	3	50	0
8	252	4	0	124	4	0	12	108	0	43	2	0	0	2	0	6	33	0
9	129	30	9	32	22	0	6	30	0	21	8	3	0	4	0	0	6	0
10	63	0	0	42	21	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1224	94	120	47	115	162	124	145	230
2	0	0	0	0	0	0	0	0	0	517	34	30	12	38	77	42	16	178
3	0	0	0	0	0	0	0	0	0	572	69	24	119	65	59	29	57	24
4	42	0	0	0	0	28	14	0	0	333	25	80	3	3	3	35	36	0
5	2	0	0	0	1	1	0	0	0	254	32	20	70	0	1	25	18	0
6	52	1	4	5	21	0	21	0	0	101	0	36	16	0	0	0	4	0
7	1	0	0	1	0	0	0	0	0	128	1	0	53	9	0	6	11	0
8	31	0	0	31	0	0	0	0	0	63	1	0	31	1	0	3	5	0
9	43	10	3	8	7	0	3	12	0	0	0	0	0	0	0	0	0	0
10	21	0	0	14	7	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	54	10	29	38	12	47	0	0	11	7	59	36	29	38	12	0
1	0	31	18	74	42	1	13	5	3	1224	31	39	1	47	14	16	37	2
2	0	8	35	13	12	0	5	0	17	517	42	9	0	6	8	3	22	0
3	0	22	4	0	43	35	7	7	8	572	5	36	20	3	5	5	29	23
4	42	22	20	12	47	8	14	25	0	333	36	9	0	0	32	4	17	50
5	2	34	1	0	9	0	17	27	0	254	10	1	3	0	23	32	4	15
6	52	1	6	0	8	0	24	6	0	101	0	11	7	6	0	0	6	15
7	1	0	0	0	0	0	0	48	0	128	0	3	0	1	21	1	0	22
8	31	0	0	0	0	0	0	22	0	63	0	2	0	3	13	4	0	0
9	43	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (175 673 183 82 39 46 16 24 1 1 0 1 4 2 1 0 1 0 0 1 2 3 0 2 0 0 0 0 0 0 0 3 16 1 3 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 2)
Cluster 1: (2 80 66 1 0 0 3 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4)
Cluster 2: (0 90 32 6 20 0 3 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 1 0 0 0 0 0 0 0 1 1)
Cluster 3: (54 108 5 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 1 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 4: (10 108 33 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 3)
Cluster 5: (30 62 1 36 2 15 1 1 0 1 0 0 3 0 1 0 1 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 6: (39 47 10 35 4 4 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (7 94 28 2 10 12 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 3 0 1)
Cluster 8: (33 84 8 0 2 15 9 22 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 2 0 1)

Inter-Cluster Connectivity Matricies																
Comb								Latched								
0	39	26	28	1	3	24	3	2	0	0	0	0	0	0	0	9
26	0	15	44	3	3	19	0	0	0	0	0	0	0	0	0	7
4	0	0	27	0	0	0	0	0	0	54	0	0	0	0	0	5
7	13	40	0	1	0	4	1	0	0	0	10	0	0	0	0	26
7	13	6	25	0	29	36	0	0	0	0	0	29	0	0	0	0
35	3	3	7	4	0	8	5	0	0	0	0	0	38	0	0	0
32	11	9	11	7	26	0	19	0	0	0	0	0	0	0	12	0
7	5	0	19	28	19	49	0	0	0	0	0	0	0	0	0	0

misex3

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1411	164	165	165	182	166	164	196	209
Number of PI	14	0	0	0	5	0	0	4	5
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1397	164	165	165	177	166	164	192	204
Number of PO	14	1	2	2	1	4	4	0	0
Number of Edges	4954	708	734	680	1007	690	682	1085	1307
Number of Intra-Cluster Edges	3015	333	340	307	437	309	318	466	505
Number of Inter-Cluster Input Edges	3878	268	259	278	194	279	241	233	187
Number of Inter-Cluster Output Edges	3878	107	135	95	376	102	123	386	615
Wirelength Approx	1.65e+06	180828	185142	171924	247905	178166	178076	259059	252699
Scaled Cost	3.08								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.5 ± 14	2.6 ± 5	2.8 ± 5	2.4 ± 3.7	4 ± 18	2.4 ± 3.8	2.6 ± 5	4 ± 21	5 ± 23
Avg. Comb. Fanout	2.2 ± 3.6	2.6 ± 5	2.8 ± 5	2.4 ± 3.7	1.6 ± 1.9	2.4 ± 3.8	2.6 ± 5	1.5 ± 1.6	1.8 ± 2.1
Avg. PI Fanout	130 ± 40	N/A	N/A	N/A	103 ± 34	N/A	N/A	139 ± 49	149 ± 9
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.5 ± 0.5	3.6 ± 0.5	3.6 ± 0.5	3.5 ± 0.5	3.5 ± 0.6	3.5 ± 0.5	3.4 ± 0.5	3.6 ± 0.5	3.3 ± 0.6
Max Fanout	185	48	26	26	142	26	31	185	161

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	14	0	0	0	5	0	0	4	5	0	0	0	0	0	0	0	0	0
1	424	24	24	26	96	31	27	77	119	0	0	0	0	0	0	0	0	0
2	588	76	74	69	51	81	91	77	69	0	0	0	0	0	0	0	0	0
3	257	43	41	45	24	36	29	26	13	0	0	0	0	0	0	0	0	0
4	88	17	19	16	4	11	10	8	3	0	0	0	0	0	0	0	0	0
5	28	3	5	7	1	6	3	3	0	3	0	0	0	0	3	0	0	0
6	11	1	2	2	1	0	4	1	0	10	1	2	2	1	0	4	0	0
7	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1817	0	0	0	515	0	0	557	745
1	1407	75	78	82	327	90	89	276	390	2003	249	285	246	205	252	301	178	287
2	2111	287	267	242	188	301	303	282	241	758	128	125	88	64	105	97	79	72
3	968	162	159	168	96	131	105	97	50	261	43	41	45	24	39	30	26	13
4	322	62	70	59	13	43	35	29	11	89	17	19	16	4	12	10	8	3
5	101	12	17	27	3	20	11	11	0	25	3	5	7	1	3	3	3	0
6	42	3	8	7	4	0	16	4	0	1	0	0	0	0	0	0	1	0
7	3	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	4131	287	289	254	348	269	287	354	439
2	0	0	0	0	0	0	0	0	0	790	44	50	51	80	38	28	112	65
3	0	0	0	0	0	0	0	0	0	33	2	1	2	9	2	3	0	1
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	189	199	229	162	241	209	207	168	4131	98	112	87	322	88	110	284	503
2	0	72	59	45	32	37	32	26	19	790	9	23	8	52	14	13	96	107
3	0	7	1	4	0	1	0	0	0	33	0	0	0	2	0	0	6	5
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (14 1055 85 61 41 21 12 12 17 13 8 7 8 8 7 2 4 4 3 3 2 0 0 2 1 0 3 0 2 0 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 2 0 0 0 0 0 0 0 0 0 1 0 0 0, 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 1: (1 115 13 6 9 2 2 4 1 2 2 1 1 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 1)
Cluster 2: (2 121 4 6 7 5 1 0 2 2 1 1 2 1 3 0 2 2 0 1 0 0 0 0 1 0 1)
Cluster 3: (2 126 5 10 3 1 1 0 2 3 2 2 1 1 1 2 1 1 0 0 0 0 0 0 0 0 1)
Cluster 4: (1 140 14 7 4 3 1 0 3 0 0 1 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1)
Cluster 5: (4 114 14 10 4 2 2 3 3 1 0 1 2 1 1 0 1 0 0 0 1 0 0 1 0 0 1)
Cluster 6: (4 127 6 4 1 3 0 2 4 2 0 1 0 2 1 0 0 1 1 1 1 0 0 1 0 0 0 0 1 0 0 1)
Cluster 7: (0 163 9 5 5 0 2 2 2 3 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 8: (0 149 20 13 8 5 3 1 0 0 2 0 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0, 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	39	17	18	13	5	8	7	0	0	0	0	0	0	0	0
36	0	16	26	14	25	8	10	0	0	0	0	0	0	0	0
16	15	0	11	23	21	3	6	0	0	0	0	0	0	0	0
65	39	60	0	49	43	58	62	0	0	0	0	0	0	0	0
8	6	33	3	0	19	23	10	0	0	0	0	0	0	0	0
11	19	42	2	28	0	9	12	0	0	0	0	0	0	0	0
64	54	40	43	68	37	0	80	0	0	0	0	0	0	0	0
68	87	70	91	84	91	124	0	0	0	0	0	0	0	0	0

multmod_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1893	209	251	247	216	248	251	248	223
Number of PI	126	6	22	70	9	10	3	1	5
Number of DFF	193	15	3	2	0	83	7	20	63
Number of Combinational Nodes	1767	203	229	177	207	238	248	247	218
Number of PO	33	0	0	0	0	0	0	22	11
Number of Edges	5839	782	1060	914	885	884	1009	966	780
Number of Intra-Cluster Edges	4385	437	679	576	506	516	587	671	412
Number of Inter-Cluster Input Edges	2895	242	114	48	301	86	280	216	153
Number of Inter-Cluster Output Edges	2895	103	267	290	78	281	142	79	215
Wirelength Approx	1.30e+06	145777	168134	133163	167475	141022	168597	230482	149497
Scaled Cost	1.54								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.0 ± 6	2.5 ± 2.8	3.7 ± 7	3.5 ± 6	2.7 ± 3.6	3.2 ± 10	2.9 ± 5	3.0 ± 6	2.8 ± 6
Avg. Comb. Fanout	2.8 ± 5	2.3 ± 1.3	3.8 ± 7	4 ± 6	2.7 ± 3.7	2.1 ± 6	2.5 ± 2.8	2.5 ± 3.4	2.4 ± 7
Avg. PI Fanout	3.0 ± 12	1.3 ± 0.4	2.2 ± 6	1.1 ± 1.5	1.7 ± 2.1	19 ± 36	10 ± 12	1 ± 0	1 ± 0
Avg. DFF Fanout	5 ± 9	6 ± 9	6 ± 0.4	34 ± 0	N/A	3.3 ± 1.6	14 ± 23	9 ± 18	3.8 ± 1.9
Avg. Comb. Fanin	3.5 ± 0.5	3.5 ± 0.5	3.5 ± 0.6	3.5 ± 0.5	3.4 ± 0.6	3.8 ± 0.4	3.5 ± 0.4	3.6 ± 0.4	3.6 ± 0.5
Max Fanout	92	39	68	34	29	92	71	85	60

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	319	21	25	72	9	93	10	21	68	0	0	0	0	0	0	0	0	0
1	189	10	5	28	6	25	42	42	31	0	0	0	0	0	0	0	0	0
2	75	1	12	8	6	12	5	21	10	0	0	0	0	0	0	0	0	0
3	209	12	74	56	28	9	26	0	4	0	0	0	0	0	0	0	0	0
4	39	4	6	9	8	6	2	0	4	0	0	0	0	0	0	0	0	0
5	208	23	61	56	34	6	24	2	2	0	0	0	0	0	0	0	0	0
6	167	25	39	18	22	8	50	4	1	0	0	0	0	0	0	0	0	0
7	119	21	23	0	23	9	38	4	1	0	0	0	0	0	0	0	0	0
8	87	30	2	0	18	8	25	4	0	0	0	0	0	0	0	0	0	0
9	81	29	2	0	16	6	23	4	1	0	0	0	0	0	0	0	0	0
10	118	24	2	0	21	25	6	14	26	0	0	0	0	0	0	0	0	0
11	69	8	0	0	5	23	0	8	25	0	0	0	0	0	0	0	0	0
12	22	1	0	0	2	10	0	4	5	0	0	0	0	0	0	0	0	0
13	12	0	0	0	2	5	0	4	1	0	0	0	0	0	0	0	0	0
14	8	0	0	0	2	2	0	4	0	0	0	0	0	0	0	0	0	0
15	6	0	0	0	2	0	0	4	0	0	0	0	0	0	0	0	0	0
16	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
17	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
18	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
19	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
20	6	0	0	0	2	0	0	4	0	0	0	0	0	0	0	0	0	0
21	6	0	0	0	1	0	0	4	1	0	0	0	0	0	0	0	0	0
22	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
23	5	0	0	0	1	0	0	4	0	0	0	0	0	0	0	0	0	0
24	5	0	0	0	1	0	0	3	1	0	0	0	0	0	0	0	0	0
25	5	0	0	0	1	0	0	1	3	0	0	0	0	0	0	0	0	0
26	6	0	0	0	1	1	0	0	4	0	0	0	0	0	0	0	0	0
27	6	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0	0
28	4	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0
29	7	0	0	0	0	0	0	0	7	0	0	0	0	0	0	0	0	0
30	15	0	0	0	0	0	0	4	11	6	0	0	0	0	0	0	0	6
31	51	0	0	0	0	0	0	46	5	3	0	0	0	0	0	0	0	3
32	24	0	0	0	0	0	0	22	2	24	0	0	0	0	0	0	22	2

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1351	102	67	151	16	467	126	176	246
1	625	36	14	112	18	89	127	126	103	978	8	109	183	15	161	112	202	188
2	296	4	48	32	24	48	20	84	36	455	2	158	124	66	11	34	41	19
3	690	36	249	168	83	36	104	0	14	588	43	242	176	61	6	51	0	9
4	150	15	24	36	31	24	7	0	13	328	14	89	74	81	5	55	0	10
5	822	89	242	222	136	23	96	7	7	510	84	143	122	75	8	68	4	6
6	488	77	99	54	63	28	150	14	3	336	56	75	34	51	11	97	10	2
7	442	77	91	0	83	33	140	14	4	279	60	51	0	61	13	84	9	1
8	321	112	8	0	69	31	87	14	0	168	53	4	0	46	6	50	9	0
9	297	101	8	0	58	22	92	14	2	156	53	4	0	37	5	46	9	2
10	451	95	8	0	69	99	24	52	104	100	44	4	0	37	5	0	9	1
11	266	31	0	0	17	91	0	30	97	31	8	0	0	9	5	0	9	0
12	83	3	0	0	8	39	0	14	19	17	0	0	0	4	4	0	9	0
13	44	0	0	0	6	20	0	14	4	14	0	0	0	3	2	0	9	0
14	30	0	0	0	8	8	0	14	0	12	0	0	0	3	0	0	9	0
15	21	0	0	0	7	0	0	14	0	12	0	0	0	3	0	0	9	0
16	17	0	0	0	3	0	0	14	0	11	0	0	0	2	0	0	9	0
17	17	0	0	0	3	0	0	14	0	11	0	0	0	2	0	0	9	0
18	17	0	0	0	3	0	0	14	0	11	0	0	0	2	0	0	9	0
19	17	0	0	0	3	0	0	14	0	11	0	0	0	2	0	0	9	0
20	22	0	0	0	8	0	0	14	0	11	0	0	0	2	0	0	9	0
21	21	0	0	0	4	0	0	14	3	10	0	0	0	1	0	0	9	0
22	18	0	0	0	4	0	0	14	0	10	0	0	0	1	0	0	9	0
23	18	0	0	0	4	0	0	14	0	10	0	0	0	1	0	0	9	0
24	18	0	0	0	4	0	0	10	4	10	0	0	0	1	0	0	7	2
25	18	0	0	0	4	0	0	3	11	10	0	0	0	1	0	0	3	6
26	22	0	0	0	4	4	0	0	14	10	0	0	0	1	0	0	0	9
27	22	0	0	0	0	0	0	0	22	8	0	0	0	0	0	0	0	8
28	15	0	0	0	0	0	0	0	15	18	0	0	0	0	0	0	0	18
29	25	0	0	0	0	0	0	0	25	24	0	0	0	0	0	0	0	24
30	56	0	0	0	0	0	0	16	40	98	0	0	0	0	0	0	93	5
31	203	0	0	0	0	0	0	184	19	48	0	0	0	0	0	0	46	2
32	94	0	0	0	0	0	0	88	6	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	19	2	0	2	0	8	0	1	6	2755	224	383	326	256	151	327	275	117
2	4	0	0	0	0	4	0	0	0	1304	75	264	234	137	37	117	70	39
3	4	0	0	0	0	4	0	0	0	215	57	32	2	29	26	26	1	10
4	3	0	0	0	0	3	0	0	0	112	18	0	14	13	18	2	6	3
5	3	0	0	0	0	2	0	0	1	177	15	0	0	29	19	76	10	1
6	2	0	0	0	0	2	0	0	0	102	10	0	0	19	20	33	11	1
7	3	0	0	0	0	3	0	0	0	49	9	0	0	3	16	0	15	0
8	6	2	0	0	0	4	0	0	0	69	12	0	0	3	20	0	15	2
9	7	4	0	0	0	3	0	0	0	160	4	0	0	2	47	0	15	50
10	64	1	0	0	0	22	6	10	25	202	9	0	0	5	70	6	25	63
11	52	3	0	0	0	20	0	4	25	114	3	0	0	2	48	0	19	32
12	13	1	0	0	0	7	0	0	5	48	1	0	0	2	23	0	15	7
13	4	0	0	0	0	3	0	0	1	30	0	0	0	2	12	0	15	1
14	2	0	0	0	0	2	0	0	0	25	0	0	0	4	6	0	15	0
15	0	0	0	0	0	0	0	0	0	17	0	0	0	0	0	0	15	0
16	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	15	0
17	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	15	0
18	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	15	0
19	0	0	0	0	0	0	0	0	0	16	0	0	0	0	0	0	15	0
20	0	0	0	0	0	0	0	0	0	16	0	0	0	0	0	0	15	1
21	1	0	0	0	0	0	0	0	1	16	0	0	0	0	0	0	15	1
22	0	0	0	0	0	0	0	0	0	17	0	0	0	0	0	0	15	1
23	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	8	5
24	0	0	0	0	0	0	0	0	0	17	0	0	0	0	0	0	6	9
25	0	0	0	0	0	0	0	0	0	17	0	0	0	0	0	0	4	12
26	1	0	0	0	0	1	0	0	0	20	0	0	0	0	3	0	1	14
27	2	0	0	0	0	0	0	0	2	12	0	0	0	0	0	0	0	9
28	1	0	0	0	0	0	0	0	1	7	0	0	0	0	0	0	0	4
29	2	0	0	0	0	0	0	0	2	21	0	0	0	0	0	0	2	14
30	0	0	0	0	0	0	0	0	0	43	0	0	0	0	0	0	22	12
31	0	0	0	0	0	0	0	0	0	5	0	0	0	0	0	0	1	4
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	3	2	0	83	7	20	63	0	0	13	0	2	0	88	6	15	69
1	19	97	27	42	99	74	151	85	121	2755	72	123	97	68	99	105	43	89
2	4	66	78	0	66	2	95	15	9	1304	6	121	153	3	4	20	12	12
3	4	21	1	0	9	0	1	0	0	215	0	14	14	2	1	1	0	0
4	3	8	4	2	16	1	1	4	2	112	6	6	17	1	2	0	2	4
5	3	7	2	4	10	0	0	4	0	177	2	2	4	4	1	10	0	4
6	2	2	0	0	3	0	0	3	0	102	2	0	1	0	2	0	0	3
7	3	5	0	0	0	1	0	0	0	49	1	0	0	0	5	0	0	0
8	6	13	0	0	3	1	0	0	0	69	1	1	0	0	14	0	0	1
9	7	10	0	0	2	0	12	18	0	160	0	0	0	0	33	0	0	9
10	64	5	0	0	2	0	0	8	9	202	0	0	0	0	18	0	3	3
11	52	5	0	0	3	0	0	0	2	114	0	0	2	0	5	0	2	1
12	13	0	0	0	0	0	0	0	0	48	0	0	0	0	0	0	0	0
13	4	0	0	0	0	0	0	0	0	30	0	0	0	0	0	0	0	0
14	2	0	0	0	0	0	0	0	0	25	0	0	0	0	0	0	0	0
15	0	0	0	0	2	0	0	0	0	17	0	0	0	0	0	0	0	2
16	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	15	0	0	0	0	0	0	0	0
19	0	0	0	0	1	0	0	0	0	16	0	0	0	0	0	0	0	1
20	0	0	0	0	0	0	0	0	0	16	0	0	0	0	0	0	0	0
21	1	0	0	0	0	0	0	0	0	16	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	1	17	0	0	0	0	0	0	1	0
23	0	0	0	0	0	0	0	2	0	15	0	0	0	0	0	0	0	2
24	0	0	0	0	0	0	0	2	0	17	0	0	0	0	0	0	0	2
25	0	0	0	0	1	0	0	0	0	17	0	0	0	0	1	0	0	0
26	1	0	0	0	1	0	0	1	0	20	0	0	0	0	0	0	0	2
27	2	0	0	0	0	0	0	1	2	12	0	0	0	0	2	0	0	1
28	1	0	0	0	0	0	0	1	2	7	0	0	0	0	2	0	0	1
29	2	0	0	0	0	0	0	0	5	21	0	0	0	0	4	0	1	0
30	0	0	0	0	0	0	0	9	0	43	0	0	0	0	0	0	0	9
31	0	0	0	0	0	0	0	0	0	5	0	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (226 318 804 269 102 50 22 39 7 1 1 1 2 2 3 0 0 0 0 0 0 0 0 4 2 0 0 4 18 6 0 0 0 0 2 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 1 1 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0, 0 0 0 0 0 2)
Cluster 1: (13 37 87 36 23 6 1 3 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (0 26 170 31 2 2 2 2 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 8 3 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (2 73 115 17 0 1 0 27 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 6 2 0 0 0 0 2)
Cluster 4: (0 43 119 32 8 5 1 1 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 1)
Cluster 5: (88 44 55 25 13 9 2 5 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 2)
Cluster 6: (6 21 147 62 8 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 1 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (37 48 83 19 26 16 13 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (80 26 28 47 22 9 3 1 1 0 1 0 0 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	3	3	8	27	11	7	31	13	0	0	0	0	0	0	0
116	0	17	37	6	87	0	4	0	0	0	0	0	0	0	0
43	100	0	86	1	58	0	0	0	0	2	0	0	0	0	0
21	3	22	0	12	13	0	7	0	0	0	0	0	0	0	0
45	0	4	13	0	33	52	46	2	3	0	0	82	1	0	0
10	6	2	54	24	0	15	25	0	0	0	0	0	6	0	0
0	0	0	7	1	16	0	40	0	0	0	0	0	0	15	0
4	0	0	13	8	42	79	0	0	0	0	0	1	0	5	63

pdc

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	4591	550	557	557	552	584	552	688	551
Number of PI	16	0	3	9	3	1	0	0	0
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	4575	550	554	548	549	583	552	688	551
Number of PO	40	8	2	20	1	0	3	0	6
Number of Edges	17153	2342	3089	2426	2674	3336	2630	3947	2547
Number of Intra-Cluster Edges	11315	1205	1426	1717	1256	1476	1264	1798	1173
Number of Inter-Cluster Input Edges	11676	804	673	327	809	740	826	784	875
Number of Inter-Cluster Output Edges	11676	333	990	382	609	1120	540	1365	499
Wirelength Approx	1.45e+07	1.72e+06	1.98e+06	1.62e+06	1.74e+06	2.03e+06	1.62e+06	2.33e+06	1.51e+06
Scaled Cost	2.88								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.7 ± 16	2.7 ± 13	4 ± 20	3.7 ± 11	3.3 ± 11	4 ± 19	3.2 ± 12	5 ± 20	3.0 ± 13
Avg. Comb. Fanout	3.4 ± 14	2.7 ± 13	2.9 ± 7	3.3 ± 10	3.0 ± 10	4 ± 15	3.2 ± 12	5 ± 20	3.0 ± 13
Avg. PI Fanout	94 ± 95	N/A	254 ± 5	31 ± 27	68 ± 7	252 ± 0	N/A	N/A	N/A
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.7 ± 0.4	3.6 ± 0.5	3.7 ± 0.4	3.7 ± 0.5	3.7 ± 0.4	3.8 ± 0.4	3.7 ± 0.4	3.7 ± 0.4	3.7 ± 0.4
Max Fanout	260	213	260	134	181	252	184	237	232

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	16	0	3	9	3	1	0	0	0	0	0	0	0	0	0	0	0	0
1	111	1	19	35	35	8	3	10	0	0	0	0	0	0	0	0	0	0
2	814	51	122	182	122	115	66	127	29	0	0	0	0	0	0	0	0	0
3	2093	236	231	220	245	284	282	351	244	0	0	0	0	0	0	0	0	0
4	979	155	112	71	99	124	117	144	157	0	0	0	0	0	0	0	0	0
5	354	56	40	14	36	36	56	42	74	0	0	0	0	0	0	0	0	0
6	133	29	18	4	10	13	18	12	29	0	0	0	0	0	0	0	0	0
7	44	13	9	2	1	2	6	2	9	0	0	0	0	0	0	0	0	0
8	40	8	3	20	1	1	3	0	4	33	7	2	20	1	0	2	0	1
9	7	1	0	0	0	0	1	0	5	7	1	0	0	0	0	1	0	5

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1499	0	761	282	204	252	0	0	0
1	350	2	60	102	113	26	11	36	0	3835	11	334	881	433	693	182	1301	0
2	3092	195	477	702	457	439	247	466	109	7405	905	804	559	776	1110	1047	1190	1014
3	8078	863	901	830	958	1113	1116	1346	951	2769	348	319	245	298	362	366	463	368
4	3538	556	399	274	363	449	412	531	554	1048	172	125	71	107	126	123	150	174
5	1305	210	150	50	130	129	209	152	275	369	59	44	14	36	36	61	44	75
6	474	101	68	15	36	49	61	44	100	139	29	19	7	10	14	18	13	29
7	161	50	32	8	4	7	22	7	31	82	13	9	40	1	2	6	2	9
8	133	29	12	63	4	4	9	0	12	7	1	1	0	0	1	1	0	3
9	22	3	0	0	0	0	3	0	16	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	12342	952	986	1113	1040	1137	1062	1376	981
2	0	0	0	0	0	0	0	0	0	4631	250	438	517	203	330	196	420	181
3	0	0	0	0	0	0	0	0	0	136	1	2	50	10	9	4	2	11
4	0	0	0	0	0	0	0	0	0	23	2	0	16	3	0	2	0	0
5	0	0	0	0	0	0	0	0	0	9	0	0	9	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	8	0	0	8	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	4	0	0	4	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	505	435	226	487	436	503	548	555	12342	254	450	284	445	649	402	830	381
2	0	292	235	94	314	297	319	233	312	4631	76	538	96	153	457	138	525	113
3	0	7	3	7	8	7	4	3	8	136	3	2	2	11	14	0	10	5
4	0	0	0	0	0	0	0	0	0	23	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	9	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	8	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (40 3497 420 157 85 36 25 21 12 7 11 16 15 14 10 5 15 25 13 11 14 12 8 7 6 4 7 4 6 3 9 2, 4 2 3 3 6 1 1 0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 3 0 0 1 1 2 0 2 0 1 0 1, 0 1 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 0 0 2 0 1 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 1, 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 1)
Cluster 1: (8 414 48 28 14 5 3 1 2 1 1 2 2 3 4 0 1 3 3 1 0 0 2 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (2 400 64 18 9 10 4 6 2 1 3 1 3 0 2 1 3 5 1 4 1 2 1 0 1 1 0 0 0 0 1 2 0 0 0 0 2 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 1)
Cluster 3: (20 397 49 21 16 5 2 1 0 0 3 6 5 1 0 0 3 3 0 1 3 0 1 0 0 0 1 1 2 0 1 0 2 0 1 0 2 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (1 422 53 13 15 2 3 1 0 1 3 2 1 3 1 1 2 6 1 2 1 2 1 3 1 1 1 0 0 2 0 0 0 0 0 0 0 1 0 0 0, 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (0 449 53 15 9 4 6 4 5 1 0 1 1 3 1 1 3 3 1 0 3 1 1 0 0 1 0 0 3 1 2 0 1 2 0 0 0 0 0 0 0, 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (3 422 61 16 6 1 4 3 2 0 0 2 0 1 2 1 1 2 3 2 3 4 0 1 2 0 1 0 0 0 1 0 0 0 2 2 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (0 562 37 24 9 6 1 2 1 2 1 2 3 1 0 1 2 2 4 0 3 2 0 2 0 0 2 2 1 0 2 0 1 0 0 0 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0, 0 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (6 431 55 22 7 3 2 3 0 1 0 0 0 2 0 0 0 1 0 1 0 1 2 1 2 0 2 1 0 0 2 0 0 0 0 1 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	76	32	43	39	36	74	33	0	0	0	0	0	0	0	0
176	0	43	193	133	125	138	182	0	0	0	0	0	0	0	0
82	33	0	57	50	45	63	52	0	0	0	0	0	0	0	0
99	81	95	0	91	82	106	55	0	0	0	0	0	0	0	0
136	172	37	189	0	232	171	183	0	0	0	0	0	0	0	0
74	55	7	94	96	0	112	102	0	0	0	0	0	0	0	0
154	177	102	191	251	222	0	268	0	0	0	0	0	0	0	0
83	79	11	42	80	84	120	0	0	0	0	0	0	0	0	0

peak_chip

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1146	142	142	138	137	145	145	157	140
Number of PI	30	6	1	2	10	10	0	1	0
Number of DFF	316	29	36	36	39	57	32	26	61
Number of Combinational Nodes	1116	136	141	136	127	135	145	156	140
Number of PO	22	7	2	5	4	1	3	0	0
Number of Edges	2754	388	434	398	378	335	413	1089	293
Number of Intra-Cluster Edges	1761	223	236	217	166	128	248	391	147
Number of Inter-Cluster Input Edges	1967	136	130	123	145	122	137	98	78
Number of Inter-Cluster Output Edges	1967	29	68	58	67	83	28	597	68
Wirelength Approx	443034	55345	64239	48692	47232	38950	65816	82403	40357
Scaled Cost	1.35								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.4 ± 19	1.7 ± 1.7	2.1 ± 2.8	1.9 ± 2.2	1.7 ± 1.5	1.4 ± 1.7	1.9 ± 2.6	6 ± 51	1.5 ± 1.7
Avg. Comb. Fanout	1.4 ± 1.6	1.5 ± 1.4	1.7 ± 2.8	1.4 ± 1.4	1.3 ± 0.9	1 ± 0.1	1.5 ± 1.1	1.7 ± 2.3	1 ± 0
Avg. PI Fanout	22 ± 114	1 ± 0	1 ± 0	1 ± 0	1 ± 0	1 ± 0	N/A	636 ± 0	N/A
Avg. DFF Fanout	2.9 ± 3.4	2.5 ± 2.2	3.2 ± 2.7	3.5 ± 3.1	2.7 ± 2.0	2.1 ± 2.5	3.2 ± 5	5 ± 6	2.2 ± 2.4
Avg. Comb. Fanin	3.0 ± 0.9	3.0 ± 0.9	3.1 ± 0.8	3.0 ± 0.9	2.8 ± 0.9	2.7 ± 0.9	3.1 ± 0.8	3.2 ± 0.8	2.8 ± 0.9
Max Fanout	636	11	22	12	9	15	29	636	11

Node Shape										PO Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	346	35	37	38	49	67	32	27	61	0	0	0	0	0	0	0	0	0	
1	418	46	45	55	45	62	49	53	63	22	7	2	5	4	1	3	0	0	
2	48	8	6	8	6	0	2	9	9	0	0	0	0	0	0	0	0	0	
3	67	11	9	13	11	0	4	12	7	0	0	0	0	0	0	0	0	0	
4	54	14	7	8	8	0	1	16	0	0	0	0	0	0	0	0	0	0	
5	32	10	2	1	3	7	3	6	0	0	0	0	0	0	0	0	0	0	
6	20	6	0	1	3	8	0	2	0	0	0	0	0	0	0	0	0	0	
7	31	5	0	11	5	0	8	2	0	0	0	0	0	0	0	0	0	0	
8	28	3	0	2	5	0	16	2	0	0	0	0	0	0	0	0	0	0	
9	14	2	1	1	1	0	9	0	0	0	0	0	0	0	0	0	0	0	
10	13	2	1	0	1	0	9	0	0	0	0	0	0	0	0	0	0	0	
11	5	0	1	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	
12	9	0	3	0	0	1	5	0	0	0	0	0	0	0	0	0	0	0	
13	22	0	18	0	0	0	2	2	0	0	0	0	0	0	0	0	0	0	
14	29	0	10	0	0	0	1	18	0	0	0	0	0	0	0	0	0	0	
15	10	0	2	0	0	0	0	8	0	0	0	0	0	0	0	0	0	0	

Input Shape										Output Shape									
Delay	Circuit	Cluster								Circuit	Cluster								
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	0	0	0	0	0	0	0	0	0	1586	81	117	131	117	133	105	766	136	
1	1033	104	109	140	99	154	124	141	162	216	21	52	38	9	3	25	59	9	
2	173	22	22	29	22	0	7	36	35	108	25	17	21	11	0	6	19	9	
3	250	43	35	48	37	0	14	45	28	126	35	18	20	23	0	4	19	7	
4	199	47	27	31	27	0	4	63	0	79	32	8	8	8	0	4	19	0	
5	114	36	6	3	11	28	10	20	0	37	12	2	1	3	7	3	9	0	
6	78	23	0	4	12	32	0	7	0	35	7	0	12	4	8	0	4	0	
7	115	20	0	36	19	0	32	8	0	45	5	0	7	8	0	22	3	0	
8	100	12	0	8	20	0	52	8	0	37	3	0	1	6	0	24	3	0	
9	53	8	4	2	3	0	36	0	0	31	2	1	0	1	0	27	0	0	
10	49	8	2	0	4	0	35	0	0	14	3	0	0	1	0	10	0	0	
11	18	0	4	0	0	0	14	0	0	12	0	4	0	0	0	8	0	0	
12	36	0	12	0	0	4	20	0	0	28	0	20	0	0	0	8	0	0	
13	86	0	70	0	0	0	8	8	0	62	0	24	0	0	0	2	36	0	
14	106	0	31	0	0	0	3	72	0	22	0	4	0	0	0	0	18	0	
15	28	0	8	0	0	0	0	20	0	0	0	0	0	0	0	0	0	0	

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	0	3	0
1	278	26	25	28	36	59	26	24	54	1614	142	153	158	98	96	164	244	116
2	2	0	0	0	2	0	0	0	0	198	29	25	25	17	0	20	29	17
3	2	0	0	0	2	0	0	0	0	158	35	8	13	19	0	4	25	14
4	1	0	0	0	1	0	0	0	0	104	8	3	6	19	0	5	35	0
5	0	0	0	0	0	0	0	0	0	56	2	5	3	3	14	4	6	0
6	0	0	0	0	0	0	0	0	0	50	4	0	4	3	16	0	5	0
7	7	0	0	6	1	0	0	0	0	59	0	0	8	3	0	18	4	0
8	1	0	0	1	0	0	0	0	0	56	1	2	0	3	0	26	2	0
9	1	0	0	1	0	0	0	0	0	17	1	3	0	0	0	5	2	0
10	1	0	1	0	0	0	0	0	0	16	1	4	0	1	0	0	3	0
11	1	0	0	0	0	0	1	0	0	13	0	2	0	0	0	2	6	0
12	3	0	2	0	0	1	0	0	0	38	0	24	0	0	2	0	2	0
13	2	0	1	0	0	0	0	1	0	29	0	3	0	0	0	0	8	0
14	7	0	6	0	0	0	1	0	0	26	0	4	0	0	0	0	18	0
15	10	0	2	0	0	0	0	8	0	4	0	0	0	0	0	0	2	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	36	36	39	57	32	26	61	0	0	26	37	36	42	60	28	33	54
1	278	53	46	51	54	74	72	31	62	1614	3	16	17	20	15	0	359	13
2	2	10	4	7	5	0	1	0	9	198	0	2	0	1	0	0	33	0
3	2	5	7	10	7	0	3	1	7	158	0	3	1	3	1	0	31	1
4	1	12	3	5	6	0	2	0	0	104	0	1	0	1	0	0	26	0
5	0	2	2	1	3	7	3	1	0	56	0	1	1	0	1	0	16	0
6	0	4	0	2	4	8	0	0	0	50	0	1	1	0	0	0	16	0
7	7	5	0	6	5	0	8	2	0	59	0	3	2	0	1	0	20	0
8	1	4	0	1	3	0	14	0	0	56	0	1	0	0	0	0	21	0
9	1	3	0	1	0	0	2	0	0	17	0	1	0	0	0	0	5	0
10	1	2	1	0	1	0	3	0	0	16	0	0	0	0	1	0	6	0
11	1	0	1	0	0	0	2	0	0	13	0	0	0	0	0	0	3	0
12	3	0	7	0	0	1	0	2	0	38	0	2	0	0	4	0	4	0
13	2	0	18	0	0	0	0	0	0	29	0	0	0	0	0	0	18	0
14	7	0	3	0	0	0	1	0	0	26	0	0	0	0	0	0	4	0
15	10	0	2	0	0	0	0	0	0	4	0	0	0	0	0	0	2	0

Fanout Distribution
Circuit: (329 501 128 63 48 15 21 7 3 7 5 9 2 0 0 1 0 0 2 0 1 0 1 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (33 63 17 15 4 3 4 1 0 0 0 2)
Cluster 2: (38 59 16 8 9 2 1 2 2 2 1 0 0 0 0 0 0 0 0 0 1 0 1)
Cluster 3: (37 63 11 7 6 1 6 1 0 3 1 0 2)
Cluster 4: (45 56 10 9 7 5 2 2 0 1)
Cluster 5: (61 57 18 3 3 0 0 0 0 0 0 2 0 0 0 1)
Cluster 6: (29 70 17 14 6 3 4 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (32 76 21 4 9 1 4 1 1 1 1 2 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (54 57 18 3 4 0 0 0 0 0 1 3)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	1	0	0	0	2	0	0	26	0	0	0	0	0	0	0
25	0	1	0	1	0	4	0	0	36	0	0	0	1	0	0
0	1	0	14	0	0	7	0	1	0	35	0	0	0	0	0
1	4	6	0	0	2	12	0	2	0	1	39	0	0	0	0
0	5	0	0	0	14	4	0	0	0	0	0	54	2	0	4
0	0	0	0	0	0	0	0	0	0	0	0	0	28	0	0
74	83	77	74	89	89	0	78	0	0	0	0	3	1	26	3
0	0	0	0	0	4	10	0	0	0	0	0	0	0	0	54

pipe_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	798	102	119	99	103	100	98	83	94
Number of PI	109	4	2	16	18	26	27	12	4
Number of DFF	218	40	36	25	27	9	23	22	36
Number of Combinational Nodes	689	98	117	83	85	74	71	71	90
Number of PO	186	28	16	25	27	9	23	22	36
Number of Edges	1908	350	478	287	283	344	272	224	268
Number of Intra-Cluster Edges	1270	138	222	149	160	178	161	100	162
Number of Inter-Cluster Input Edges	1236	123	97	76	53	88	47	96	18
Number of Inter-Cluster Output Edges	1236	89	159	62	70	78	64	28	88
Wirelength Approx	218983	29248	42603	27748	29617	30943	21153	17419	20252
Scaled Cost	1.17								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.3 ± 7	2.2 ± 4	3.2 ± 15	2.1 ± 3.4	2.2 ± 3.4	2.5 ± 6	2.2 ± 6	1.5 ± 1.1	2.6 ± 5
Avg. Comb. Fanout	1.4 ± 3.3	1 ± 0	1 ± 0	1.7 ± 4	1.2 ± 0.4	2.7 ± 7	1.6 ± 4	1.1 ± 1.2	1 ± 0
Avg. PI Fanout	6 ± 17	17 ± 16	113 ± 16	1.3 ± 0.6	2.7 ± 7	2.0 ± 0.1	3.7 ± 11	1.5 ± 0.5	27 ± 3.5
Avg. DFF Fanout	2.6 ± 1.4	2.5 ± 0.6	2.0 ± 0.6	3.4 ± 2.3	4 ± 2.3	2.4 ± 0.4	2 ± 0	2.3 ± 0.4	2.5 ± 0.5
Avg. Comb. Fanin	3.5 ± 0.5	3.8 ± 0.3	3.6 ± 0.4	3.4 ± 0.5	3.5 ± 0.4	3.7 ± 0.4	3.8 ± 0.4	3.2 ± 0.6	3.3 ± 0.4
Max Fanout	129	32	129	32	32	30	53	10	30

Node Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	327	44	38	41	45	35	50	34	40
1	167	40	54	19	18	8	1	9	18
2	127	12	20	5	0	48	24	18	0
3	68	0	2	6	0	5	23	14	18
4	38	0	1	7	0	4	0	8	18
5	9	0	0	9	0	0	0	0	0
6	9	0	0	7	2	0	0	0	0
7	9	0	0	4	5	0	0	0	0
8	9	0	0	1	8	0	0	0	0
9	9	0	1	0	8	0	0	0	0
10	9	0	1	0	8	0	0	0	0
11	8	1	0	0	7	0	0	0	0
12	6	3	1	0	2	0	0	0	0
13	3	2	1	0	0	0	0	0	0

PO Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	156	28	16	25	27	5	23	14	18
1	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0
3	30	0	0	0	0	4	0	8	18
4	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0

Input Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	565	155	191	56	54	25	4	26	54
2	507	48	80	19	0	192	96	72	0
3	240	0	8	22	0	14	86	38	72
4	120	0	3	27	0	12	0	24	54
5	33	0	0	33	0	0	0	0	0
6	33	0	0	25	8	0	0	0	0
7	33	0	0	13	20	0	0	0	0
8	33	0	0	3	30	0	0	0	0
9	33	0	3	0	30	0	0	0	0
10	33	0	3	0	30	0	0	0	0
11	29	4	0	0	25	0	0	0	0
12	21	11	3	0	7	0	0	0	0
13	10	7	3	0	0	0	0	0	0

Output Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	1223	169	300	107	158	75	148	70	196
1	260	15	45	39	1	120	30	10	0
2	98	0	0	8	0	48	24	18	0
3	38	0	0	8	0	4	0	8	18
4	9	0	0	9	0	0	0	0	0
5	9	0	0	9	0	0	0	0	0
6	9	0	0	5	4	0	0	0	0
7	9	0	0	1	8	0	0	0	0
8	9	0	0	0	9	0	0	0	0
9	9	0	0	0	9	0	0	0	0
10	8	0	0	0	8	0	0	0	0
11	6	1	0	0	5	0	0	0	0
12	3	2	0	0	1	0	0	0	0
13	0	0	0	0	0	0	0	0	0

Latched Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	94	25	9	13	17	4	0	8	18
2	32	12	20	0	0	0	0	0	0
3	33	0	2	1	0	1	23	6	0
4	32	0	1	1	0	4	0	8	18
5	3	0	0	3	0	0	0	0	0
6	3	0	0	3	0	0	0	0	0
7	3	0	0	3	0	0	0	0	0
8	3	0	0	1	2	0	0	0	0
9	3	0	1	0	2	0	0	0	0
10	3	0	1	0	2	0	0	0	0
11	3	0	0	0	3	0	0	0	0
12	3	1	1	0	1	0	0	0	0
13	3	2	1	0	0	0	0	0	0

Intra-Cluster Edge Length Distribution

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	962	117	157	73	88	113	50	48	72
2	333	12	51	13	0	57	71	36	0
3	132	0	4	14	0	4	40	8	54
4	82	0	2	18	0	4	0	8	36
5	24	0	0	19	0	0	0	0	0
6	24	0	0	8	5	0	0	0	0
7	24	0	0	3	11	0	0	0	0
8	24	0	0	1	14	0	0	0	0
9	24	0	2	0	15	0	0	0	0
10	24	1	2	0	14	0	0	0	0
11	20	1	0	0	11	0	0	0	0
12	11	5	2	0	2	0	0	0	0
13	6	2	2	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution

Edge Length	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	36	25	27	9	23	22	36	0
1	94	56	61	25	6	18	24	36	18
2	32	24	11	2	0	43	1	12	0
3	33	0	0	4	0	0	0	4	0
4	32	0	0	2	0	4	0	8	0
5	3	0	0	5	0	0	0	0	0
6	3	0	0	6	5	0	0	0	0
7	3	0	0	4	6	0	0	0	0
8	3	0	0	1	8	0	0	0	0
9	3	0	0	0	7	0	0	0	0
10	3	1	0	0	6	0	0	0	0
11	3	3	0	0	5	0	0	0	0
12	3	1	0	0	1	0	0	0	0
13	3	2	0	0	0	0	0	0	0

Inter-cluster Output Edge Length Distribution

Edge Length	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	40	36	25	27	9	23	22	36
1	962	38	52	19	39	62	12	4	18
2	333	11	26	0	0	7	29	2	18
3	132	0	4	0	0	0	0	0	4
4	82	0	2	0	0	0	0	0	12
5	24	0	5	0	0	0	0	0	0
6	24	0	6	3	2	0	0	0	0
7	24	0	6	3	1	0	0	0	0
8	24	0	6	3	0	0	0	0	0
9	24	0	4	3	0	0	0	0	0
10	24	0	4	3	0	0	0	0	0
11	20	0	4	3	1	0	0	0	0
12	11	0	2	0	0	0	0	0	0
13	6	0	2	0	0	0	0	0	0

Fanout Distribution
Circuit: (218 313 150 68 3 3 25 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0 0 0 0 7 0 4 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (40 23 12 24 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 2: (36 52 20 9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (25 44 12 4 1 2 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (27 44 14 0 1 1 15 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (9 52 30 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4)
Cluster 6: (23 48 24 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (22 32 20 8 0 0 0 0 0 0 1)
Cluster 8: (36 18 18 18 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 2)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	45	3	1	0	0	0	0	40	0	0	0	0	0	0	0
68	0	30	25	0	0	0	0	0	36	0	0	0	0	0	0
5	14	0	18	0	0	0	0	0	0	25	0	0	0	0	0
14	13	16	0	0	0	0	0	0	0	0	27	0	0	0	0
0	0	0	0	0	25	26	18	0	0	0	0	9	0	0	0
0	0	0	0	29	0	12	0	0	0	0	0	0	23	0	0
0	0	0	0	6	0	0	0	0	0	0	0	0	0	22	0
0	0	0	0	30	0	22	0	0	0	0	0	0	0	0	36

prils_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	501	75	64	63	52	63	62	63	59
Number of PI	113	5	11	2	23	21	20	23	8
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	388	70	53	61	29	42	42	40	51
Number of PO	39	0	9	18	5	4	2	0	1
Number of Edges	1429	416	190	255	140	215	210	202	237
Number of Intra-Cluster Edges	993	220	116	136	71	138	109	94	109
Number of Inter-Cluster Input Edges	872	60	62	70	37	20	47	54	86
Number of Inter-Cluster Output Edges	872	136	12	49	32	57	54	54	42
Wirelength Approx	203908	41240	23746	28076	12809	21198	25242	21543	30054
Scaled Cost	1.96								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.8 ± 6	5 ± 12	2 ± 3.4	2.9 ± 7	1.9 ± 5	3.0 ± 5	2.6 ± 2.8	2.3 ± 1.7	2.5 ± 2.8
Avg. Comb. Fanout	2.8 ± 6	5 ± 13	2.1 ± 3.7	3 ± 7	1.5 ± 3.3	2.6 ± 1.4	2.9 ± 3.4	2.3 ± 1.3	2.0 ± 1.6
Avg. PI Fanout	2.7 ± 5	2.6 ± 1.9	1.0 ± 0.2	1 ± 0	2.4 ± 7	4 ± 9	2.0 ± 0.9	2.3 ± 2.3	6 ± 6
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.6 ± 0.6	4 ± 0	3.3 ± 0.8	3.3 ± 0.8	3.7 ± 0.5	3.7 ± 0.6	3.7 ± 0.5	3.7 ± 0.6	3.8 ± 0.4
Max Fanout	68	68	28	47	35	32	16	13	18

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	113	5	11	2	23	21	20	23	8	0	0	0	0	0	0	0	0	0
1	36	2	0	0	0	17	9	6	2	0	0	0	0	0	0	0	0	0
2	14	0	0	0	0	8	3	3	0	0	0	0	0	0	0	0	0	0
3	6	0	0	0	0	2	2	2	0	0	0	0	0	0	0	0	0	0
4	7	0	0	0	0	3	3	1	0	0	0	0	0	0	0	0	0	0
5	11	0	0	0	0	5	6	0	0	2	0	0	0	0	0	2	0	0
6	6	1	0	0	0	2	3	0	0	1	0	0	0	0	1	0	0	0
7	27	2	0	0	0	3	2	6	14	1	0	0	0	0	1	0	0	0
8	36	1	0	0	0	2	14	6	13	2	0	0	0	0	2	0	0	0
9	31	16	1	1	0	0	0	7	6	0	0	0	0	0	0	0	0	0
10	61	48	0	2	2	0	0	5	4	0	0	0	0	0	0	0	0	0
11	32	0	8	18	1	0	0	1	4	0	0	0	0	0	0	0	0	0
12	54	0	13	20	16	0	0	1	4	0	0	0	0	0	0	0	0	0
13	36	0	9	19	4	0	0	2	2	20	0	2	17	1	0	0	0	0
14	17	0	13	1	2	0	0	0	1	6	0	4	1	1	0	0	0	0
15	9	0	5	0	3	0	0	0	1	5	0	2	0	2	0	0	0	1
16	3	0	2	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
17	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	311	13	12	2	57	85	41	54	47
1	142	8	0	0	0	68	36	24	6	197	45	0	0	0	65	47	28	12
2	44	0	0	0	0	24	10	10	0	22	0	0	0	0	13	5	4	0
3	21	0	0	0	0	8	7	6	0	16	0	0	0	0	7	5	4	0
4	25	0	0	0	0	12	9	4	0	21	0	0	0	0	12	8	1	0
5	42	0	0	0	0	20	22	0	0	13	0	0	0	0	5	8	0	0
6	24	4	0	0	0	8	12	0	0	55	49	0	0	0	3	3	0	0
7	104	8	0	0	0	12	4	24	56	139	71	0	0	0	3	32	16	17
8	137	4	0	0	0	6	56	20	51	134	67	0	0	0	2	14	12	39
9	119	64	4	4	0	0	0	26	21	165	63	28	47	0	0	0	15	12
10	238	192	0	5	5	0	0	20	16	121	48	0	39	20	0	0	6	8
11	81	0	19	39	3	0	0	4	16	113	0	31	72	4	0	0	2	4
12	215	0	51	80	64	0	0	4	16	76	0	27	23	16	0	0	2	8
13	133	0	30	74	16	0	0	6	7	23	0	11	2	3	0	0	4	3
14	59	0	43	4	8	0	0	0	4	15	0	13	0	1	0	0	0	1
15	27	0	16	0	9	0	0	0	2	5	0	3	0	2	0	0	0	0
16	11	0	8	0	3	0	0	0	0	2	0	2	0	0	0	0	0	0
17	3	0	3	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
18	4	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	679	64	56	59	4	96	65	48	48
2	0	0	0	0	0	0	0	0	0	184	47	18	35	18	9	6	7	6
3	0	0	0	0	0	0	0	0	0	224	67	20	38	3	19	10	10	8
4	0	0	0	0	0	0	0	0	0	46	1	5	2	0	9	8	0	4
5	0	0	0	0	0	0	0	0	0	20	0	5	0	1	3	1	0	4
6	0	0	0	0	0	0	0	0	0	32	3	0	0	0	2	0	0	1
7	0	0	0	0	0	0	0	0	0	79	3	0	0	0	0	9	14	25
8	0	0	0	0	0	0	0	0	0	73	35	0	0	0	0	10	5	11
9	0	0	0	0	0	0	0	0	0	12	0	1	1	0	0	0	5	1
10	0	0	0	0	0	0	0	0	0	9	0	0	0	1	0	0	3	0
11	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
12	0	0	0	0	0	0	0	0	0	33	0	0	0	32	0	0	1	0
13	0	0	0	0	0	0	0	0	0	14	0	2	1	6	0	0	0	1
14	0	0	0	0	0	0	0	0	0	13	0	5	0	2	0	0	0	0
15	0	0	0	0	0	0	0	0	0	7	0	3	0	2	0	0	0	0
16	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	28	22	59	30	18	31	33	18	679	80	8	22	19	36	32	21	21
2	0	16	5	0	0	2	1	9	5	184	15	0	1	0	0	2	4	16
3	0	12	15	6	2	0	3	2	9	224	17	3	14	0	1	0	12	2
4	0	0	5	0	2	0	1	2	7	46	6	0	9	1	0	0	1	0
5	0	0	3	0	3	0	0	0	0	20	1	1	3	0	0	0	1	0
6	0	0	0	0	0	0	0	0	26	32	2	0	0	0	13	5	6	0
7	0	3	0	0	0	0	7	6	12	79	11	0	0	0	1	8	7	1
8	0	0	0	0	0	0	4	0	8	73	0	0	0	0	5	4	1	2
9	0	0	2	2	0	0	0	0	0	12	4	0	0	0	0	0	0	0
10	0	1	0	2	0	0	0	2	0	9	0	0	0	2	0	3	0	0
11	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	33	0	0	0	0	0	0	0	0
13	0	0	2	1	0	0	0	0	1	14	0	0	0	4	0	0	0	0
14	0	0	6	0	0	0	0	0	0	13	0	0	0	4	1	0	1	0
15	0	0	2	0	0	0	0	0	0	7	0	0	0	2	0	0	0	0
16	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (34 252 64 47 66 16 3 0 0 0 1 0 1 1 0 0 2 0 1 3 1 0 0 0 0 0 1 0 1 0 0 0 2 0 0 1 0 0 0 0 0, 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 1: (0 51 0 2 15 2 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 2: (9 25 20 1 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (18 21 3 0 18 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 1)
Cluster 4: (5 43 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (0 33 6 5 14 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 6: (1 32 3 14 2 5 3 0 0 0 0 0 0 0 0 0 2)
Cluster 7: (0 20 23 11 4 4 0 0 0 0 0 0 0 1)
Cluster 8: (1 27 8 14 4 2 0 0 0 0 1 0 1 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	18	38	3	0	2	27	48	0	0	0	0	0	0	0	0
0	0	6	6	0	0	0	0	0	0	0	0	0	0	0	0
0	22	0	22	0	0	2	3	0	0	0	0	0	0	0	0
0	9	21	0	0	0	0	2	0	0	0	0	0	0	0	0
2	2	1	0	0	23	12	17	0	0	0	0	0	0	0	0
18	0	0	0	15	0	12	9	0	0	0	0	0	0	0	0
14	11	0	1	3	18	0	7	0	0	0	0	0	0	0	0
26	0	4	5	2	4	1	0	0	0	0	0	0	0	0	0

rsadd_dp

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	521	60	71	61	61	77	54	76	61
Number of PI	168	38	16	26	20	3	11	30	24
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	353	22	55	35	41	74	43	46	37
Number of PO	35	3	9	12	10	0	0	0	1
Number of Edges	1231	84	193	159	168	348	172	299	172
Number of Intra-Cluster Edges	867	63	111	92	89	186	79	167	80
Number of Inter-Cluster Input Edges	728	18	73	25	52	58	68	11	59
Number of Inter-Cluster Output Edges	728	3	9	42	27	104	25	121	33
Wirelength Approx	165663	6203	28397	18924	21427	33460	19859	20808	16585
Scaled Cost	1.56								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.3 ± 7	1.1 ± 0.4	1.6 ± 0.9	2.1 ± 6	1.9 ± 4	3.7 ± 10	1.9 ± 1.1	3.7 ± 13	1.8 ± 1.1
Avg. Comb. Fanout	1.5 ± 0.9	1.2 ± 0.6	1.8 ± 1.0	1.3 ± 0.9	1.5 ± 0.8	2.1 ± 1.0	1.6 ± 1.0	1.0 ± 0.1	1.2 ± 0.7
Avg. PI Fanout	3.9 ± 12	1 ± 0	1 ± 0	3.3 ± 8	2.7 ± 7	45 ± 31	2.9 ± 1.1	8 ± 19	2.8 ± 0.8
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.4 ± 0.7	3.6 ± 0.5	3.3 ± 0.7	3.3 ± 0.4	3.4 ± 0.5	3.2 ± 0.9	3.4 ± 0.8	3.8 ± 0.4	3.7 ± 0.6
Max Fanout	81	2	4	32	34	67	4	81	4

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	168	38	16	26	20	3	11	30	24	0	0	0	0	0	0	0	0	0
1	128	11	8	12	9	2	15	45	26	0	0	0	0	0	0	0	0	0
2	39	2	6	0	2	17	8	1	3	0	0	0	0	0	0	0	0	0
3	65	2	10	0	2	35	13	0	3	1	1	0	0	0	0	0	0	0
4	21	0	3	0	1	9	6	0	2	0	0	0	0	0	0	0	0	0
5	33	2	10	0	7	11	1	0	2	0	0	0	0	0	0	0	0	0
6	5	0	0	0	4	0	0	0	1	2	0	0	0	1	0	0	0	1
7	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
8	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
9	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
10	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
11	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
12	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
13	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
14	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
15	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
16	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
17	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
18	2	0	0	2	0	0	0	0	0	1	0	0	1	0	0	0	0	0
19	2	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0
20	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
21	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
22	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
23	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
24	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
25	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
26	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
27	2	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
28	2	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
29	2	2	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
30	2	2	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
31	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
32	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
33	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
34	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
35	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
36	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
37	2	0	0	0	2	0	0	0	0	2	0	0	0	2	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	671	38	16	88	54	134	32	241	68
1	504	44	32	48	36	4	60	176	104	162	14	16	24	18	4	15	45	26
2	84	8	12	0	6	34	16	2	6	135	2	24	0	4	63	30	2	10
3	258	6	40	0	8	140	52	0	12	96	2	20	0	4	52	14	0	4
4	52	0	6	0	3	22	15	0	6	37	0	6	0	2	15	11	0	3
5	131	8	40	0	27	44	4	0	8	64	4	20	0	14	22	2	0	2
6	16	0	0	0	13	0	0	0	3	6	0	0	0	6	0	0	0	0
7	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
8	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
9	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
10	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
11	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
12	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
13	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
14	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
15	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
16	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
17	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
18	6	0	0	6	0	0	0	0	0	2	0	0	2	0	0	0	0	0
19	6	0	3	3	0	0	0	0	0	2	0	2	0	0	0	0	0	0
20	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
21	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
22	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
23	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
24	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
25	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
26	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
27	6	0	6	0	0	0	0	0	0	2	0	2	0	0	0	0	0	0
28	6	3	3	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0
29	6	6	0	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0
30	6	6	0	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0
31	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
32	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
33	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
34	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
35	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
36	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
37	6	0	0	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	854	52	57	69	37	88	76	167	73
2	0	0	0	0	0	0	0	0	0	77	2	20	0	8	26	1	0	5
3	0	0	0	0	0	0	0	0	0	128	0	0	0	0	69	0	0	1
4	0	0	0	0	0	0	0	0	0	17	0	0	0	1	3	2	0	1
5	0	0	0	0	0	0	0	0	0	35	0	0	0	9	0	0	0	0
6	0	0	0	0	0	0	0	0	0	8	0	0	0	6	0	0	0	0
7	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	4	0	0	2	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	4	0	1	2	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	4	0	2	2	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	4	0	2	2	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	4	0	2	2	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	4	0	2	1	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	4	0	4	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	4	0	4	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	4	0	4	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	4	0	4	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	4	0	3	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	4	2	2	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	4	2	2	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	4	0	2	0	2	0	0	0	0
27	0	0	0	0	0	0	0	0	0	4	1	0	0	2	0	0	0	0
28	0	0	0	0	0	0	0	0	0	4	2	0	0	2	0	0	0	0
29	0	0	0	0	0	0	0	0	0	4	2	0	0	2	0	0	0	0
30	0	0	0	0	0	0	0	0	0	6	0	0	0	6	0	0	0	0
31	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
32	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
33	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
34	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
35	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
36	0	0	0	0	0	0	0	0	0	2	0	0	0	2	0	0	0	0
37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	11	41	2	38	47	37	11	48	854	2	7	41	3	9	25	115	33
2	0	2	0	0	9	0	2	0	2	77	0	0	0	0	13	0	2	0
3	0	2	20	2	4	0	25	0	5	128	0	0	0	0	57	0	1	0
4	0	0	0	2	1	0	4	0	3	17	0	0	0	0	7	0	3	0
5	0	2	10	2	0	11	0	0	1	35	0	0	0	24	2	0	0	0
6	0	0	0	2	0	0	0	0	0	8	0	0	0	0	2	0	0	0
7	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
8	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
9	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
10	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
11	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
12	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
13	0	0	0	2	0	0	0	0	0	4	0	0	0	0	2	0	0	0
14	0	0	0	1	0	0	0	0	0	4	0	1	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
18	0	0	1	0	0	0	0	0	0	4	0	0	1	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
23	0	1	0	0	0	0	0	0	0	4	0	1	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
27	0	0	1	0	0	0	0	0	0	4	1	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
33	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (35 242 164 23 50 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 1 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 1: (3 48 9)
Cluster 2: (9 16 40 0 6)
Cluster 3: (12 24 23 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 4: (10 19 30 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (0 23 35 4 13 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 6: (0 30 9 4 11)
Cluster 7: (0 50 6 7 11 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1)
Cluster 8: (1 32 12 7 9)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0
3	0	1	0	5	0	0	0	0	0	0	0	0	0	0	0
6	18	0	18	0	0	0	0	0	0	0	0	0	0	0	0
2	10	2	0	11	0	0	2	0	0	0	0	0	0	0	0
4	25	22	17	0	29	0	7	0	0	0	0	0	0	0	0
2	6	0	7	7	0	3	0	0	0	0	0	0	0	0	0
0	8	0	4	21	38	0	50	0	0	0	0	0	0	0	0
1	5	0	4	14	1	8	0	0	0	0	0	0	0	0	0

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Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1941	202	207	202	255	291	255	238	291
Number of PI	3	0	0	0	0	0	0	0	3
Number of DFF	8	0	0	0	0	4	3	0	1
Number of Combinational Nodes	1938	202	207	202	255	291	255	238	288
Number of PO	6	0	0	0	1	0	2	3	0
Number of Edges	6952	787	852	811	1029	1994	1276	894	2087
Number of Intra-Cluster Edges	4174	391	549	451	471	700	430	381	801
Number of Inter-Cluster Input Edges	5556	366	231	287	409	349	443	422	271
Number of Inter-Cluster Output Edges	5556	30	72	73	149	945	403	91	1015
Wirelength Approx	5.15e+06	507851	604925	567282	549526	886017	596199	514207	932619
Scaled Cost	3.10								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.5 ± 26	2.0 ± 8	3 ± 16	2.5 ± 13	2.4 ± 9	6 ± 40	3.2 ± 20	1.9 ± 10	6 ± 44
Avg. Comb. Fanout	1.8 ± 9	2.0 ± 8	3 ± 16	2.5 ± 13	2.4 ± 9	1 ± 0	1.2 ± 2.7	1.9 ± 10	1 ± 0
Avg. PI Fanout	382 ± 18	N/A	N/A	N/A	N/A	N/A	N/A	N/A	382 ± 18
Avg. DFF Fanout	283 ± 93	N/A	N/A	N/A	N/A	340 ± 23	174 ± 52	N/A	383 ± 0
Avg. Comb. Fanin	3.5 ± 0.6	3.7 ± 0.5	3.7 ± 0.5	3.6 ± 0.6	3.4 ± 0.7	3.6 ± 0.5	3.4 ± 0.6	3.3 ± 0.7	3.7 ± 0.4
Max Fanout	396	83	139	108	94	366	243	107	396

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	11	0	0	0	0	4	3	0	4	0	0	0	0	0	0	0	0	0
1	805	31	10	32	61	221	147	87	216	1	0	0	0	0	0	1	0	0
2	309	27	18	28	23	59	67	23	64	1	0	0	0	0	0	1	0	0
3	188	4	0	4	38	5	28	105	4	3	0	0	0	0	0	0	3	0
4	91	1	0	2	70	0	6	12	0	1	0	0	0	1	0	0	0	0
5	98	16	11	8	45	2	4	9	3	0	0	0	0	0	0	0	0	0
6	18	0	0	3	13	0	0	2	0	0	0	0	0	0	0	0	0	0
7	113	2	0	106	5	0	0	0	0	0	0	0	0	0	0	0	0	0
8	16	0	3	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	145	4	135	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	25	2	23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	7	2	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	85	83	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	21	21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	5	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	4	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	3409	0	0	0	0	1358	522	0	1529
1	2796	99	36	102	180	828	491	254	806	876	80	10	32	61	221	167	89	216
2	1044	100	49	89	66	190	238	73	239	763	27	18	28	208	59	106	253	64
3	719	16	0	14	152	20	107	394	16	262	4	0	4	110	5	28	107	4
4	322	4	0	8	249	0	22	39	0	199	1	0	3	177	0	6	12	0
5	349	57	33	23	167	8	15	35	11	99	16	11	9	45	2	4	9	3
6	60	0	0	9	44	0	0	7	0	338	0	0	323	13	0	0	2	0
7	450	8	0	424	18	0	0	0	0	112	2	0	105	5	0	0	0	0
8	62	0	12	50	0	0	0	0	0	430	0	417	13	0	0	0	0	0
9	574	16	539	19	0	0	0	0	0	144	4	134	6	0	0	0	0	0
10	96	8	88	0	0	0	0	0	0	37	14	23	0	0	0	0	0	0
11	23	6	17	0	0	0	0	0	0	165	160	5	0	0	0	0	0	0
12	337	331	6	0	0	0	0	0	0	84	82	2	0	0	0	0	0	0
13	82	82	0	0	0	0	0	0	0	21	21	0	0	0	0	0	0	0
14	17	17	0	0	0	0	0	0	0	5	5	0	0	0	0	0	0	0
15	13	13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	5336	319	508	400	300	582	340	286	701
2	0	0	0	0	0	0	0	0	0	914	27	6	17	102	105	78	80	92
3	0	0	0	0	0	0	0	0	0	249	7	0	5	56	8	10	11	2
4	1	0	0	0	1	0	0	0	0	136	11	14	5	13	3	2	4	4
5	0	0	0	0	0	0	0	0	0	143	2	0	22	0	2	0	0	2
6	0	0	0	0	0	0	0	0	0	37	0	0	2	0	0	0	0	0
7	1	0	0	1	0	0	0	0	0	61	13	18	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	18	0	3	0	0	0	0	0	0
9	1	0	1	0	0	0	0	0	0	26	2	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	22	9	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	2	1	0	0	0	0	0	0	0
12	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	4	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	4	3	0	1	0	0	5	1	1	1	0	0	0	0
1	0	169	87	158	255	322	368	323	218	5336	14	27	28	69	685	245	15	817
2	0	31	43	54	56	23	62	87	51	914	1	2	20	8	150	97	11	118
3	0	51	0	11	65	0	13	10	0	249	0	42	0	10	47	17	1	33
4	1	9	15	36	19	1	0	0	0	136	1	0	0	5	13	12	30	19
5	0	43	33	26	10	0	0	1	2	143	3	0	24	22	36	15	0	15
6	0	2	31	2	0	0	0	0	0	37	1	0	0	7	2	4	21	0
7	1	9	21	0	0	0	0	0	0	61	5	0	0	7	4	8	1	5
8	0	15	0	0	0	0	0	0	0	18	0	0	0	14	0	0	1	0
9	1	23	1	0	0	0	0	0	0	26	0	0	0	6	2	4	11	1
10	0	13	0	0	0	0	0	0	0	22	0	0	0	0	5	1	0	7
11	0	1	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	0
12	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (9 1891 3 1 0 1 0 2 0 0 0 0 0 0 0 0 1 2 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 3 2 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 1 0 0 1)
Cluster 1: (5 190 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1)
Cluster 2: (1 203 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3)
Cluster 3: (1 196 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2)
Cluster 4: (0 248 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 2 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1 0)
Cluster 5: (0 287 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (0 249 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 7: (2 231 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 8: (0 287 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	7	4	8	0	1	5	0	0	0	0	0	4	0	0	1
71	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
30	37	0	2	0	1	1	1	0	0	0	0	0	1	0	0
44	42	37	0	2	7	13	3	0	0	0	0	0	1	0	0
67	43	84	149	0	240	155	207	0	0	0	0	0	0	0	0
56	34	42	68	90	0	53	60	0	0	0	0	0	0	0	0
17	21	34	16	0	3	0	0	0	0	0	0	0	0	0	0
81	47	86	162	254	191	194	0	0	0	0	0	0	0	0	0

s38417

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	7465	852	994	1119	853	1030	832	876	909
Number of PI	28	19	0	0	0	0	1	1	7
Number of DFF	1463	190	134	218	159	180	166	162	254
Number of Combinational Nodes	7437	833	994	1119	853	1030	831	875	902
Number of PO	57	19	0	3	0	2	0	0	33
Number of Edges	22269	2644	3416	5065	2825	4350	2691	2979	2510
Number of Intra-Cluster Edges	17882	1841	2501	3074	1875	2881	1837	1985	1881
Number of Inter-Cluster Input Edges	8598	502	736	248	715	240	637	766	360
Number of Inter-Cluster Output Edges	8598	301	179	1743	229	1229	216	228	269
Wirelength Approx	1.54e+07	1.74e+06	1.86e+06	2.56e+06	2.01e+06	2.19e+06	1.75e+06	1.87e+06	1.47e+06
Scaled Cost	0.90								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.9 ± 17	2.5 ± 3.1	2.6 ± 3.4	4 ± 34	2.4 ± 2.9	3.9 ± 28	2.4 ± 2.4	2.5 ± 2.9	2.3 ± 3.4
Avg. Comb. Fanout	2.0 ± 4	2.1 ± 2.8	2.4 ± 3.5	1.8 ± 7	2.0 ± 2.7	1.7 ± 6	2.0 ± 2.3	2.1 ± 2.5	1.8 ± 2.3
Avg. PI Fanout	3.4 ± 8	1.1 ± 0.6	N/A	N/A	N/A	N/A	14 ± 0	44 ± 0	2.4 ± 1.2
Avg. DFF Fanout	7 ± 37	3.7 ± 3.7	4 ± 1.7	14 ± 74	4 ± 2.9	14 ± 66	4 ± 2.0	4 ± 1.9	3.6 ± 5
Avg. Comb. Fanin	3.4 ± 0.5	3.4 ± 0.6	3.5 ± 0.5	3.5 ± 0.6	3.4 ± 0.6	3.4 ± 0.5	3.4 ± 0.5	3.5 ± 0.5	3.4 ± 0.6
Max Fanout	661	41	40	661	38	522	17	44	30

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1491	209	134	218	159	180	167	163	261	47	19	0	3	0	2	0	0	23
1	2233	194	170	459	218	432	253	257	250	1	0	0	0	0	0	0	0	1
2	819	59	58	99	65	149	122	120	147	2	0	0	0	0	0	0	0	2
3	1056	141	195	135	138	110	130	127	80	3	0	0	0	0	0	0	0	3
4	546	76	121	61	73	45	65	67	38	1	0	0	0	0	0	0	0	1
5	381	33	55	53	48	52	50	65	25	3	0	0	0	0	0	0	0	3
6	329	33	63	31	35	38	26	51	52	0	0	0	0	0	0	0	0	0
7	159	14	31	30	22	6	7	13	36	0	0	0	0	0	0	0	0	0
8	159	20	36	24	25	15	9	10	20	0	0	0	0	0	0	0	0	0
9	141	32	57	9	34	3	3	3	0	0	0	0	0	0	0	0	0	0
10	112	29	56	0	27	0	0	0	0	0	0	0	0	0	0	0	0	0
11	39	12	18	0	9	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	9685	646	533	3106	612	2573	662	663	890
1	7260	606	539	1563	705	1460	787	809	791	3239	220	210	682	239	692	389	354	453
2	2826	202	201	317	224	528	421	407	526	3014	369	588	284	356	315	421	491	190
3	3735	481	648	508	468	384	488	474	284	1961	286	483	242	299	139	185	197	130
4	2051	280	456	241	276	158	249	258	133	1055	115	209	105	135	136	125	164	66
5	1460	122	207	197	183	208	195	254	94	648	67	108	82	67	73	59	102	90
6	1206	120	225	112	124	127	99	196	203	469	60	116	51	70	15	28	51	78
7	598	50	111	120	83	24	28	50	132	304	42	83	30	54	18	21	27	29
8	600	78	142	78	91	57	36	40	78	195	46	85	9	46	3	3	3	0
9	517	121	218	27	124	9	9	9	0	197	55	96	0	46	0	0	0	0
10	436	113	218	0	105	0	0	0	0	39	12	18	0	9	0	0	0	0
11	117	36	54	0	27	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	336	85	24	19	53	18	41	48	48	0	0	0	0	6	0	1	0	0
1	198	46	0	69	19	1	5	2	56	15773	1349	1779	2438	1391	2350	1459	1568	1293
2	163	4	0	1	0	37	39	36	46	2166	195	270	202	189	316	262	251	307
3	216	23	9	68	19	37	22	11	27	1045	150	189	175	120	73	31	46	139
4	86	15	26	0	13	14	7	4	7	447	40	74	61	44	46	23	39	56
5	102	4	4	12	11	0	31	36	4	411	23	46	66	34	15	44	57	25
6	64	1	0	18	3	24	6	12	0	229	11	25	51	16	48	6	12	7
7	31	1	2	9	1	0	0	2	16	198	23	38	33	28	3	3	3	40
8	81	3	5	21	7	12	6	7	20	159	7	5	30	8	24	6	6	14
9	54	9	15	9	12	3	3	3	0	105	10	9	18	12	6	3	3	0
10	93	21	48	0	24	0	0	0	0	195	21	48	0	24	0	0	0	0
11	39	12	18	0	9	0	0	0	0	78	12	18	0	9	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	336	134	218	159	180	166	162	254	0	0	224	151	226	171	146	160	161	224
1	198	250	299	69	374	62	390	419	283	15773	59	20	994	47	915	39	48	24
2	163	27	27	4	33	0	21	25	37	2166	9	8	79	5	56	8	3	6
3	216	11	23	15	16	11	9	2	35	1045	8	0	54	3	34	9	8	6
4	86	10	27	1	14	0	7	1	4	447	1	0	46	1	7	0	8	1
5	102	0	4	0	20	1	33	42	1	411	0	0	51	0	44	0	0	6
6	64	5	16	0	14	0	6	12	0	229	0	0	44	0	9	0	0	0
7	31	8	12	0	6	0	0	1	0	198	0	0	26	0	0	0	0	1
8	81	9	21	0	16	0	6	7	0	159	0	0	44	2	12	0	0	1
9	54	9	20	0	9	0	3	3	0	105	0	0	38	0	6	0	0	0
10	93	27	51	0	24	0	0	0	0	195	0	0	102	0	0	0	0	0
11	39	12	18	0	9	0	0	0	0	78	0	0	39	0	0	0	0	0

Fanout Distribution
Circuit: (1287 3490 656 497 394 462 144 103 90 73 46 41 55 45 13 16 8 4 6 4 1 1 4 1 1 2 1 0 1 0 1, 0 1 1 0 0 0 0 1 1 1 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (180 370 66 73 35 34 22 16 13 12 8 5 4 2 7 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0, 0 0 0 0 1)
Cluster 2: (133 504 60 80 24 62 24 31 13 13 9 14 9 5 4 4 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0, 0 0 1 1)
Cluster 3: (207 539 74 76 68 82 20 8 9 6 2 6 1 4 0 4 2 1 2 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (141 417 53 57 48 51 17 18 9 15 9 2 6 3 1 2 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1)
Cluster 5: (142 543 101 27 54 70 33 5 15 4 1 0 4 24 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0)
Cluster 6: (139 356 88 53 59 64 13 10 18 9 6 4 9 1 0 1 1 1)
Cluster 7: (133 388 75 84 66 68 6 6 7 9 3 7 16 4 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 1)
Cluster 8: (212 373 139 47 40 31 9 9 6 5 8 3 6 2 1 3 0 0 1 3 1 1 3 1 0 2 1 0 1 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	14	38	10	0	1	3	11	188	0	16	9	7	1	0	3
10	0	2	10	0	3	3	0	1	134	0	0	15	0	0	1
343	488	0	492	18	63	103	10	0	0	202	0	9	0	0	15
2	4	40	0	0	0	3	9	1	0	0	150	6	12	0	2
10	12	9	18	0	388	374	272	0	0	0	0	139	0	0	7
0	0	0	0	25	0	5	26	0	0	0	0	3	153	1	3
1	0	0	5	16	13	0	32	0	0	0	0	0	0	161	0
2	0	0	0	15	7	21	0	0	0	0	0	1	0	0	223

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Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	7489	1121	894	904	894	919	918	919	920
Number of PI	37	13	4	0	10	0	10	0	0
Number of DFF	1260	249	165	139	161	160	125	117	144
Number of Combinational Nodes	7452	1108	890	904	884	919	908	919	920
Number of PO	248	64	36	27	42	17	41	9	12
Number of Edges	21553	5603	2680	2880	2757	2875	3045	3093	2742
Number of Intra-Cluster Edges	17192	2662	1917	1930	1928	2037	2493	2212	2008
Number of Inter-Cluster Input Edges	8483	302	551	619	559	567	392	609	518
Number of Inter-Cluster Output Edges	8483	2636	212	330	270	270	160	272	216
Wirelength Approx	1.61e+07	2.16e+06	1.45e+06	2.01e+06	1.49e+06	1.86e+06	2.85e+06	2.25e+06	2.01e+06
Scaled Cost	0.90								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.8 ± 32	5 ± 82	2.3 ± 4	2.5 ± 9	2.4 ± 4	2.5 ± 3.8	2.8 ± 7	2.7 ± 8	2.4 ± 4
Avg. Comb. Fanout	1.6 ± 4	1.3 ± 1.5	1.3 ± 1.6	1.2 ± 1.4	1.4 ± 1.9	1.6 ± 3.1	2.4 ± 7	2.0 ± 8	1.7 ± 3.6
Avg. PI Fanout	81 ± 444	222 ± 727	2 ± 1.7	N/A	2.7 ± 1.5	N/A	6 ± 8	N/A	N/A
Avg. DFF Fanout	7 ± 9	5 ± 6	7 ± 7	9 ± 22	7 ± 8	6 ± 4	5 ± 7	7 ± 7	6 ± 4
Avg. Comb. Fanin	3.2 ± 0.8	3.2 ± 0.8	3.2 ± 0.8	3.1 ± 0.8	3.2 ± 0.9	3.2 ± 0.8	3.5 ± 0.7	3.3 ± 0.8	3.2 ± 0.8
Max Fanout	2741	2741	40	187	40	36	152	165	34

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	1297	262	169	139	171	160	135	117	144	167	42	28	27	29	12	16	4	9
1	3140	490	394	536	405	370	234	342	369	45	15	6	0	10	1	11	1	1
2	1326	199	191	129	185	163	152	200	107	13	3	2	0	1	2	1	3	1
3	1033	114	99	73	93	147	138	164	205	3	0	0	0	1	1	0	0	1
4	479	35	37	20	36	56	107	96	92	6	3	0	0	1	1	0	1	0
5	124	13	4	7	4	13	80	0	3	1	1	0	0	0	0	0	0	0
6	43	6	0	0	0	6	31	0	0	0	0	0	0	0	0	0	0	0
7	33	2	0	0	0	3	28	0	0	12	0	0	0	0	0	12	0	0
8	9	0	0	0	0	1	8	0	0	0	0	0	0	0	0	0	0	0
9	5	0	0	0	0	0	5	0	0	1	0	0	0	0	0	1	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	11047	4073	1097	1265	1152	1025	735	830	870
1	8550	1397	1062	1491	1113	986	661	894	946	5354	635	569	652	599	629	701	975	594
2	5164	760	740	511	712	629	602	791	419	2341	234	220	130	207	321	433	397	399
3	3988	439	369	282	350	569	549	634	796	1120	70	70	64	69	136	331	166	214
4	1818	127	142	79	136	214	407	358	355	239	14	6	10	6	17	181	0	5
5	438	44	16	25	16	42	285	0	10	124	19	0	0	0	15	90	0	0
6	166	24	0	0	0	24	118	0	0	49	4	0	0	0	4	41	0	0
7	116	8	0	0	0	11	97	0	0	13	0	0	0	0	1	12	0	0
8	36	0	0	0	0	4	32	0	0	6	0	0	0	0	0	6	0	0
9	17	0	0	0	0	0	17	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	153	37	25	27	30	11	15	0	8	0	3	0	1	0	1	0	0	0
1	150	56	6	0	12	12	54	1	9	15778	2092	1552	1724	1567	1534	1782	1705	1508
2	296	68	58	65	51	32	9	4	9	2940	374	274	154	271	343	480	362	326
3	259	53	43	30	39	45	7	16	26	1150	144	83	44	83	112	99	118	145
4	332	27	31	10	29	49	4	95	87	239	19	6	6	5	24	33	27	28
5	31	4	4	7	4	4	5	0	3	99	28	2	2	2	15	36	0	1
6	17	2	0	0	0	3	12	0	0	37	3	0	0	0	7	24	0	0
7	13	2	0	0	0	2	9	0	0	36	2	0	0	0	1	29	0	0
8	5	0	0	0	0	1	4	0	0	11	0	0	0	0	1	8	0	0
9	4	0	0	0	0	0	4	0	0	3	0	0	0	0	0	2	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	153	165	139	161	160	125	117	144	0	0	249	167	139	165	159	123	116	142
1	150	122	308	396	300	292	186	325	385	15778	1762	40	157	79	89	27	125	35
2	296	13	53	32	53	75	48	46	36	2940	251	5	17	19	6	9	27	22
3	259	2	45	23	42	54	30	60	66	1150	261	0	17	7	15	1	4	17
4	332	0	4	5	2	15	2	34	29	239	90	0	0	0	1	0	0	0
5	31	0	2	2	2	3	2	0	2	99	13	0	0	0	0	0	0	0
6	17	0	0	0	0	1	2	0	0	37	3	0	0	0	0	0	0	0
7	13	0	0	0	0	1	3	0	0	36	4	0	0	0	0	0	0	0
8	5	0	0	0	0	1	1	0	0	11	2	0	0	0	0	0	0	0
9	4	0	0	0	0	0	1	0	0	3	1	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (1177 4366 415 512 212 188 119 74 60 22 37 38 45 24 11 6 21 9 6 10 8 19 6 6 3 7 12 12 6 4, 7 12 1 3 10 2 1 0 3 0 4 0 1 0 0 0 0 0 0 1 1 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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Cluster 1: (237 576 85 54 49 29 17 17 12 3 9 6 6 3 0 2 3 1 0 0 1 0 0 0 0 0 0 2 2 0 1 0 1 1 1 0 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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Fanout Distribution
Cluster 2: (149 506 54 69 25 8 19 17 9 2 5 1 4 4 1 1 4 0 1 2 1 0 1 0 0 0 5 0 1 1 1 1 0 0 0 0 0 0 1, 0 1)
Cluster 3: (112 600 29 83 14 20 7 7 3 0 0 0 1 3 0 0 6 0 0 2 0 1 1 1 0 0 0 7 2 0 2 1 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (147 505 59 69 24 13 15 10 8 2 2 1 4 7 2 1 4 4 1 2 1 0 0 0 0 1 4 3 1 0 1 0 0 1 0 0 0 0, 1 0 1)
Cluster 5: (153 504 46 53 29 38 18 10 13 9 8 8 12 2 1 1 0 0 2 1 1 2 1 0 0 0 2 0 0 0 0 2 0 0 2 0 1)
Cluster 6: (125 549 41 67 27 36 14 6 8 2 1 0 1 3 0 1 3 3 0 1 2 4 2 4 0 3 1 0 0 2 1 2 0 0 0 2 0 0 1, 0 1 0 1 0 0 0 0 0 0 0 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (119 581 54 60 17 15 14 0 3 0 6 11 4 0 6 0 0 0 1 0 0 12 0 1 2 3 0 0 0 1 1 2 0 1 3 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (135 545 47 57 27 29 15 7 4 4 6 11 13 2 1 0 1 1 1 2 2 0 1 0 1 0 0 0 0 0 0 4 0 0 4)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	326	401	317	376	218	359	390	238	3	1	1	3	2	0	1
25	0	12	8	0	0	0	0	5	162	0	0	0	0	0	0
59	52	0	61	6	3	2	8	1	0	137	1	0	0	0	0
19	24	41	0	0	9	12	0	5	0	0	159	0	0	1	0
11	0	0	0	0	27	51	22	0	0	0	0	157	1	0	1
7	5	0	5	16	0	4	0	0	0	1	0	0	122	0	0
11	5	4	8	27	3	0	98	0	0	0	0	0	0	116	0
5	0	0	0	17	15	37	0	0	0	0	0	0	0	0	142

scale125_chip

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	3856	466	473	466	578	467	467	468	471
Number of PI	21	0	0	0	1	0	0	9	11
Number of DFF	1236	239	197	208	147	92	168	111	74
Number of Combinational Nodes	3835	466	473	466	577	467	467	459	460
Number of PO	80	0	3	0	0	22	32	8	15
Number of Edges	9823	1125	1343	1153	3661	1641	1285	1388	1429
Number of Intra-Cluster Edges	6472	441	595	458	1443	964	673	839	1014
Number of Inter-Cluster Input Edges	6553	426	488	452	178	498	430	372	313
Number of Inter-Cluster Output Edges	6553	258	245	243	2040	153	178	177	102
Wirelength Approx	6.34e+06	553797	599564	510690	1.43e+06	852438	750102	752763	893271
Scaled Cost	1.28								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.5 ± 35	1.5 ± 6	1.7 ± 2.2	1.5 ± 1.4	6 ± 90	2.3 ± 7	1.8 ± 7	2.1 ± 3.0	2.3 ± 2.8
Avg. Comb. Fanout	1.7 ± 10	1.6 ± 9	1.1 ± 0.4	1.2 ± 1.4	2.4 ± 21	1.6 ± 6	1.6 ± 9	1.6 ± 2.2	2.1 ± 2.6
Avg. PI Fanout	103 ± 454	N/A	N/A	N/A	2135 ± 0	N/A	N/A	1.1 ± 0.3	1.0 ± 0.2
Avg. DFF Fanout	2.4 ± 3.7	1.3 ± 0.5	2.5 ± 3.3	1.8 ± 1.3	2 ± 0.5	5 ± 9	2.0 ± 3.1	3.7 ± 5	3.8 ± 3.2
Avg. Comb. Fanin	3.3 ± 0.8	2.9 ± 0.9	3.1 ± 0.9	2.9 ± 0.9	3.5 ± 0.7	3.4 ± 0.7	3.3 ± 0.9	3.2 ± 0.8	3.4 ± 0.7
Max Fanout	2135	140	39	24	2135	103	120	29	23

Node Shape										PO Shape									
Delay Level	Circuit	Cluster								Circuit	Cluster								
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8	
0	1257	239	197	208	148	92	168	120	85	0	0	0	0	0	0	0	0	0	
1	865	103	151	129	61	98	115	132	76	80	0	3	0	0	22	32	8	15	
2	299	1	22	14	4	39	113	76	30	0	0	0	0	0	0	0	0	0	
3	380	123	22	15	2	122	46	36	14	0	0	0	0	0	0	0	0	0	
4	419	0	21	29	291	20	25	28	5	0	0	0	0	0	0	0	0	0	
5	169	0	22	54	71	3	0	13	6	0	0	0	0	0	0	0	0	0	
6	53	0	16	8	0	15	0	10	4	0	0	0	0	0	0	0	0	0	
7	44	0	18	7	1	9	0	5	4	0	0	0	0	0	0	0	0	0	
8	20	0	4	2	0	4	0	3	7	0	0	0	0	0	0	0	0	0	
9	21	0	0	0	0	7	0	7	7	0	0	0	0	0	0	0	0	0	
10	67	0	0	0	0	37	0	23	7	0	0	0	0	0	0	0	0	0	
11	47	0	0	0	0	18	0	8	21	0	0	0	0	0	0	0	0	0	
12	39	0	0	0	0	2	0	6	31	0	0	0	0	0	0	0	0	0	
13	43	0	0	0	0	0	0	1	42	0	0	0	0	0	0	0	0	0	
14	36	0	0	0	0	1	0	0	35	0	0	0	0	0	0	0	0	0	
15	27	0	0	0	0	0	0	0	27	0	0	0	0	0	0	0	0	0	
16	24	0	0	0	0	0	0	0	24	0	0	0	0	0	0	0	0	0	
17	21	0	0	0	0	0	0	0	21	0	0	0	0	0	0	0	0	0	
18	14	0	0	0	0	0	0	0	14	0	0	0	0	0	0	0	0	0	
19	8	0	0	0	0	0	0	0	8	0	0	0	0	0	0	0	0	0	
20	3	0	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0	

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	5222	332	511	386	2429	492	350	428	294
1	2082	213	390	274	126	263	281	335	200	643	4	22	20	5	98	214	152	128
2	1145	4	87	56	14	135	452	298	99	625	140	22	12	5	179	128	95	44
3	1403	453	86	55	8	471	160	118	52	851	0	20	14	623	90	24	66	14
4	1662	0	82	116	1164	77	99	104	20	367	0	23	52	247	6	0	31	8
5	575	0	88	198	213	12	0	41	23	69	0	16	8	0	16	0	23	6
6	205	0	64	32	0	56	0	38	15	91	0	18	8	0	24	0	36	5
7	165	0	66	26	4	36	0	18	15	37	0	4	2	0	8	0	7	16
8	72	0	12	6	0	15	0	11	28	42	0	0	0	0	14	0	13	15
9	75	0	0	0	0	27	0	28	20	94	0	0	0	0	43	0	26	25
10	253	0	0	0	0	135	0	91	27	83	0	0	0	0	34	0	23	26
11	166	0	0	0	0	55	0	31	80	84	0	0	0	0	4	0	5	75
12	143	0	0	0	0	8	0	22	113	111	0	0	0	0	0	0	1	110
13	150	0	0	0	0	0	0	2	148	69	0	0	0	0	0	0	0	69
14	132	0	0	0	0	4	0	0	128	54	0	0	0	0	1	0	0	53
15	94	0	0	0	0	0	0	0	94	53	0	0	0	0	0	0	0	53
16	93	0	0	0	0	0	0	0	93	41	0	0	0	0	0	0	0	41
17	80	0	0	0	0	0	0	0	80	32	0	0	0	0	0	0	0	32
18	52	0	0	0	0	0	0	0	52	15	0	0	0	0	0	0	0	15
19	31	0	0	0	0	0	0	0	31	4	0	0	0	0	0	0	0	4
20	9	0	0	0	0	0	0	0	9	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	15	0	0	26	4	0	0
1	599	100	132	117	57	24	80	73	16	4886	235	369	264	905	552	457	545	606
2	40	0	10	6	1	2	8	6	7	902	0	43	24	12	81	191	153	117
3	198	123	10	9	0	33	22	1	0	933	206	40	25	3	188	25	44	47
4	110	0	10	6	44	17	25	8	0	827	0	37	42	520	12	0	36	18
5	141	0	14	50	71	0	0	6	0	234	0	44	74	0	7	0	16	12
6	19	0	8	4	0	7	0	0	0	137	0	30	16	0	24	0	5	15
7	24	0	16	5	1	2	0	0	0	103	0	28	11	3	6	0	9	11
8	6	0	4	2	0	0	0	0	0	72	0	4	2	0	36	0	8	9
9	0	0	0	0	0	0	0	0	0	57	0	0	0	0	23	0	13	4
10	13	0	0	0	0	7	0	6	0	97	0	0	0	0	31	0	6	27
11	18	0	0	0	0	14	0	4	0	74	0	0	0	0	2	0	1	35
12	12	0	0	0	0	2	0	5	5	63	0	0	0	0	2	0	3	27
13	10	0	0	0	0	0	0	1	9	32	0	0	0	0	0	0	0	14
14	16	0	0	0	0	0	0	0	16	34	0	0	0	0	0	0	0	1
15	10	0	0	0	0	0	0	0	10	42	0	0	0	0	0	0	0	24
16	4	0	0	0	0	0	0	0	4	45	0	0	0	0	0	0	0	25
17	4	0	0	0	0	0	0	0	4	28	0	0	0	0	0	0	0	10
18	5	0	0	0	0	0	0	0	5	11	0	0	0	0	0	0	0	6
19	4	0	0	0	0	0	0	0	4	8	0	0	0	0	0	0	0	6
20	3	0	0	0	0	0	0	0	3	2	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	197	208	147	92	168	111	74	0	0	223	204	199	174	108	135	110	83
1	599	105	147	191	24	107	145	150	84	4886	23	23	1	808	23	20	42	13
2	40	0	22	14	2	31	115	71	26	902	3	0	0	270	6	1	1	0
3	198	124	24	15	0	134	35	13	10	933	7	0	2	313	11	19	2	1
4	110	0	23	29	60	5	24	16	5	827	2	17	41	96	1	2	2	1
5	141	0	22	38	0	7	0	9	5	234	0	1	0	74	1	1	0	4
6	19	0	18	8	0	11	0	5	5	137	0	0	0	43	0	0	4	0
7	24	0	20	8	0	3	0	0	4	103	0	0	0	31	0	0	4	0
8	6	0	4	2	0	0	0	1	6	72	0	0	0	9	0	0	4	0
9	0	0	0	0	0	6	0	7	4	57	0	0	0	14	1	0	2	0
10	13	0	0	0	0	13	0	18	2	97	0	0	0	31	0	0	2	0
11	18	0	0	0	0	10	0	3	23	74	0	0	0	33	0	0	3	0
12	12	0	0	0	0	2	0	4	25	63	0	0	0	29	1	0	1	0
13	10	0	0	0	0	0	0	1	17	32	0	0	0	18	0	0	0	0
14	16	0	0	0	0	1	0	0	32	34	0	0	0	32	1	0	0	0
15	10	0	0	0	0	0	0	0	18	42	0	0	0	18	0	0	0	0
16	4	0	0	0	0	0	0	0	20	45	0	0	0	20	0	0	0	0
17	4	0	0	0	0	0	0	0	18	28	0	0	0	18	0	0	0	0
18	5	0	0	0	0	0	0	0	5	11	0	0	0	5	0	0	0	0
19	4	0	0	0	0	0	0	0	2	8	0	0	0	2	0	0	0	0
20	3	0	0	0	0	0	0	0	2	2	0	0	0	2	0	0	0	0

Fanout Distribution
Circuit: (1291 1527 626 102 92 45 36 33 25 21 11 4 6 4 5 2 3 2 5 0 0 1 0 2 2 0 0 0 0 1 0 0 0 0 0 0, 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (222 152 89 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (207 94 119 15 17 6 4 1 3 0 2 1 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (199 130 111 6 7 4 0 4 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 4: (174 263 133 1 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (125 242 24 13 7 4 11 11 6 6 6 2 2 1 2 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Fanout Distribution
Cluster 6: (167 209 55 8 24 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 7: (113 224 46 17 11 15 10 7 7 7 0 0 1 0 3 1 2 0 1 0 0 1 0 1 0 0 0 0 0 1)
Cluster 8: (84 213 49 40 24 15 10 10 5 8 3 1 0 3 0 1 0 1 3 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	0	4	6	2	23	0	0	207	0	0	0	7	9	0	0
0	0	1	33	0	0	7	0	1	188	15	0	0	0	0	0
1	0	0	42	0	1	0	0	28	0	168	0	0	3	0	0
224	267	300	0	276	273	268	258	2	0	25	147	0	0	0	0
0	0	0	0	0	20	7	18	0	0	0	0	82	26	0	0
4	0	0	0	35	0	4	0	1	0	0	0	0	130	4	0
0	13	0	5	10	2	0	37	0	9	0	0	2	0	99	0
0	0	0	0	7	0	12	0	0	0	0	0	1	0	8	74

scale2_chip

Basic Statistics	Circuit	Cluster 1	2	3	4	5	6	7	8
Number of Nodes	1524	181	180	190	193	173	194	185	228
Number of PI	12	1	0	10	0	0	0	0	1
Number of DFF	370	73	47	41	25	70	50	29	35
Number of Combinational Nodes	1512	180	180	180	193	173	194	185	227
Number of PO	70	8	2	1	2	12	26	10	9
Number of Edges	4131	468	524	586	672	464	589	613	1488
Number of Intra-Cluster Edges	2811	208	311	334	455	128	353	393	616
Number of Inter-Cluster Input Edges	2593	165	150	150	189	222	164	163	57
Number of Inter-Cluster Output Edges	2593	95	63	95	28	108	72	57	815
Wirelength Approx	747241	62472	82979	94135	99116	64887	98793	106021	138838
Scaled Cost	1.47								

Fanout Statistics	Circuit	Cluster 1	2	3	4	5	6	7	8
Avg. Fanout	2.7 ± 22	1.6 ± 1.9	2.0 ± 2.5	2.2 ± 3.8	2.5 ± 2.5	1.3 ± 1.2	2.1 ± 7	2.4 ± 3.0	6 ± 57
Avg. Comb. Fanout	1.6 ± 4	1.1 ± 0.9	1.4 ± 1.5	1.7 ± 2.7	1.8 ± 1.7	0.9 ± 0.3	2.1 ± 9	1.7 ± 2.2	1.7 ± 7
Avg. PI Fanout	72 ± 236	2 ± 0	N/A	1.1 ± 0.3	N/A	N/A	N/A	N/A	854 ± 0
Avg. DFF Fanout	3.7 ± 5	2.4 ± 2.6	3.7 ± 3.7	4 ± 6	7 ± 2.9	2.0 ± 1.7	2.4 ± 1.4	6 ± 4	7 ± 12
Avg. Comb. Fanin	3.2 ± 0.8	3.0 ± 0.9	3.1 ± 0.9	3.3 ± 0.8	3.4 ± 0.7	2.9 ± 0.9	3.3 ± 0.9	3.3 ± 0.7	3.5 ± 0.7
Max Fanout	854	16	15	29	13	11	75	15	854

Node Shape Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8	PO Shape Circuit	Cluster 1	2	3	4	5	6	7	8
0	382	74	47	51	25	70	50	29	36	0	0	0	0	0	0	0	0	0
1	392	71	59	48	51	54	29	40	40	70	8	2	1	2	12	26	10	9
2	231	10	16	47	8	24	73	30	23	0	0	0	0	0	0	0	0	0
3	179	9	15	9	8	18	25	18	77	0	0	0	0	0	0	0	0	0
4	79	9	6	8	9	7	17	8	15	0	0	0	0	0	0	0	0	0
5	31	4	4	0	6	0	0	4	13	0	0	0	0	0	0	0	0	0
6	21	2	3	1	11	0	0	1	3	0	0	0	0	0	0	0	0	0
7	35	0	6	11	3	0	0	2	13	0	0	0	0	0	0	0	0	0
8	29	1	6	9	2	0	0	6	5	0	0	0	0	0	0	0	0	0
9	56	0	14	5	4	0	0	31	2	0	0	0	0	0	0	0	0	0
10	35	0	4	1	16	0	0	13	1	0	0	0	0	0	0	0	0	0
11	21	1	0	0	18	0	0	2	0	0	0	0	0	0	0	0	0	0
12	18	0	0	0	17	0	0	1	0	0	0	0	0	0	0	0	0	0
13	9	0	0	0	9	0	0	0	0	0	0	0	0	0	0	0	0	0
14	5	0	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0
15	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8	Output Shape Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2248	179	177	186	174	143	121	182	1086
1	1014	193	151	124	139	124	62	114	107	509	13	51	84	61	8	166	76	50
2	865	37	52	173	30	92	292	106	83	378	15	28	47	15	18	89	51	115
3	689	34	56	35	30	70	100	64	300	154	15	19	9	14	4	20	20	53
4	234	32	20	25	34	14	34	26	49	71	5	12	0	15	0	0	9	30
5	121	16	16	0	23	0	0	16	50	56	4	4	0	37	0	0	4	7
6	81	8	12	3	43	0	0	4	11	49	2	4	11	17	0	0	2	13
7	137	0	24	43	12	0	0	8	50	50	0	8	15	3	0	0	12	12
8	106	4	24	32	7	0	0	23	16	76	0	15	17	7	0	0	34	3
9	209	0	55	20	16	0	0	113	5	71	0	9	4	28	0	0	30	0
10	111	0	10	4	58	0	0	37	2	45	0	0	1	41	0	0	3	0
11	80	2	0	0	70	0	0	8	0	26	0	0	0	25	0	0	1	0
12	61	0	0	0	59	0	0	2	0	21	0	0	0	21	0	0	0	0
13	35	0	0	0	35	0	0	0	0	6	0	0	0	6	0	0	0	0
14	16	0	0	0	16	0	0	0	0	1	0	0	0	1	0	0	0	0
15	2	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	7	0	6	0	0	0
1	157	53	29	35	0	36	0	0	4	2192	151	192	205	302	89	253	223	313
2	22	2	1	0	0	6	7	6	0	609	19	32	92	44	27	95	54	53
3	54	4	1	0	0	14	5	0	30	403	12	25	0	16	12	5	27	189
4	54	6	0	8	0	7	17	5	11	96	13	9	0	21	0	0	3	3
5	9	2	0	0	0	0	0	0	7	69	8	4	0	11	0	0	7	28
6	3	1	1	0	0	0	0	0	1	57	4	12	19	3	0	0	4	9
7	12	0	2	6	0	0	0	0	4	99	1	18	10	1	0	0	34	16
8	12	1	4	5	0	0	0	0	2	59	0	12	7	0	0	0	20	2
9	10	0	5	1	0	0	0	2	2	61	0	7	1	0	0	0	21	2
10	16	0	4	0	0	0	0	11	1	45	0	0	0	22	0	0	0	1
11	6	1	0	0	4	0	0	1	0	35	0	0	0	17	0	0	0	0
12	6	0	0	0	5	0	0	1	0	20	0	0	0	9	0	0	0	0
13	4	0	0	0	4	0	0	0	0	9	0	0	0	6	0	0	0	0
14	4	0	0	0	4	0	0	0	0	6	0	0	0	3	0	0	0	0
15	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	47	41	25	70	50	29	35	0	0	70	47	55	18	63	29	26	62
1	157	85	62	52	44	116	37	58	10	2192	14	13	36	7	14	41	6	333
2	22	9	12	40	4	25	76	24	3	609	2	2	3	2	9	2	1	172
3	54	9	6	1	8	24	5	20	44	403	3	1	1	1	22	0	23	66
4	54	8	1	8	5	7	17	1	0	96	1	0	0	0	0	0	0	46
5	9	4	1	2	3	0	0	1	0	69	4	0	0	0	0	0	0	7
6	3	2	2	0	2	0	0	0	0	57	1	0	0	0	0	0	0	5
7	12	0	5	11	1	0	0	2	0	99	0	0	0	0	0	0	0	19
8	12	0	5	6	1	0	0	6	0	59	0	0	0	0	0	0	1	17
9	10	0	14	5	4	0	0	7	0	61	0	0	0	0	0	0	0	30
10	16	0	1	0	14	0	0	7	0	45	0	0	0	0	0	0	0	22
11	6	1	0	0	16	0	0	1	0	35	0	0	0	0	0	0	0	18
12	6	0	0	0	10	0	0	1	0	20	0	0	0	0	0	0	0	11
13	4	0	0	0	3	0	0	0	0	9	0	0	0	0	0	0	0	3
14	4	0	0	0	3	0	0	0	0	6	0	0	0	0	0	0	0	3
15	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1

Fanout Distribution
Circuit: (419 705 158 50 46 22 29 24 13 12 9 5 7 3 3 4 2 0 1 0 1 1 1 0 2 1 0 0 0 1 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 1: (77 47 37 8 1 6 1 1 0 1 0 0 0 0 0 0 2)
Cluster 2: (48 74 27 7 6 3 3 4 2 1 1 0 0 0 2 2)
Cluster 3: (51 90 26 4 3 0 2 2 2 1 0 1 3 0 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 1)
Cluster 4: (13 108 20 12 5 3 11 9 4 3 2 0 1 2)
Cluster 5: (75 57 30 2 6 1 0 0 0 0 1 1)
Cluster 6: (55 109 0 7 19 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 7: (34 100 10 4 4 3 9 4 4 4 2 2 1 1 1 2)
Cluster 8: (66 120 8 6 2 6 3 4 1 2 3 1 2 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	12	5	7	0	0	0	1	66	0	0	0	4	0	0	0
7	0	0	0	2	0	0	7	0	43	0	0	4	0	0	0
11	0	0	12	7	4	6	0	6	3	35	7	2	0	2	0
2	1	5	0	0	0	2	0	0	0	0	18	0	0	0	0
0	0	5	0	0	8	7	25	0	0	2	0	55	6	0	0
0	0	0	0	43	0	0	0	1	0	4	0	0	24	0	0
0	0	1	3	3	0	0	24	0	0	0	0	1	0	25	0
98	96	109	97	117	123	113	0	0	1	0	0	4	20	2	35

seq

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1791	232	207	268	219	207	207	220	231
Number of PI	41	4	7	8	1	7	1	6	7
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	1750	228	200	260	218	200	206	214	224
Number of PO	35	5	5	0	6	7	6	3	3
Number of Edges	6158	1100	811	1619	951	822	816	1024	1078
Number of Intra-Cluster Edges	4095	526	440	789	441	422	414	479	584
Number of Inter-Cluster Input Edges	4126	275	255	129	324	284	323	266	207
Number of Inter-Cluster Output Edges	4126	299	116	701	186	116	79	279	287
Wirelength Approx	2.53e+06	310080	248763	474270	286000	275929	267592	316895	360189
Scaled Cost	2.59								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.4 ± 13	3.5 ± 10	2.6 ± 5	6 ± 27	2.8 ± 7	2.5 ± 5	2.3 ± 5	3.4 ± 12	3.7 ± 13
Avg. Comb. Fanout	2.1 ± 5	2.5 ± 6	2.1 ± 3.2	1.7 ± 2.5	2.8 ± 7	1.8 ± 2.6	2.2 ± 5	2.1 ± 6	1.7 ± 2.4
Avg. PI Fanout	57 ± 60	60 ± 33	19 ± 11	128 ± 89	1 ± 0	23 ± 12	20 ± 0	50 ± 41	67 ± 29
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.5 ± 0.6	3.5 ± 0.5	3.4 ± 0.6	3.5 ± 0.6	3.5 ± 0.5	3.5 ± 0.6	3.5 ± 0.6	3.4 ± 0.6	3.5 ± 0.6
Max Fanout	233	91	40	233	89	36	46	112	112

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	41	4	7	8	1	7	1	6	7	0	0	0	0	0	0	0	0	0
1	486	56	41	158	34	39	13	58	87	1	0	0	0	1	0	0	0	0
2	723	116	83	81	121	75	76	99	72	1	1	0	0	0	0	0	0	0
3	359	38	48	18	46	55	70	43	41	4	0	1	0	3	0	0	0	0
4	127	14	20	3	14	21	28	10	17	5	3	1	0	0	1	0	0	0
5	40	3	6	0	2	9	12	3	5	10	0	1	0	1	5	0	2	1
6	14	1	1	0	1	1	7	1	2	13	1	1	0	1	1	6	1	2
7	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2351	240	136	1026	1	159	20	298	471
1	1559	176	118	539	95	126	44	182	279	2246	398	214	349	427	175	172	289	222
2	2615	423	308	295	439	262	263	353	272	1030	135	133	94	141	125	177	117	108
3	1305	133	169	72	168	203	252	157	151	374	38	49	18	43	55	80	43	48
4	478	54	73	12	53	78	105	38	65	125	11	19	3	14	20	30	10	18
5	146	11	20	0	8	33	45	12	17	31	3	5	0	1	4	13	1	4
6	52	4	4	0	2	4	28	3	7	1	0	0	0	0	0	1	0	0
7	3	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	4903	450	344	624	397	315	353	387	444
2	0	0	0	0	0	0	0	0	0	1104	68	85	133	42	96	57	87	123
3	0	0	0	0	0	0	0	0	0	129	8	8	28	2	6	4	5	16
4	0	0	0	0	0	0	0	0	0	18	0	1	4	0	3	0	0	1
5	0	0	0	0	0	0	0	0	0	4	0	2	0	0	2	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	218	198	120	252	208	206	204	183	4903	250	106	508	165	75	69	214	202
2	0	51	54	8	64	65	103	49	19	1104	43	8	167	19	34	10	59	73
3	0	4	2	1	8	8	14	10	5	129	6	1	19	2	7	0	6	11
4	0	2	1	0	0	3	0	3	0	18	0	1	7	0	0	0	0	1
5	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (33 1311 151 77 40 25 20 15 10 8 7 12 5 3 6 2 7 4 1 4 8 3 1 1 2 0 0 1 1 1 1 1 0 1 1 1 1 0, 1 0 1 0 2 0 1 1 1 0 0 0 0 1 0 0 0 1 0 2 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0, 0 1 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 2 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 1: (4 174 15 9 4 3 3 2 3 1 0 1 0 1 1 1 2 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1)
Cluster 2: (5 145 15 9 9 4 4 1 1 1 0 3 0 0 2 0 0 1 0 1 2 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (0 210 19 13 2 4 1 3 1 3 1 0 1 0 0 0 1 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 4: (5 171 9 3 3 1 3 2 1 2 3 4 1 2 1 1 1 0 1 1 2 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 5: (7 140 24 12 5 3 0 0 1 0 3 3 1 0 1 0 1 0 0 1 1 0 0 1 0 0 0 0 0 0 0 1 1 0 1)
Cluster 6: (6 137 25 12 9 3 3 3 3 0 0 0 0 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 1)
Cluster 7: (3 169 20 5 3 3 4 2 0 0 0 1 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (3 165 24 14 5 4 2 2 0 1 0 0 1 0 0 0 1 0 0 0 1 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0, 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	72	27	58	27	19	54	42	0	0	0	0	0	0	0	0
30	0	17	20	13	19	13	4	0	0	0	0	0	0	0	0
149	80	0	166	66	105	76	59	0	0	0	0	0	0	0	0
24	38	24	0	41	16	23	20	0	0	0	0	0	0	0	0
18	0	14	9	0	55	6	14	0	0	0	0	0	0	0	0
4	16	17	4	22	0	12	4	0	0	0	0	0	0	0	0
31	41	19	38	39	47	0	64	0	0	0	0	0	0	0	0
19	8	11	29	76	62	82	0	0	0	0	0	0	0	0	0

smu_dpath

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	886	111	111	111	111	108	111	94	129
Number of PI	204	8	23	32	23	15	7	61	35
Number of DFF	190	41	38	7	30	31	36	5	2
Number of Combinational Nodes	682	103	88	79	88	93	104	33	94
Number of PO	166	8	22	27	24	15	4	33	33
Number of Edges	1857	293	278	353	282	334	427	91	374
Number of Intra-Cluster Edges	1247	140	147	195	130	129	232	56	215
Number of Inter-Cluster Input Edges	1185	107	10	95	81	131	26	30	92
Number of Inter-Cluster Output Edges	1185	46	121	60	71	74	169	5	67
Wirelength Approx	294099	34761	35406	41198	36549	42201	49984	8048	45952
Scaled Cost	1.13								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.0 ± 6	1.6 ± 3.0	2.4 ± 3.4	2.2 ± 6	1.8 ± 1.7	1.8 ± 1.8	3.6 ± 10	0.6 ± 0.4	2.1 ± 9
Avg. Comb. Fanout	1.2 ± 2.4	0.9 ± 0.2	0.9 ± 0.8	2.0 ± 5	0.9 ± 0.6	1.2 ± 0.7	1.4 ± 0.4	N/A	1.3 ± 3.0
Avg. PI Fanout	3.1 ± 11	5 ± 10	2.3 ± 6	3.0 ± 8	1 ± 0	1.4 ± 1.3	27 ± 30	1 ± 0	5 ± 16
Avg. DFF Fanout	3.1 ± 2.2	2.1 ± 1.0	4 ± 1.6	1.1 ± 1.6	4 ± 1.9	3.3 ± 2.7	3.2 ± 2.5	N/A	N/A
Avg. Comb. Fanin	3.3 ± 0.6	3.3 ± 0.5	3 ± 0	3.6 ± 0.5	3.1 ± 0.3	3.6 ± 0.4	3.7 ± 0.4	3 ± 0	3.3 ± 0.9
Max Fanout	95	32	32	33	5	7	62	1	95

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	394	49	61	39	53	46	43	66	37	32	3	5	3	5	5	4	5	2
1	147	41	17	27	18	13	1	28	2	73	4	0	24	6	10	0	28	1
2	68	0	2	24	6	5	0	0	31	1	0	1	0	0	0	0	0	0
3	42	0	2	21	9	7	0	0	3	2	0	1	0	0	0	0	0	1
4	14	0	2	0	0	8	0	0	4	3	0	1	0	0	0	0	0	2
5	14	0	2	0	0	8	0	0	4	3	0	1	0	0	0	0	0	2
6	14	0	2	0	0	8	0	0	4	3	0	1	0	0	0	0	0	2
7	14	0	2	0	0	7	1	0	4	3	0	1	0	0	0	0	0	2
8	15	1	2	0	0	4	4	0	4	3	0	1	0	0	0	0	0	2
9	15	1	2	0	0	2	6	0	4	3	0	1	0	0	0	0	0	2
10	15	1	2	0	0	0	8	0	4	3	0	1	0	0	0	0	0	2
11	15	1	2	0	0	0	8	0	4	3	0	1	0	0	0	0	0	2
12	16	2	2	0	0	0	8	0	4	3	0	1	0	0	0	0	0	2
13	14	0	2	0	0	0	8	0	4	3	0	1	0	0	0	0	0	2
14	16	2	2	0	0	0	8	0	4	3	0	1	0	0	0	0	0	2
15	14	1	2	0	0	0	7	0	4	3	0	1	0	0	0	0	0	2
16	13	2	2	0	0	0	5	0	4	3	0	1	0	0	0	0	0	2
17	11	3	2	0	0	0	3	0	3	3	0	1	0	0	0	0	0	2
18	7	3	1	0	1	0	1	0	1	2	0	1	0	0	0	0	0	1
19	4	2	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
20	3	1	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
21	3	1	0	0	2	0	0	0	0	2	1	0	0	1	0	0	0	0
22	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
23	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
24	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
25	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
26	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
27	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
28	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
29	2	0	0	0	2	0	0	0	0	1	0	0	0	1	0	0	0	0
30	2	0	0	0	2	0	0	0	0	2	0	0	0	2	0	0	0	0

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1181	123	214	103	139	107	280	56	159
1	445	125	51	81	54	41	2	84	7	150	3	0	104	6	6	0	0	31
2	269	0	6	96	24	19	0	0	124	72	0	2	24	6	9	0	0	31
3	152	0	6	83	27	26	0	0	10	15	0	2	0	0	10	0	0	3
4	48	0	6	0	0	30	0	0	12	16	0	2	0	0	10	0	0	4
5	48	0	6	0	0	30	0	0	12	16	0	2	0	0	10	0	0	4
6	48	0	6	0	0	30	0	0	12	16	0	2	0	0	10	0	0	4
7	48	0	6	0	0	26	4	0	12	16	0	2	0	0	8	2	0	4
8	52	4	6	0	0	14	16	0	12	17	1	2	0	0	2	8	0	4
9	52	4	6	0	0	8	22	0	12	17	1	2	0	0	0	10	0	4
10	52	4	6	0	0	0	30	0	12	17	1	2	0	0	0	10	0	4
11	52	4	6	0	0	0	30	0	12	17	1	2	0	0	0	10	0	4
12	56	8	6	0	0	0	30	0	12	18	2	2	0	0	0	10	0	4
13	48	0	6	0	0	0	30	0	12	16	0	2	0	0	0	10	0	4
14	56	8	6	0	0	0	30	0	12	17	2	2	0	0	0	9	0	4
15	48	4	6	0	0	0	26	0	12	14	1	2	0	0	0	7	0	4
16	44	8	6	0	0	0	18	0	12	12	2	2	0	0	0	4	0	4
17	37	12	6	0	0	0	11	0	8	9	3	2	0	0	0	1	0	3
18	24	12	3	0	3	0	4	0	2	6	3	0	0	2	0	0	0	1
19	14	8	0	0	6	0	0	0	0	4	2	0	0	2	0	0	0	0
20	10	4	0	0	6	0	0	0	0	3	1	0	0	2	0	0	0	0
21	10	4	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
22	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
23	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
24	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
25	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
26	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
27	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
28	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
29	6	0	0	0	6	0	0	0	0	2	0	0	0	2	0	0	0	0
30	6	0	0	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	64	4	5	3	5	18	22	5	2	0	0	0	3	0	0	0	0	0
1	66	36	17	0	12	0	1	0	0	812	93	82	89	67	82	66	56	66
2	0	0	0	0	0	0	0	0	0	247	3	4	105	6	7	0	0	64
3	31	0	0	21	9	1	0	0	0	53	1	4	1	9	8	0	0	6
4	2	0	0	0	0	2	0	0	0	39	3	4	0	0	8	0	0	6
5	2	0	0	0	0	2	0	0	0	38	2	4	0	0	8	0	0	6
6	2	0	0	0	0	2	0	0	0	34	0	4	0	0	8	0	0	6
7	2	0	0	0	0	2	0	0	0	38	1	4	0	0	6	2	0	6
8	2	0	0	0	0	2	0	0	0	38	3	4	0	0	2	12	0	6
9	2	0	0	0	0	2	0	0	0	40	4	4	0	0	0	16	0	6
10	2	0	0	0	0	0	2	0	0	38	3	4	0	0	0	20	0	6
11	2	0	0	0	0	0	2	0	0	38	2	4	0	0	0	20	0	6
12	2	0	0	0	0	0	2	0	0	38	4	4	0	0	0	20	0	6
13	2	0	0	0	0	0	2	0	0	34	0	4	0	0	0	20	0	6
14	2	0	0	0	0	0	2	0	0	38	4	4	0	0	0	20	0	6
15	2	0	0	0	0	0	2	0	0	33	2	4	0	0	0	17	0	6
16	2	0	0	0	0	0	2	0	0	28	4	4	0	0	0	11	0	5
17	2	0	0	0	0	0	2	0	0	20	5	4	0	0	0	6	0	2
18	1	0	0	0	0	0	1	0	0	11	4	1	0	0	0	2	0	0
19	0	0	0	0	0	0	0	0	0	6	2	0	0	4	0	0	0	0
20	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
21	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
22	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
23	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
24	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
25	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
26	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
27	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
28	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
29	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
30	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	64	38	7	30	31	36	5	2	0	0	40	22	24	26	31	40	5	2
1	66	54	2	45	39	8	3	28	32	812	3	50	23	18	29	38	0	50
2	0	1	0	19	0	7	0	0	31	247	2	32	1	14	1	7	0	1
3	31	1	0	1	9	11	0	0	2	53	1	0	9	1	2	10	0	1
4	2	2	0	0	0	14	0	0	2	39	0	2	0	0	2	12	0	2
5	2	2	0	0	0	14	0	0	2	38	0	2	0	0	2	12	0	2
6	2	0	0	0	0	14	0	0	2	34	0	2	0	0	2	12	0	0
7	2	3	0	0	0	13	1	0	2	38	0	2	0	0	3	11	0	3
8	2	1	0	0	0	8	0	0	2	38	0	2	0	0	2	6	0	1
9	2	2	0	0	0	6	0	0	2	40	0	2	0	0	0	6	0	2
10	2	1	0	0	0	0	2	0	2	38	0	2	0	0	0	2	0	1
11	2	2	0	0	0	0	2	0	2	38	0	2	0	0	0	2	0	2
12	2	0	0	0	0	0	2	0	2	38	0	0	1	1	0	2	0	0
13	2	0	0	0	0	0	2	0	2	34	0	0	0	2	0	2	0	0
14	2	0	0	0	0	0	2	0	2	38	0	0	0	2	0	2	0	0
15	2	0	0	0	0	0	2	0	2	33	0	0	0	2	0	2	0	0
16	2	0	0	0	0	0	2	0	2	28	0	0	0	2	0	2	0	0
17	2	0	0	0	0	0	2	0	1	20	0	0	0	2	0	1	0	0
18	1	0	1	0	2	0	1	0	0	11	0	1	2	1	0	0	0	0
19	0	0	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (262 389 127 3 1 84 7 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 3 0 3 2 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 1)
Cluster 1: (46 26 34 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 2: (44 17 16 0 0 33 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 3: (27 76 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 2 0 1 1)
Cluster 4: (44 31 12 0 0 24)
Cluster 5: (33 28 32 1 0 7 7 0)
Cluster 6: (26 33 32 1 1 15 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1)
Cluster 7: (38 56)
Cluster 8: (4 122 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	2	2	0	1	0	0	1	40	0	0	0	0	0	0	0
20	0	33	14	12	4	0	16	0	22	0	0	0	0	0	0
2	1	0	31	0	1	0	1	1	16	4	3	0	0	0	0
12	0	9	0	0	12	0	12	0	0	0	26	0	0	0	0
0	0	13	0	0	4	0	26	0	0	0	0	31	0	0	0
2	0	8	5	78	0	0	36	0	0	3	1	0	36	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	0
33	0	0	0	4	0	28	0	0	0	0	0	0	0	0	2

spla

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	3706	540	386	449	453	540	455	424	459
Number of PI	16	9	0	0	0	4	3	0	0
Number of DFF	0	0	0	0	0	0	0	0	0
Number of Combinational Nodes	3690	531	386	449	453	536	452	424	459
Number of PO	46	22	8	4	4	2	2	2	2
Number of Edges	13762	2365	1758	1950	2176	3171	2259	2059	2301
Number of Intra-Cluster Edges	9485	1691	784	1063	1161	1498	1203	939	1146
Number of Inter-Cluster Input Edges	8554	308	652	587	506	486	527	630	581
Number of Inter-Cluster Output Edges	8554	366	322	300	509	1187	529	490	574
Wirelength Approx	8.23e+06	1.06e+06	871981	927505	939788	1.29e+06	1.26e+06	918243	958678
Scaled Cost	2.65								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	3.7 ± 14	3.8 ± 12	2.8 ± 10	3.0 ± 10	3.6 ± 13	5 ± 19	3.8 ± 18	3.3 ± 11	3.7 ± 13
Avg. Comb. Fanout	3.4 ± 12	3.3 ± 11	2.8 ± 10	3.0 ± 10	3.6 ± 13	5 ± 18	2.4 ± 7	3.3 ± 11	3.7 ± 13
Avg. PI Fanout	69 ± 75	30 ± 24	N/A	N/A	N/A	48 ± 42	214 ± 0	N/A	N/A
Avg. DFF Fanout	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Avg. Comb. Fanin	3.7 ± 0.4	3.7 ± 0.4	3.7 ± 0.4	3.6 ± 0.4	3.6 ± 0.4	3.7 ± 0.4	3.8 ± 0.3	3.7 ± 0.4	3.7 ± 0.4
Max Fanout	214	141	136	116	125	154	214	135	129

Node Shape										PO Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	16	9	0	0	0	4	3	0	0	0	0	0	0	0	0	0	0	0
1	73	36	3	1	0	19	7	6	1	1	1	0	0	0	0	0	0	0
2	930	177	63	36	36	244	208	109	57	2	2	0	0	0	0	0	0	0
3	1585	208	198	233	227	177	141	185	216	3	3	0	0	0	0	0	0	0
4	733	91	78	119	124	63	68	67	123	5	5	0	0	0	0	0	0	0
5	238	16	24	39	43	21	17	35	43	13	10	2	0	0	1	0	0	0
6	85	3	13	13	13	9	8	15	11	3	1	0	1	0	0	1	0	0
7	32	0	4	5	7	2	2	5	7	5	0	3	0	1	0	0	0	1
8	14	0	3	3	3	1	1	2	1	14	0	3	3	3	1	1	2	1

Input Shape										Output Shape								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	1104	269	0	0	0	193	642	0	0
1	235	108	11	3	0	62	24	23	4	3674	972	268	14	0	1626	220	516	58
2	3569	685	240	140	137	918	821	412	216	6048	507	472	878	1202	595	621	586	1187
3	5857	783	733	842	825	643	527	686	818	1846	213	247	284	281	177	155	202	287
4	2722	350	287	442	462	237	253	240	451	743	88	78	127	125	63	68	69	125
5	886	61	92	142	161	77	64	125	164	230	6	23	40	43	20	17	36	45
6	321	12	47	50	48	35	29	57	43	88	2	16	14	13	9	7	15	12
7	119	0	15	19	24	8	8	18	27	29	0	2	6	6	2	2	5	6
8	53	0	11	12	10	4	4	8	4	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay	Circuit	Cluster								Circuit	Cluster							
Level		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	10528	1078	655	926	971	1228	606	825	923
2	0	0	0	0	0	0	0	0	0	2970	464	125	131	179	262	593	107	212
3	0	0	0	0	0	0	0	0	0	251	146	4	6	11	8	4	7	11
4	0	0	0	0	0	0	0	0	0	5	3	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge	Circuit	Cluster								Circuit	Cluster							
Length		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	249	492	460	377	398	435	485	420	10528	265	255	229	405	914	389	409	450
2	0	59	156	118	119	79	83	129	154	2970	88	64	65	94	263	140	74	109
3	0	0	4	7	6	8	8	14	7	251	4	3	6	10	10	0	7	14
4	0	0	0	0	1	0	1	0	0	5	1	0	0	0	0	0	0	1
5	0	0	0	2	2	0	0	2	0	6	6	0	0	0	0	0	0	0
6	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0
7	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (46 2868 262 87 66 33 56 29 12 22 15 14 17 14 12 13 9 6 5 3 2 5 1 5 5 5 5 5 5 4 4 4 1 3 0, 1 1 0 1 0 2 2 1 2 0 0 0 1 1 2 0 0 1 0 0 0 0 0 1 0 0 1 0 2 0 0 0 0 0 1 1 0 0 2 0 1 0 1 0 1 0 0 0 0 0, 0 0 1 0 0 1 1 1 1 2 1 1 1 0 0 0 0 1 0 1 1 0 1 0 0 1 0 1 1 0 0 1 0 0 1 0 1 1 0 0 1 0 1 0 1 1 0 1 0 0, 1 2 0 1 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3)
Cluster 1: (22 390 28 23 17 7 4 6 1 4 4 1 2 4 0 4 1 0 0 0 1 0 0 1 0 2 0 1 0 0 1 2 0 1 0 0 1 0 1 0, 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 1)
Cluster 2: (8 296 33 11 2 3 3 2 3 2 3 2 2 1 3 0 2 0 2 1 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1)
Cluster 3: (4 359 35 14 0 4 9 2 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 1 1 2 2 1 0 1 1 0 1 0 1 0 0 0 0 1, 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1)
Cluster 4: (4 374 25 12 2 1 3 2 1 0 1 0 1 1 1 1 0 0 0 0 0 2 0 0 1 1 3 1 4 2 2 1 0 1 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1)
Cluster 5: (2 434 15 7 19 12 10 2 2 5 4 1 1 2 1 1 0 1 1 0 0 0 0 0 3 1 0 0 0 2 0 0 1 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 1 0 1 0 0 0 1 0 1 1, 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1)
Cluster 6: (2 353 36 8 13 3 14 5 0 5 1 2 2 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3)
Cluster 7: (2 322 37 3 6 1 10 8 5 3 1 3 5 2 2 2 3 1 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 1 0 0 1, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)
Cluster 8: (2 340 53 9 7 2 3 2 0 3 1 5 4 3 4 4 3 3 2 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 1 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	86	61	47	46	48	21	57	0	0	0	0	0	0	0	0
44	0	37	73	35	60	9	64	0	0	0	0	0	0	0	0
22	70	0	99	22	13	53	21	0	0	0	0	0	0	0	0
20	100	150	0	80	43	84	32	0	0	0	0	0	0	0	0
127	207	133	118	0	207	224	171	0	0	0	0	0	0	0	0
65	50	43	61	98	0	97	115	0	0	0	0	0	0	0	0
22	31	68	49	113	86	0	121	0	0	0	0	0	0	0	0
8	108	95	59	92	70	142	0	0	0	0	0	0	0	0	0

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Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1482	181	181	222	175	181	181	180	181
Number of PI	51	20	15	1	0	1	4	0	10
Number of DFF	385	46	52	94	57	31	39	19	47
Number of Combinational Nodes	1431	161	166	221	175	180	177	180	171
Number of PO	122	33	34	6	33	1	4	1	10
Number of Edges	4022	589	564	1286	476	630	603	724	563
Number of Intra-Cluster Edges	2569	204	199	458	138	440	383	443	301
Number of Inter-Cluster Input Edges	2866	231	276	94	277	131	117	173	111
Number of Inter-Cluster Output Edges	2866	154	89	733	61	59	103	106	151
Wirelength Approx	1.06e+06	99460	101677	179009	114739	165693	128162	175081	99937
Scaled Cost	1.63								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.7 ± 14	1.9 ± 8	1.5 ± 1.6	5 ± 35	1.1 ± 0.7	2.7 ± 3.2	2.6 ± 3.5	3.0 ± 5	2.4 ± 3.1
Avg. Comb. Fanout	1.8 ± 9	1.8 ± 10	0.9 ± 0.7	2.8 ± 22	0.7 ± 0.4	2.4 ± 3.4	1.9 ± 3.0	1.8 ± 1.6	1.5 ± 1.5
Avg. PI Fanout	9 ± 54	1 ± 0	1 ± 0	388 ± 0	N/A	1 ± 0	1 ± 0	N/A	1.7 ± 1.5
Avg. DFF Fanout	4 ± 13	2.6 ± 1.5	3.1 ± 2.0	5 ± 26	2 ± 0	4 ± 1.7	5 ± 3.7	13 ± 12	5 ± 5
Avg. Comb. Fanin	3.4 ± 0.7	3.3 ± 0.7	3.3 ± 0.8	3.8 ± 0.4	3.2 ± 0.8	3.5 ± 0.6	3.4 ± 0.6	3.5 ± 0.6	3.3 ± 0.6
Max Fanout	388	113	11	388	2	23	28	51	20

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	436	66	67	95	57	32	43	19	57	1	0	0	1	0	0	0	0	0
1	291	39	46	6	33	11	37	70	49	121	33	34	5	33	1	4	1	10
2	341	39	38	117	52	17	29	16	33	0	0	0	0	0	0	0	0	0
3	158	37	30	4	30	5	20	13	19	0	0	0	0	0	0	0	0	0
4	69	0	0	0	0	4	34	17	14	0	0	0	0	0	0	0	0	0
5	34	0	0	0	1	7	13	9	4	0	0	0	0	0	0	0	0	0
6	23	0	0	0	1	6	2	11	3	0	0	0	0	0	0	0	0	0
7	22	0	0	0	1	8	2	10	1	0	0	0	0	0	0	0	0	0
8	14	0	0	0	0	7	0	7	0	0	0	0	0	0	0	0	0	0
9	16	0	0	0	0	10	0	5	1	0	0	0	0	0	0	0	0	0
10	28	0	0	0	0	25	0	3	0	0	0	0	0	0	0	0	0	0
11	29	0	0	0	0	28	1	0	0	0	0	0	0	0	0	0	0	0
12	18	0	0	0	0	18	0	0	0	0	0	0	0	0	0	0	0	0
13	3	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0

Input Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	879	104	120	14	66	33	128	247	167
2	1284	153	147	467	208	53	94	51	111
3	544	126	114	14	98	17	68	50	57
4	244	0	0	0	0	14	122	63	45
5	129	0	0	0	4	26	49	36	14
6	87	0	0	0	4	22	8	41	12
7	80	0	0	0	4	30	8	34	4
8	52	0	0	0	0	27	0	25	0
9	52	0	0	0	0	34	0	16	2
10	101	0	0	0	0	95	0	6	0
11	114	0	0	0	0	110	4	0	0
12	61	0	0	0	0	61	0	0	0
13	10	0	0	0	0	10	0	0	0

Output Shape

Circuit	Cluster 1	2	3	4	5	6	7	8
2121	141	181	825	114	138	212	252	258
655	29	38	245	0	57	74	132	80
374	147	27	25	29	32	44	37	33
116	0	0	0	0	13	66	21	16
85	0	0	0	0	11	39	22	13
42	0	0	0	0	22	4	13	3
41	0	0	0	0	16	4	16	5
34	0	0	0	0	17	4	13	0
26	0	0	0	0	20	0	6	0
52	0	0	0	0	49	0	3	0
61	0	0	0	0	61	0	0	0
27	0	0	0	0	27	0	0	0
3	0	0	0	0	3	0	0	0
0	0	0	0	0	0	0	0	0

Latched Shape

Delay Level	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0
1	11	0	1	0	0	0	2	5	3
2	166	4	11	92	23	0	16	0	20
3	115	37	30	4	30	0	5	1	8
4	19	0	0	0	0	0	4	6	9
5	18	0	0	0	1	0	11	5	1
6	5	0	0	0	1	0	0	3	1
7	8	0	0	0	1	0	0	6	1
8	3	0	0	0	0	0	0	3	0
9	3	0	0	0	0	0	0	2	1
10	12	0	0	0	0	9	0	3	0
11	7	0	0	0	0	6	1	0	0
12	15	0	0	0	0	15	0	0	0
13	3	0	0	0	0	3	0	0	0

Intra-Cluster Edge Length Distribution

Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	0	1	0	0	0	2	0
2059	139	115	131	83	247	268	262	226
949	41	43	327	52	49	36	66	35
258	24	41	0	1	7	36	36	19
95	0	0	0	1	5	34	20	8
51	0	0	0	1	5	4	24	7
32	0	0	0	0	5	2	14	4
30	0	0	0	0	7	2	13	1
22	0	0	0	0	5	0	5	1
37	0	0	0	0	34	0	3	0
50	0	0	0	0	47	0	0	0
40	0	0	0	0	15	1	0	0
11	0	0	0	0	11	0	0	0
3	0	0	0	0	3	0	0	0

Inter-cluster Input Edge Length Distribution

Edge Length	Circuit	Cluster 1	2	3	4	5	6	7	8
0	0	52	94	57	31	39	19	47	0
1	11	84	113	9	106	25	71	112	68
2	166	73	66	23	105	12	8	2	11
3	115	22	3	5	30	3	3	3	25
4	19	0	0	0	1	3	13	6	4
5	18	0	0	0	2	4	1	2	1
6	5	0	0	0	1	3	0	1	2
7	8	0	0	0	1	6	0	0	0
8	3	0	0	0	0	11	0	0	0
9	3	0	0	0	0	0	0	0	0
10	12	0	0	0	0	2	1	0	0
11	7	0	0	0	0	23	1	0	0
12	15	0	0	0	0	0	0	0	0
13	3	0	0	0	0	0	0	0	0

Inter-cluster Output Edge Length Distribution

Circuit	Cluster 1	2	3	4	5	6	7	8
0	41	42	96	56	33	39	34	44
2059	103	32	314	0	20	41	22	56
949	5	4	259	5	6	1	9	11
258	2	11	19	0	0	12	29	21
95	1	0	18	0	0	0	5	3
51	1	0	2	0	0	0	1	6
32	0	0	0	0	0	0	2	5
30	1	0	0	0	0	0	2	4
22	0	0	8	0	0	2	1	0
37	0	0	0	0	0	0	0	0
50	0	0	2	0	0	0	0	1
40	0	0	15	0	0	8	1	0
11	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0

Fanout Distribution

Circuit: (456 465 330 44 51 29 32 18 21 5 3 3 0 1 3 3 0 1 0 1 4 1 1 2 0 0 1 0 1 0 1 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
1)

Cluster 1: (54 77 42 0 1 0 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 2: (61 62 42 0 4 0 5 5 1 0 0 1)

Cluster 3: (101 25 93 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1)

Cluster 4: (89 29 57)

Cluster 5: (33 64 26 11 14 12 6 4 5 0 2 1 0 0 0 0 0 0 0 0 0 1 1 1)

Cluster 6: (39 71 21 4 16 8 5 4 5 3 1 0 0 0 0 1 0 0 0 0 2 0 0 0 0 0 0 0 1)

Cluster 7: (34 74 19 18 9 4 6 1 5 2 0 1 0 0 0 1 0 1 0 1 0 0 0 1 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0,
0 0 0 0 0 0 0 0 0 0 1)

Cluster 8: (45 63 30 11 7 5 7 1 5 0 0 0 0 1 3 1 0 0 0 0 2)

Inter-Cluster Connectivity Matricies

Comb								Latched							
0	30	8	33	1	16	11	14	40	0	1	0	0	0	0	0
6	0	4	6	0	0	20	11	0	42	0	0	0	0	0	0
144	137	0	169	29	54	38	66	1	0	93	1	0	0	0	1
0	0	5	0	0	0	0	0	0	0	0	56	0	0	0	0
2	4	6	2	0	11	1	0	1	1	0	0	31	0	0	0
15	7	1	7	16	0	17	1	0	0	0	0	0	39	0	0
5	3	4	18	18	5	0	19	4	9	0	0	0	0	19	2
7	1	9	11	28	12	39	0	0	0	0	0	0	0	0	44

ucode_dat

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	1806	230	229	227	208	226	237	236	213
Number of PI	324	33	7	32	7	66	98	32	49
Number of DFF	224	65	60	29	6	2	0	54	8
Number of Combinational Nodes	1482	197	222	195	201	160	139	204	164
Number of PO	258	0	64	30	65	66	0	29	4
Number of Edges	4787	970	742	747	695	629	824	697	720
Number of Intra-Cluster Edges	3485	418	417	436	550	400	465	380	419
Number of Inter-Cluster Input Edges	2539	164	162	181	126	130	101	181	192
Number of Inter-Cluster Output Edges	2539	388	163	130	19	99	258	136	109
Wirelength Approx	1.00e+06	135518	118577	132143	145685	104948	106166	129339	132700
Scaled Cost	1.35								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	2.6 ± 8	3.5 ± 13	2.5 ± 5	2.4 ± 7	2.7 ± 5	2.2 ± 6	3.0 ± 8	2.1 ± 5	2.4 ± 8
Avg. Comb. Fanout	2.0 ± 7	4 ± 18	1.7 ± 5	1.5 ± 2.8	2.3 ± 4	1.5 ± 5	2.0 ± 7	2.0 ± 6	1.1 ± 2.4
Avg. PI Fanout	5 ± 10	2.1 ± 0.5	8 ± 10	7 ± 16	12 ± 9	3.8 ± 8	4 ± 9	1.3 ± 1.2	6 ± 14
Avg. DFF Fanout	3.1 ± 0.6	2.5 ± 0.6	4 ± 0	3 ± 0	3 ± 0	3 ± 0	N/A	3 ± 0	3 ± 0
Avg. Comb. Fanin	3.6 ± 0.7	3.9 ± 0.2	3.3 ± 0.8	3.6 ± 0.7	3.4 ± 0.8	3.3 ± 0.9	3.6 ± 0.7	3.6 ± 0.5	3.9 ± 0.3
Max Fanout	194	194	32	64	32	66	64	32	68

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	548	98	67	61	13	68	98	86	57	33	0	32	0	0	0	0	1	0
1	288	6	35	76	23	15	58	6	69	32	0	32	0	0	0	0	0	0
2	336	32	3	35	32	49	81	61	43	32	0	0	18	0	14	0	0	0
3	290	29	64	14	4	54	0	82	43	46	0	0	2	0	14	0	27	3
4	243	65	60	39	39	38	0	1	1	79	0	0	8	33	36	0	1	1
5	68	0	0	2	64	2	0	0	0	4	0	0	2	0	2	0	0	0
6	32	0	0	0	32	0	0	0	0	31	0	0	0	31	0	0	0	0
7	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	2191	239	293	315	102	259	438	204	341
1	1071	18	106	292	87	50	228	16	274	1394	354	67	156	210	133	184	190	100
2	1216	128	12	104	128	164	284	232	164	494	32	96	52	34	65	101	67	47
3	1130	116	256	56	16	216	0	301	169	278	116	64	12	15	38	0	1	32
4	781	260	176	155	90	92	0	4	4	141	0	0	2	137	2	0	0	0
5	268	0	0	4	256	8	0	0	0	64	0	0	0	64	0	0	0	0
6	93	0	0	0	93	0	0	0	0	1	0	0	0	1	0	0	0	0
7	4	0	0	0	4	0	0	0	0	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	2574	133	262	303	338	132	371	188	236
2	0	0	0	0	0	0	0	0	0	1034	65	39	44	51	184	94	135	141
3	64	0	0	0	0	2	0	54	8	655	155	88	58	5	69	0	56	41
4	160	65	60	29	6	0	0	0	0	274	65	28	31	136	9	0	1	1
5	0	0	0	0	0	0	0	0	0	22	0	0	0	16	6	0	0	0
6	0	0	0	0	0	0	0	0	0	4	0	0	0	4	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	60	29	6	2	0	54	8	0	0	65	60	29	6	2	0	54	8
1	0	72	37	124	48	82	19	87	142	2574	128	7	69	10	44	204	70	79
2	0	28	0	14	63	16	28	84	48	1034	96	62	29	0	45	20	10	19
3	64	4	96	36	13	30	0	2	2	655	99	34	3	3	8	32	2	2
4	160	0	0	1	0	2	0	0	0	274	0	0	0	0	0	2	0	1
5	0	0	0	0	0	0	0	0	0	22	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (385 784 170 234 120 16 33 2 9 1 1 0 1 0 2 1 6 0 1 0 4 0 1 1 0 0 0 0 0 0 1 0 20 0 0 0 1 0, 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 6 0 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 1)
Cluster 1: (65 32 62 29 36 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 5 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 1)
Cluster 2: (92 64 2 4 60 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6)
Cluster 3: (41 121 21 30 4 0 0 0 1 0 1 0 0 0 0 1 2 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 4: (39 102 5 10 19 14 1 1 7 0 0 0 0 0 0 0 4 0 1 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 5: (54 118 18 7 1 1 20 0 0 1 0 0 1 0 2 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1)
Cluster 6: (0 118 20 87 0 0 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 4)
Cluster 7: (82 86 6 54 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 5)
Cluster 8: (12 143 36 13 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 1 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	95	90	42	2	1	54	39	65	0	0	0	0	0	0	0
36	0	1	0	32	0	2	32	0	60	0	0	0	0	0	0
0	0	0	36	65	0	0	0	0	0	29	0	0	0	0	0
3	6	2	0	2	0	0	0	0	0	0	6	0	0	0	0
3	2	10	0	0	37	24	21	0	0	0	0	2	0	0	0
56	30	38	6	22	0	60	46	0	0	0	0	0	0	0	0
0	0	26	0	2	0	0	54	0	0	0	0	0	0	54	0
6	0	8	40	5	9	33	0	0	0	0	0	0	0	0	8

ucode_reg

Basic Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Number of Nodes	230	25	27	27	30	30	34	27	30
Number of PI	78	9	9	9	10	10	12	9	10
Number of DFF	74	8	9	9	9	10	10	9	10
Number of Combinational Nodes	152	16	18	18	20	20	22	18	20
Number of PO	74	8	9	9	9	10	10	9	10
Number of Edges	378	50	54	54	59	60	191	55	50
Number of Intra-Cluster Edges	175	16	18	18	22	20	43	18	20
Number of Inter-Cluster Input Edges	398	25	27	27	28	30	10	28	20
Number of Inter-Cluster Output Edges	398	9	9	9	9	10	138	9	10
Wirelength Approx	18573	1977	2234	2234	2437	2442	2573	2234	2442
Scaled Cost	1.20								

Fanout Statistics	Circuit	Cluster							
		1	2	3	4	5	6	7	8
Avg. Fanout	1.6 ± 7	1 ± 0	1 ± 0	1 ± 0	1.0 ± 0.4	1 ± 0	5 ± 17	1 ± 0	1 ± 0
Avg. Comb. Fanout	2.8 ± 12	1 ± 0	1 ± 0	1 ± 0	0.8 ± 0.3	1 ± 0	13 ± 27	1 ± 0	1 ± 0
Avg. PI Fanout	1.0 ± 0.1	1 ± 0	1 ± 0	1 ± 0	1.1 ± 0.3	1 ± 0	1.0 ± 0.2	1 ± 0	1 ± 0
Avg. DFF Fanout	1.0 ± 0.1	1 ± 0	1 ± 0	1 ± 0	1.2 ± 0.4	1 ± 0	1 ± 0	1 ± 0	1 ± 0
Avg. Comb. Fanin	3.8 ± 0.4	4 ± 0	4 ± 0	4 ± 0	3.6 ± 0.7	4 ± 0	3.6 ± 0.7	4 ± 0	4 ± 0
Max Fanout	74	1	1	1	2	1	74	1	1

Node Shape										PO Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	152	17	18	18	19	20	22	18	20	72	8	9	9	7	10	10	9	10
1	4	0	0	0	2	0	2	0	0	2	0	0	0	2	0	0	0	0
2	74	8	9	9	9	10	10	9	10	0	0	0	0	0	0	0	0	0

Input Shape										Output Shape								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	156	17	18	18	22	20	23	18	20
1	8	0	0	0	4	0	4	0	0	148	0	0	0	0	0	148	0	0
2	296	32	36	36	36	40	40	36	40	0	0	0	0	0	0	0	0	0

Latched Shape										Intra-Cluster Edge Length Distribution								
Delay Level	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	156	0	0	0	4	0	24	0	0
2	74	8	9	9	9	10	10	9	10	148	16	18	18	18	20	19	18	20

Inter-cluster Input Edge Length Distribution										Inter-cluster Output Edge Length Distribution								
Edge Length	Circuit	Cluster								Circuit	Cluster							
		1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8
0	0	9	9	9	10	10	9	10	0	0	8	9	9	9	10	10	9	10
1	0	16	18	18	18	20	0	18	20	156	0	0	0	0	0	128	0	0
2	74	0	0	0	0	0	1	0	0	148	1	0	0	0	0	0	0	0

Fanout Distribution
Circuit: (76 148 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 1: (8 17)
Cluster 2: (9 18)
Cluster 3: (9 18)
Cluster 4: (11 16 3)
Cluster 5: (10 20)
Cluster 6: (10 21 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2)
Cluster 7: (9 18)
Cluster 8: (10 20)

Inter-Cluster Connectivity Matricies															
Comb								Latched							
0	0	0	0	0	1	0	0	8	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	9	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	9	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	9	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	10	0	0	0
16	18	18	18	20	0	18	20	0	0	0	0	0	10	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	9	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10

B Results for Original Circuits and Mike Hutton's Clones

Table B.1: Original Circuit Results and Mike Hutton's Clone Results

Circuit	Test Set	Type	Size	bb cost		Total Wirelength		Min. Number of Tracks		Critial Path Delay	
				Orig	MH	Orig	MH	Orig	MH	Orig	MH
alu4	1	Comb	1536	209	179	23852	19006	14	11	8.40E-08	6.81E-08
apex2	1	Comb	1916	297	275	33868	31648	16	15	8.70E-08	8.54E-08
apex4	1	Comb	1270	201	170	23059	19320	17	13	7.90E-08	7.25E-08
des	1	Comb	1847	277	398	31344	46591	10	17	1.00E-07	9.75E-08
ex5p	1	Comb	1072	188	160	20777	18369	17	15	7.10E-08	6.85E-08
ex1010	1	Comb	4608	693	817	76083	91522	15	18	1.60E-07	1.34E-07
misex3	1	Comb	1411	221	184	24100	20943	15	13	8.60E-08	6.92E-08
pdc	1	Comb	4591	974	862	110830	96675	23	18	2.20E-07	1.25E-07
seq	1	Comb	1791	282	239	33246	27177	17	14	9.20E-08	7.71E-08
spla	1	Comb	3706	665	672	77666	76898	22	19	1.30E-07	1.12E-07
bigkey	1	Seq	2159	256	288	26476	31002	9	16	5.70E-08	5.32E-08
diffeq	1	Seq	1934	177	267	18913	30144	12	17	7.90E-08	7.45E-08
dsip	1	Seq	1822	235	190	23317	18812	9	11	7.90E-08	5.12E-08
elliptic	1	Seq	4854	580	844	58017	96444	16	23	1.10E-07	9.68E-08
frisc	1	Seq	4444	641	987	69611	112758	20	31	1.40E-07	1.55E-07
s298	1	Seq	1941	244	274	25423	27511	11	15	1.40E-07	1.22E-07
tseng	1	Seq	1482	108	201	11520	23548	11	18	5.50E-08	7.45E-08
display chip	1	Seq	2417	204	372	19158	41420	10	19	7.60E-08	8.57E-08
img interp	1	Seq	3424	319	519	32545	57166	12	19	9.30E-08	1.21E-07
input chip	1	Seq	1106	74	122	7526	13803	8	15	5.60E-08	6.50E-08
peak chip	1	Seq	1146	71	98	6759	10792	9	11	8.00E-08	8.15E-08
scale125 chip	1	Seq	3856	292	638	26834	71125	10	25	8.80E-08	1.10E-07
scale2 chip	1	Seq	1524	117	198	11125	22118	9	17	6.80E-08	7.83E-08
prils dp	2	Comb	501	46	51	4874	5473	14	11	8.40E-08	1.09E-07
rsadd dp	2	Comb	521	43	53	4546	5731	16	9	8.70E-08	1.68E-07
code seq dp	2	Seq	588	47	35	5110	3635	17	9	7.90E-08	7.28E-08
dcu dpath	2	Seq	1590	222	332	23193	37609	10	14	1.00E-07	7.76E-08
ex dpath	2	Seq	3925	1238	1613	133554	184977	17	27	7.10E-08	3.20E-07
exponent dp	2	Seq	644	66	75	7543	8782	15	15	1.60E-07	9.69E-08
icu dpath	2	Seq	3813	592	999	69064	114071	15	32	8.60E-08	1.83E-07
incmod	2	Seq	1007	104		11319		23		2.20E-07	
imdr dpath	2	Seq	1410	201		22384		17		9.20E-08	
mantissa dp	2	Seq	1284	278		32050		22		1.30E-07	
multmod dp	2	Seq	1893	205	345	22532	40001	9	23	5.70E-08	1.46E-07
pipe dpath	2	Seq	798	67	67	7351	7632	12	13	7.90E-08	5.65E-08
smu dpath	2	Seq	866	93		10023		9		7.90E-08	
ucode dat	2	Seq	1806	377		43554		16		1.10E-07	
ucode reg	2	Seq	230	7	14	799	1485	20	7	1.40E-07	1.61E-08
s38417	2	Seq	7465	729	1947	71038	213739	11	33	8.63E-08	1.06E-07
s38584.1	2	Seq	21553	753		69751		11		8.75E-08	

C Bounding Box Measurements

Table C.1 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	147	237	131	286	114	1196	148	1120	209	773	298	198
2	155	238	137	294	118	998	148	1124	210	770	334	199
3	159	248	133	296	124	1038	147	1102	215	771	327	201
4	163	246	132	310	123	996	155	1125	217	761	311	213
5	162	248	136	312	121	935	154	1089	222	754	300	222
6	166	249	142	321	126	950	154	1078	228	758	291	198
7	178	251	145	309	129	864	156	1073	222	789	275	203
8	170	256	143	302	130	844	166	1089	225	749	287	202
9	169	260	140	317	132	941	166	1087	234	748	278	197
10	170	255	148	339	137	936	169	1117	225	752	276	204
11	182	276	149	312	137	910	166	1096	231	755	271	211
12	180	260	149	327	137	912	168	1101	244	756	282	205
13	181	267	156	326	139	906	178	1119	242	759	268	211
14	182	266	154	335	143	947	172	1143	243	783	279	210
15	182	271	160	311	153	922	177	1109	243	777	275	215
16	183	275	158	318	152	938	176	1121	255	790	270	192

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	260	786	886	203	131	255	479	87	76	444	135
2	295	737	769	209	135	260	421	86	83	379	136
3	317	725	748	225	130	228	415	85	79	389	138
4	274	721	766	233	135	232	394	82	76	381	138
5	272	696	743	243	131	224	385	80	76	362	125
6	263	705	761	248	133	209	404	82	81	375	127
7	269	729	742	249	132	225	380	84	76	376	131
8	263	726	739	250	132	202	398	81	73	360	130
9	253	669	762	249	131	225	366	81	76	363	131
10	265	696	741	249	132	213	385	87	76	354	133
11	253	687	788	246	135	214	384	81	72	365	128
12	269	689	839	251	143	210	397	82	75	393	137
13	252	701	786	246	133	232	400	82	81	351	128
14	262	732	745	249	128	208	368	85	77	386	134
15	254	710	768	256	134	232	355	82	74	366	133
16	256	754	784	253	143	227	376	79	79	362	132

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	70	286	1449	57	768	116	180
2	62	239	1513	59	735	114	205
3	62	229	1536	60	666	97	188
4	66	237	1331	64	697	105	195
6	58	233	1383	67	619	107	194
8	57	230	1319	65	657	104	207
11	49	240	1345	65	662	108	221
12	54	217	1274	73	605	106	205
13	56	227	1268	68	633	112	211
14	49	234	1311	73	639	116	221
16	48	221	1378	71	700	121	213

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	206	250	90	104	289	20	2251	1909
2	227	218	61	108	317	13	1809	1655
3	249	230	76	114	317	10	1728	1631
4	234	225	63	108	338	9	1687	1426
6	238	257	64	113	326	10	1494	1302
8	256	224	69	100	356	10	1367	1263
11	255	223	71	103	376	10	1351	1139
12	267	242	70	106	352	9	1281	1142
13	259	240	65	106	339	9	1283	1161
14	267	241	73	102	354	7	1283	1138
16	275	242	71	108	371	7	1191	1106

Table C.2 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	177	258	172	320	148	1201	195	1105	243	802	350	245
2	190	282	167	345	153	963	195	1120	273	790	391	247
3	194	300	177	363	152	1031	201	1090	271	787	366	250
4	199	327	176	338	154	1019	213	1099	277	756	331	247
5	200	320	184	358	160	943	208	1078	283	749	344	255
6	197	327	184	355	162	960	211	1072	281	761	312	242
7	202	316	189	335	167	880	208	1087	284	765	304	234
8	199	317	192	347	163	850	210	1094	287	786	307	242
9	205	329	191	345	169	899	210	1092	288	797	308	232
10	207	315	196	349	175	923	216	1118	287	791	306	238
11	207	333	194	346	174	943	219	1114	289	809	299	235
12	211	343	195	350	173	933	220	1109	302	813	297	229
13	210	337	202	343	174	938	220	1120	293	815	288	238
14	204	347	197	352	175	951	219	1165	294	827	299	232
16	211	329	199	330	175	925	228	1153	322	868	293	228

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	295	839	852	238	178	333	558	110	104	505	181
2	315	734	833	246	164	295	469	103	99	474	166
3	318	760	817	251	152	268	445	106	90	425	152
4	287	743	810	245	172	258	483	92	84	425	152
5	276	773	861	244	164	257	431	90	91	434	153
6	290	764	832	251	169	246	450	87	89	401	137
7	284	777	823	253	164	249	425	91	85	410	143
8	281	777	806	249	161	241	437	88	86	390	143
9	268	781	821	250	153	244	381	88	88	388	143
10	279	767	829	259	152	240	395	86	87	381	140
11	266	797	825	252	155	244	414	87	81	389	137
12	272	773	793	256	156	250	418	87	79	432	142
13	254	788	828	256	152	244	417	83	81	409	131
14	269	830	810	255	149	246	398	83	78	373	138
16	276	818	828	253	149	234	375	83	81	375	135

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	75	348	1454	81	771	137	236
2	61	288	1607	76	752	124	232
3	66	265	1559	80	702	130	240
4	63	268	1518	77	769	126	233
6	53	283	1464	82	701	127	239
8	60	277	1404	75	749	121	238
11	52	251	1401	78	740	122	229
12	54	249	1326	76	722	122	231
13	47	215	1390	74	719	126	226
14	48	253	1327	75	716	123	235
16	49	237	1337	75	731	121	223

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	281	326	106	142	393	20	2226	1867
2	261	277	84	140	391	19	1781	1652
3	282	276	96	130	399	13	1790	1551
4	271	282	81	124	405	20	1654	1441
6	273	293	80	117	395	10	1454	1315
8	285	284	75	110	408	10	1375	1240
11	282	293	80	108	416	8	1314	1162
12	287	307	81	112	401	12	1270	1215
13	281	304	77	107	394	12	1249	1128
14	283	302	78	101	403	9	1277	1117
16	289	304	80	113	398	11	1277	1126

Table C.3 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Wirelength from Characterization

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	241	381	239	381	185	1355	243	1332	320	947	349	293
2	233	368	231	353	187	1185	247	1326	321	978	380	241
3	235	393	230	359	181	1183	245	1252	337	932	347	253
4	233	400	228	361	193	1173	254	1341	325	980	330	252
5	231	393	227	363	204	1137	254	1301	342	982	327	256
6	240	383	224	372	198	1150	244	1303	342	979	306	241
7	229	382	222	343	197	1042	250	1324	334	968	304	236
8	235	393	222	345	204	1047	254	1282	338	985	298	245
9	228	389	229	351	196	1030	254	1277	337	954	317	244
10	230	385	222	357	202	1145	247	1278	333	935	296	240
11	232	387	224	354	195	1055	251	1274	339	940	294	240
12	235	384	224	350	202	1039	250	1276	340	953	305	235
13	228	385	229	340	207	1053	254	1313	338	938	292	241
14	230	375	227	344	208	1028	255	1280	327	932	290	231
15	227	374	228	345	206	1025	251	1290	332	944	301	230

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	285	804	956	243	179	312	532	112	82	517	169
2	313	794	847	248	164	291	455	100	96	411	161
3	323	777	911	251	160	268	423	98	92	399	168
4	260	820	904	246	156	253	458	91	86	387	146
5	273	793	870	253	148	242	456	91	84	407	143
6	263	791	906	252	166	242	442	91	89	409	142
7	271	797	878	251	160	237	415	88	82	397	144
8	276	811	842	249	154	250	433	83	83	376	138
9	253	807	849	254	147	250	391	84	87	372	140
10	279	810	861	256	154	252	396	90	83	374	140
11	266	804	852	252	148	238	409	89	84	391	142
12	273	789	858	257	153	238	440	86	81	406	140
13	259	813	832	253	150	256	406	87	83	374	131
14	269	784	811	252	150	235	388	85	79	381	137
15	254	799	848	251	150	249	381	89	83	378	139
16			824	252	144	232	392	88	77		139

Table C.4 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	149	238	132	273	119	1185	147	1128	210	806	300	194
2	148	241	132	287	119	1002	147	1058	209	752	274	202
3	150	238	132	278	119	978	149	1055	215	759	285	215
4	150	242	132	294	123	943	148	1075	213	734	276	205
5	154	232	137	319	119	933	150	1045	222	730	284	213
6	151	246	135	311	121	921	146	1051	230	751	274	211
7	155	239	136	318	126	932	153	1059	233	740	275	198
8	154	244	139	336	126	849	153	1060	241	748	277	213
9	153	255	145	314	131	924	157	1050	221	737	269	214
10	155	241	142	331	127	887	155	1057	229	736	269	225
11	157	251	141	311	131	883	157	1060	241	734	269	193
12	157	248	143	312	134	849	159	1063	223	745	273	205
13	158	252	154	309	137	859	162	1074	230	774	264	223
14	158	252	146	333	130	850	164	1077	245	746	266	210
15	160	253	145	332	139	858	173	1081	240	743	266	206
16	163	255	151	318	139	863	170	1085	236	747	261	207

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	246	797	887	207	127	249	462	87	83	477	142
2	266	695	774	218	137	238	428	95	83	431	147
3	276	736	801	224	132	238	409	81	81	405	136
4	260	731	743	227	130	229	400	77	82	376	131
5	271	715	806	216	131	215	418	85	80	422	127
6	275	691	771	215	135	222	409	87	83	403	129
7	262	727	732	239	137	228	383	77	76	384	127
8	267	697	734	237	139	227	372	80	75	365	133
9	255	763	748	236	132	223	388	85	77	384	139
10	263	751	744	235	139	217	388	82	83	364	137
11	254	737	744	234	142	220	388	78	78	381	133
12	257	698	721	235	140	212	370	79	82	359	129
13	248	689	740	245	137	222	347	79	77	344	132
14	243	730	757	238	133	231	383	80	79	364	129
15	254	758	748	244	132	223	371	80	75	374	137
16	246	718	824	255	140	219	370	78	72	346	133

Table C.5 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	170	277	168	341	147	1172	180	1118	247	797	340	257
2	184	287	175	350	150	1008	199	1118	262	740	327	243
3	184	286	176	359	151	955	197	1057	266	764	328	240
4	192	288	170	365	160	926	194	1048	266	747	322	260
5	202	295	172	348	161	932	196	1051	285	737	322	259
6	195	289	179	362	157	873	207	1044	285	758	310	264
7	194	292	179	356	157	891	203	1059	280	736	312	242
8	202	322	179	356	164	864	209	1055	287	745	306	246
9	203	312	185	351	164	909	221	1077	286	747	315	245
10	198	296	183	361	167	866	207	1045	293	767	307	243
11	205	312	187	350	164	890	220	1071	295	760	314	236
12	205	318	187	335	166	864	210	1069	288	783	306	243
13	207	305	184	351	169	856	218	1092	291	765	297	241
14	210	320	187	351	174	851	220	1074	296	796	302	232
15	208	312	191	346	171	886	227	1060	292	791	302	234
16	213	320	189	329	170	856	225	1066	293	777	292	230

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	279	826	853	238	165	340	559	111	106	514	172
2	294	733	780	246	165	274	504	106	97	448	165
3	304	774	812	248	164	284	470	98	95	474	165
4	309	766	800	243	163	260	485	96	91	439	155
5	318	774	792	246	160	266	450	104	91	422	156
6	295	764	815	248	160	244	453	92	91	430	151
7	277	834	818	249	158	277	454	87	85	400	143
8	303	735	793	252	163	249	412	86	91	408	141
9	277	789	814	244	153	260	416	94	94	391	142
10	273	788	839	249	150	248	395	89	89	375	135
11	259	776	786	243	157	250	402	85	80	368	140
12	279	767	802	252	156	241	396	86	85	417	139
13	267	772	793	253	159	239	385	87	82	368	137
14	265	796	817	250	154	242	400	85	82	364	136
15	274	833	834	245	164	247	408	84	84	387	147
16	271	824	800	253	148	244	386	86	83	375	138

Table C.6 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Wirelength from Characterization

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	235	382	235	386	189	1452	244	1219	325	944	354	263
2	224	380	225	380	179	1248	248	1275	319	936	319	252
3	231	369	213	393	185	1196	248	1276	317	969	316	284
4	229	376	233	371	191	1210	244	1322	311	961	313	256
5	233	369	227	361	179	1167	238	1311	323	929	319	268
6	230	380	221	360	195	1104	244	1252	338	972	309	267
7	218	361	229	353	183	1096	253	1245	335	933	305	256
8	220	389	227	363	198	1060	241	1248	331	961	301	249
9	229	379	221	359	191	1083	249	1281	331	933	301	250
10	223	365	219	368	196	1015	249	1276	335	967	300	243
11	222	384	220	341	194	1043	247	1297	339	948	294	249
12	223	381	221	347	200	1022	240	1267	335	951	297	242
13	224	218	218	354	196	974	241	1318	337	917	251	239
14	231	368	225	353	201	979	245	1303	335	965	298	236
15	222	372	222		195	971	242	1283	335	947	249	243
16	231	380	223	330	197	970	248	1311	339	928	295	240

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	274	858	944	239	179	315	532	112	85	498	178
2	285	791	864	243	174	286	477	94	92	428	133
3	281	815	885	249	159	268	468	95	89	417	149
4	297	800	879	245	161	244	494	102	92	407	145
5	281	807	891	245	162	264	449	96	94	416	151
6	296	758	872	252	153	254	399	85	87	397	159
7	277	789	862	250	153	251	446	88	87	386	133
8	276	794	826	248	157	254	432	92	89	398	134
9	265	815	846	247	158	248	383	90	91	360	143
10	268	833	816	248	154	249	397	85	89	363	141
11	265	829	861	245	157	250	416	91	83	389	137
12	268	772	772	253	158	246	394	85	83	398	136
13	252	792	855	251	150	247	388	90	88	388	136
14	254	789	848	252	152	138	397	81	85	370	143
15	265			249	163		385	86	80	390	137
16	246										0

Table C.7 - Partitioning Condition: t3 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	150	238	131	269	118	1179	149	1119	211	800	306	200
2	153	240	133	300	122	1124	144	1104	209	791	326	191
3	158	247	130	307	123	947	145	1134	216	773	309	215
4	161	245	134	294	124	911	156	1097	216	784	288	202
5	160	246	133	301	125	964	157	1126	220	752	288	205
6	173	248	134	306	127	942	153	1082	227	767	328	211
7	171	253	143	323	127	896	164	1071	246	745	278	203
8	178	257	144	316	134	958	163	1092	229	738	272	208
9	170	261	150	328	135	888	160	1137	226	773	283	204
10	169	261	153	324	133	915	167	1080	236	752	285	215
11	182	261	146	321	131	888	170	1104	234	753	285	220
12	176	262	149	313	136	897	176	1081	230	750	281	205
13	181	262	153	329	140	902	175	1095	233	768	272	207
14	182	261	158	315	141	898	175	1096	250	751	267	214
15	184	265	156	314	142	871	177	1105	245	784	265	207
16	183	269	161	329	145	1134	796	277	775	794	260	219

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	273	815	856	218	126	251	466	81	82	469	138
2	290	735	748	225	128	227	431	89	92	421	133
3	295	702	776	228	134	236	442	87	78	409	134
4	282	716	743	229	130	228	405	84	71	372	124
5	271	731	717	250	123	213	399	83	81	394	139
6	264	668	724	241	140	216	400	80	79	383	131
7	276	743	783	244	127	230	390	83	80	371	123
8	266	711	735	252	134	211	384	76	75	392	132
9	250	698	746	246	136	223	380	85	81	354	134
10	267	711	725	247	140	222	382	78	81	360	132
11	262	716	811	256	134	221	388	83	78	379	130
12	254	742	763	252	139	231	382	77	77	372	129
13	253	736	792	250	140	213	380	83	73	353	129
14	261	739	749	252	130	217	378	82	75	395	125
15	260	700	800	248	129	226	388	79	77	377	132
16	257	723	736	258	135	221	378	78	76	365	128

Table C.8 - Partitioning Condition: t3 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	178	269	169	335	155	1190	175	1111	240	798	352	250
2	187	268	174	343	148	1060	205	1115	248	777	409	236
3	195	314	172	371	155	966	203	1097	269	783	361	245
4	205	309	170	349	163	902	213	1134	274	785	330	257
5	210	324	176	352	155	949	211	1065	283	787	331	248
6	205	306	187	347	165	940	209	1093	281	773	351	243
7	211	309	191	340	161	874	214	1072	285	787	317	240
8	209	332	188	350	168	974	209	1061	288	789	298	246
9	204	332	191	356	170	911	213	1105	283	827	315	241
10	206	318	200	362	172	943	218	1151	300	803	316	234
11	208	342	199	365	173	940	219	1151	297	803	301	241
12	212	332	195	347	176	928	218	1126	300	821	306	232
13	210	325	203	343	173	920	220	1129	296	834	304	225
14	206	323	203	350	175	929	223	1138	308	849	293	237
15	210	325	206	336	178	945	225	1139	298	850	292	233
16	208	341	202	346	179	990	223	1136	295	877	299	234

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	289	794	897	237	175	324	547	109	100	528	173
2	323	769	803	240	159	275	487	102	97	499	173
3	340	757	804	245	150	276	440	101	94	440	151
4	298	785	808	244	162	256	481	91	85	418	144
5	306	777	760	256	157	255	415	93	89	425	156
6	279	796	806	247	161	255	458	90	91	401	144
7	298	780	844	250	159	257	429	90	87	406	140
8	281	732	804	251	158	242	413	85	82	405	144
9	270	766	812	259	159	243	396	90	86	401	142
10	278	771	845	259	149	235	411	84	83	381	144
11	275	781	828	252	156	243	421	88	85	395	136
12	267	756	860	253	154	237	389	84	78	380	138
13	268	783	816	256	157	246	441	88	82	374	130
14	270	854	825	250	148	238	395	81	81	386	139
15	258	793	824	255	149	241	416	86	80	363	136
16	268	831	835	253	152	243	387	87	81	372	131

D Wirelength Measurements

Table D.1 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	15187	26861	14538	33016	12832	129267	15942	127749	23438	90125	32591	21872
2	15929	26385	14648	33228	13137	108868	16160	126578	23325	86964	36780	21267
3	16580	27932	14509	33105	13450	111795	15978	125453	23779	86673	35550	21723
4	16708	27013	14267	33925	13475	105805	17202	128584	23799	87320	33256	22775
5	16753	28353	14666	34674	13232	97785	16758	125582	24447	84910	31180	23710
6	16990	27408	15168	35147	14270	100634	17199	124353	24749	84999	30523	20804
7	18858	28316	15483	34297	14300	91621	16920	122270	24632	87828	28959	21376
8	17874	28682	15951	33297	14593	87388	18297	126085	24759	82670	30035	21469
9	17349	29480	15296	35267	14822	99218	17913	125913	26180	82827	28634	20660
10	17506	28315	16497	36978	15457	95574	18686	128181	24613	84762	28631	21306
11	19366	30466	16393	34395	15671	95077	18099	129107	25606	86469	28344	22432
12	18897	29386	16185	36738	15542	94460	18456	123810	26489	84614	28903	21668
13	18847	30147	17138	35720	15814	94292	19684	130607	26229	86659	27706	22024
14	19193	30022	17180	36345	16148	100087	18922	131697	27074	87973	28282	22259
15	19476	30211	17427	34662	17624	96667	19513	127932	27018	87481	28069	22788
16	19209	31020	17540	34787	17640	97812	19618	132025	27963	90794	28108	20088

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	25971	87556	101380	18904	14225	26487	50116	8875	7433	45148	13824
2	30516	81028	86602	19838	14664	26902	42375	8614	8083	36396	13825
3	32168	78756	83533	20784	13974	23078	41298	8561	7755	37350	14172
4	27378	78473	84600	23300	14476	23500	39825	8201	7304	36870	13875
5	27206	73793	83466	23754	14036	22574	38348	7933	7352	34427	12599
6	26418	76131	85758	24361	14067	20850	39784	8167	7821	36481	12962
7	27298	79119	82259	24730	13884	22674	38060	8420	7419	35834	13290
8	26420	77767	81510	25514	13845	20061	39584	8304	6978	33936	13337
9	25372	71256	84950	24736	13516	22221	35538	7886	7439	34337	13317
10	26689	74490	82106	24902	14076	21258	38136	8782	7361	33645	13569
11	25309	72948	86803	25405	14018	21113	37725	8148	6688	34980	12948
12	27612	73886	92077	26032	15307	20977	39639	8274	7086	38034	13969
13	25122	74795	87310	24875	13812	23040	39484	8156	7854	32825	13187
14	26496	78918	81389	25079	13729	20425	36246	8638	7548	36753	13596
15	25264	76399	86267	25841	14036	23753	34854	8358	7139	34561	13524
16	25596	80860	87306	25950	15246	22388	36400	7814	7767	33822	13533

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	7495	32277	154070	6135	90667	12625	20101
2	6568	26173	173838	6440	86385	12458	22662
3	6783	24245	168422	6593	76704	10343	20974
4	6870	24963	146375	7183	78810	11502	21723
6	6304	23958	149216	7479	70035	11780	21259
8	6082	24511	142369	7023	75224	11449	22987
11	5399	24396	145468	7291	73770	11981	24414
12	6045	21926	135761	8370	67440	11676	23162
13	6130	23664	135608	7495	72391	12213	23601
14	5517	23459	137993	8210	71611	12660	24420
16	5060	22359	147897	7808	79182	13618	24195

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	22860	27697	10321	11058	32604	2092	245818	217115
2	25306	23138	6612	11462	35575	1474	202524	186520
3	27358	25269	8285	12370	33625	1178	188688	178927
4	26123	23933	6689	11834	38420	1174	180738	153275
6	26715	28162	6859	12253	36276	1220	157380	137475
8	28929	23467	7384	11016	39771	1183	142339	132489
11	28161	23812	7623	10936	42560	1246	141004	117459
12	29974	26155	7519	11133	40145	1141	132127	117814
13	28905	26023	6838	11219	38638	1191	133256	118171
14	30058	26167	7943	10915	40093	857	132263	116622
16	30796	26206	7772	11597	41549	937	122812	111093

Table D.2 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	19181	29570	19397	36548	16822	128268	21290	124334	27944	89667	39242	27504
2	20315	31273	18626	38932	17390	105919	21466	125953	30533	89175	43957	27098
3	21085	34711	19562	42199	17502	110005	22203	122357	30706	89460	39802	27153
4	21778	36988	19155	37038	17429	106762	23948	125283	31136	84439	35906	27115
5	21760	36334	21029	38981	17754	99528	23458	123839	31712	84370	37201	27869
6	21477	37253	20706	39262	18386	101198	23529	124183	31717	86803	33453	26586
7	22352	36071	21080	36361	18554	91327	23657	122944	31755	87581	32793	25033
8	21730	35724	21334	38425	18373	88761	23657	125495	32972	89570	33432	26363
9	22047	39110	21152	38697	19392	93782	24329	125450	32278	91035	32209	25471
10	22712	36495	21914	39387	20448	96437	24501	126662	33113	89740	32851	25573
11	23081	38326	21725	39272	19952	99688	25009	129403	32708	93807	31690	25537
12	23206	39305	22193	39114	20707	96487	25492	130090	34531	92916	31527	24752
13	23240	39694	23095	37701	20255	98145	25525	129837	33202	93382	29828	25896
14	21788	39808	21953	38903	20044	99198	25125	133854	33287	96913	31852	25266
16	22721	38032	22045	36405	19662	98361	26266	131149	37172	101669	30576	24454

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	30010	93102	96891	24181	19688	35886	58803	12018	10755	52318	19861
2	34216	81071	95102	24292	18137	31854	48860	11136	10083	47038	17871
3	32793	84019	93133	26516	16784	27819	45872	11272	9306	42550	16222
4	29491	82163	91391	24712	18762	26047	49725	9523	8335	41812	15787
5	28030	83056	96711	25502	17858	26180	43655	9373	9122	43234	15864
6	30033	83464	94731	25524	18373	24844	45687	9042	8794	38866	14255
7	28938	83965	93327	26350	17874	25607	43265	9357	8229	40469	14931
8	28816	85418	90976	24473	17371	25134	45307	9047	8601	37540	14806
9	26765	84545	92686	25777	16532	25114	38192	9298	8712	37887	14825
10	28356	82056	93345	26494	16401	24096	39832	8975	8544	37005	14260
11	26035	86112	92926	24915	16573	24987	41823	8872	8137	38354	14047
12	28039	83793	87077	26023	16819	25644	41791	9222	7651	42771	14848
13	25697	85497	92804	25902	16344	25216	42114	8578	8003	40078	13558
14	27408	89719	88857	26052	15959	24998	39689	8377	7788	35429	14447
16	27948	89165	92120	26185	15995	23327	37014	8264	8038	35599	13872

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	8223	41107	154061	9016	91784	16030	26694
2	6678	32714	181296	8459	88753	13724	26755
3	7131	28239	172792	9112	81027	14407	27543
4	6629	28847	166658	8576	88196	14064	26437
6	5904	30013	163123	9350	80041	14294	27247
8	6712	29329	152758	8503	86796	13709	27146
11	5654	26949	150891	8908	84477	13418	25342
12	6083	26562	140061	8474	81413	13638	26356
13	5344	22328	145939	8317	81626	14156	25284
14	5343	26945	142941	8592	79273	13423	26256
16	5403	24585	142834	8483	82157	13587	25363

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	32495	36704	12127	15971	44944	2031	246964	213269
2	29650	31740	9258	15284	44463	1998	197492	188063
3	31811	30447	10600	14586	44797	1467	196086	165640
4	30567	31330	9233	13284	47389	2075	179512	154701
6	31316	32251	8651	12963	45099	1254	153856	140356
8	32589	31661	8393	11703	46771	1115	143752	130315
11	31610	32337	8847	11899	46739	1044	135848	118684
12	32303	33973	8749	12242	44960	1297	131927	125202
13	32416	34062	8444	11659	45633	1439	128427	114936
14	32176	34295	8401	11037	46030	1162	132388	113567
16	32935	33497	8914	12372	45438	1281	131715	115446

Table D.3 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	15621	27345	14327	31112	13004	129133	16073	129884	23319	89048	33550	21532
2	15364	26851	14361	31634	12951	110068	16047	120675	23136	83467	29452	21367
3	15461	26590	14644	30278	13224	105935	15920	120529	23410	82624	31130	23143
4	15164	27076	14368	31028	13581	101132	16097	122496	23460	82379	29543	21641
5	15753	26233	14711	33352	13084	99485	16401	116715	23886	81011	30666	22691
6	15389	27980	14690	33381	13317	97665	15835	118262	25420	84451	28872	22549
7	15871	26718	14698	33957	13870	99193	16653	119298	25288	82322	29541	20640
8	16085	27752	15229	36008	13867	89473	16679	119865	25839	83373	29361	22295
9	16100	28328	15733	33385	14352	100576	16661	119520	24347	82701	28561	22876
10	15880	26869	15288	35720	14049	93637	17112	118214	25657	81731	28252	23849
11	15990	28063	15303	33520	14885	92413	17379	118038	25908	80781	27537	20612
12	16244	27689	15574	33831	14473	89766	17317	120843	24534	83127	28376	21541
13	16500	27860	16338	33445	15103	91008	17610	122458	25534	87783	27424	24036
14	16542	28292	15994	36170	14251	89516	17934	121326	26347	83054	27874	22456
15	16771	28032	15933	35624	15594	89446	18722	122500	26204	84154	27557	21287
16	17385	28517	16515	34978	15050	91004	18627	122620	26090	84371	26840	21765

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	25373	89908	101714	20358	13626	25800	47856	9025	7989	48537	14320
2	27600	75217	87288	21075	14317	24109	43302	9658	8164	41914	14790
3	28221	79211	90064	21379	14263	23969	40915	8246	7879	39199	13931
4	25824	79797	81857	21743	13625	22710	39682	7611	7961	35422	13136
5	27241	76692	89448	20971	13848	21166	42017	8538	7849	41255	12768
6	27800	74350	86101	20519	14280	21965	41371	8765	8041	39511	12913
7	25823	78115	80766	23110	14498	22516	38214	7652	7386	36633	12860
8	26748	74361	80347	23556	14840	22316	36010	8022	7287	34337	13600
9	24714	82828	83427	22800	13708	22535	38811	8489	7432	36744	14124
10	25759	81054	82141	23278	14906	21864	37804	8338	8032	34768	14075
11	24783	79638	81339	22593	14827	22121	38369	7735	7664	36310	13722
12	24973	74709	79025	23061	14753	21364	35970	7768	7935	34439	12955
13	24332	73536	80299	24327	14314	22838	34707	7928	7533	32255	13468
14	24015	78527	82991	23494	14070	23029	37621	8029	7776	34369	12993
15	24871	83574	82590	24153	14042	22132	36071	7885	7306	35824	13626
16	24333	76869	91065	26547	14807	21531	36255	7763	6937	32652	13375

Table D.4 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	18019	31126	18837	39745	16390	126472	20688	127335	28063	91837	38336	29273
2	19482	32987	19883	38498	16952	110182	22644	124237	29969	83120	36064	27074
3	19391	33397	19910	39608	17013	104251	22183	118492	29614	85842	36611	26703
4	20444	32537	18956	40038	18881	98675	21587	118786	30425	83895	34959	28834
5	21527	33272	19092	36738	18782	97995	21894	118112	32422	80875	34891	28833
6	21425	33352	20275	39243	18243	92456	23025	117958	32857	84584	33964	28659
7	20752	33086	20268	38581	17334	93254	22807	92270	32179	83878	33591	26416
8	22257	36400	19652	40006	18914	92033	23899	118048	33328	84496	32580	27007
9	21557	35763	20501	38137	18779	96201	24286	121029	32470	83838	33692	26431
10	21590	33280	20580	40871	18854	91344	23137	115903	33881	87452	33374	26517
11	22161	35241	21199	38321	18942	92991	24911	120659	33708	85532	33669	25010
12	22089	37299	20517	36823	19931	90617	23560	119255	33156	87711	32612	26694
13	22704	34696	20076	39193	19739	90405	24726	122402	33202	87122	31506	25676
14	22775	37171	20604	39587	20926	89350	25506	121185	33634	90318	32470	25044
15	23100	35399	20806	36875	19055	93602	26148	118667	33729	90974	31769	25479
16	23385	36980	21587	36452	20159	90208	25443	120219	33471	89287	31182	24797

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	29450	92076	99125	23453	18373	36520	59182	11948	10910	54244	18439
2	30635	79947	88061	25173	18423	28721	54235	11594	9938	45412	17419
3	31272	85073	90897	25386	17625	29922	48909	10290	9618	47912	17807
4	32103	83600	89882	24809	18011	26914	50776	10046	9213	43712	16389
5	33024	82914	89165	25042	17286	28106	46593	11264	9107	40824	16451
6	30397	84216	91982	25138	17451	25112	47012	9489	9335	42715	15971
7	28257	91254	92270	25677	17194	28802	46324	8996	8475	38579	14823
8	30830	78704	88187	26155	17620	25071	41314	8879	9090	40333	14893
9	28140	86599	91826	24578	16798	27159	42194	9854	9291	37876	14644
10	27821	85828	94787	25360	16352	25525	39847	8867	8817	36457	13986
11	25858	83903	87211	25145	16818	24995	40831	8613	8087	34776	14365
12	28438	82992	90646	25981	16712	25214	40284	8942	8532	41773	14400
13	26914	82683	88469	25853	17160	25071	38686	8928	8122	35332	14113
14	26955	86369	91570	25884	16433	24967	40505	8651	8024	34631	14011
15	27323	90760	93102	25067	17883	25030	40512	8691	8360	37388	15509
16	27589	90317	89165	25794	16081	24786	38060	8912	8228	36398	14204

E Minimum Number of Routing Tracks Measurements

Table E.1 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	9	12	9	14	10	27	10	25	12	22	13	14
2	10	12	10	16	11	21	10	25	11	21	13	14
3	10	13	10	13	10	21	10	26	12	22	14	13
4	10	12	10	12	11	22	10	25	13	22	12	14
5	9	12	11	12	11	19	10	25	12	22	12	16
6	10	13	10	12	12	20	11	25	13	21	11	13
7	10	13	11	12	11	18	10	24	12	21	11	14
8	10	13	11	12	12	17	12	24	14	21	11	12
9	10	14	10	12	11	21	11	25	13	21	11	13
10	10	13	12	13	13	20	11	25	13	22	11	14
11	12	15	11	12	12	19	11	26	13	22	11	15
12	10	14	12	13	13	19	12	28	14	22	11	13
13	11	14	12	13	13	18	12	26	14	23	10	13
14	11	14	11	13	13	20	11	27	14	22	11	14
15	11	14	12	11	15	19	12	26	14	22	11	14
16	11	15	12	11	16	20	13	28	14	23	10	13

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	11	22	27	10	12	13	17	11	9	15	11
2	13	21	22	12	13	13	16	10	10	14	12
3	13	21	21	11	12	12	16	12	9	15	12
4	11	20	21	13	12	12	14	9	9	14	11
5	11	19	21	13	12	11	13	10	8	13	10
6	11	20	23	13	12	11	15	10	10	14	10
7	11	21	21	13	12	12	13	9	9	15	11
8	10	21	21	12	12	10	14	10	8	14	11
9	9	19	22	12	14	13	14	9	10	13	11
10	12	21	22	12	12	12	14	12	9	13	11
11	10	20	22	12	13	12	13	9	9	13	11
12	11	21	26	13	13	11	15	10	9	16	11
13	10	20	25	13	13	12	15	10	10	15	11
14	11	21	21	12	12	11	12	10	9	15	11
15	10	20	22	13	13	14	12	10	9	13	12
16	10	23	23	12	14	13	13	9	10	16	11

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	9	15	21	10	23	15	15
2	10	14	19	11	22	15	16
3	10	10	28	11	19	11	14
4	13	12	19	12	19	12	14
6	7	13	19	12	19	13	14
8	8	10	18	11	19	13	16
11	8	15	18	12	17	13	17
12	8	16	26	15	18	12	16
13	8	13	16	13	19	12	16
14	6	19	21	13	18	13	17
16	12	15	19	13	20	15	17

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	10	15	11	9	12	6	40	31
2	12	12	10	8	15	5	29	28
3	14	15	9	8	17	4	27	28
4	12	14	10	8	12	4	28	21
6	12	16	9	10	14	4	23	19
8	14	14	9	9	13	4	20	18
11	13	15	11	10	14	4	22	17
12	14	15	9	11	12	3	20	18
13	13	15	9	12	11	4	19	17
14	14	14	9	11	12	4	20	17
16	15	15	11	10	15	4	18	16

Table E.2 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	11	13	13	14	13	28	13	24	15	21	17	15
2	11	15	13	15	14	20	13	25	14	22	16	16
3	12	15	14	15	14	22	14	24	16	22	15	17
4	12	19	13	12	14	22	16	26	15	21	14	15
5	12	18	14	14	16	22	14	24	16	22	14	17
6	12	18	15	12	15	21	14	25	16	22	12	16
7	13	18	15	14	15	19	15	25	16	22	13	16
8	12	16	15	14	15	18	15	26	16	22	13	16
9	13	19	15	13	16	18	15	25	16	24	12	14
10	13	16	16	14	16	19	15	27	16	23	13	17
11	14	18	17	14	17	20	16	27	17	22	13	17
12	13	19	16	13	16	19	16	27	17	23	12	15
13	13	19	17	13	17	20	17	26	17	24	11	17
14	14	20	15	15	19	22	17	31	16	25	12	16
16	14	18	15	11	16	19	16	26	17	24	12	16

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	14	23	24	12	17	18	20	14	12	19	15
2	13	20	23	13	16	16	15	12	12	19	14
3	14	23	24	13	13	15	15	13	11	17	14
4	12	21	22	13	18	13	18	10	10	16	13
5	13	21	25	13	16	13	14	11	11	19	13
6	12	21	25	12	16	13	16	9	11	16	12
7	12	22	25	13	17	13	15	12	11	17	12
8	12	22	23	12	16	13	15	10	9	16	12
9	11	21	23	12	14	13	13	10	10	15	12
10	11	22	25	15	14	12	13	10	10	15	12
11	12	23	24	12	14	13	15	11	10	16	12
12	12	24	23	12	15	14	14	11	10	19	12
13	12	25	24	13	15	13	17	9	9	19	12
14	11	25	26	13	14	13	14	9	9	14	12
16	12	25	24	13	14	12	13	9	9	14	11

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	8	15	21	15	23	16	18
2	8	16	24	13	21	15	17
3	10	19	24	14	22	16	19
4	9	15	23	14	23	15	17
6	7	15	22	15	20	16	17
8	8	13	22	14	22	13	18
11	8	12	26	15	23	13	17
12	7	18	19	15	21	14	18
13	7	17	20	15	21	15	16
14	10	15	24	15	21	13	19
16	10	19	21	14	23	15	17

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	17	20	12	13	18	8	38	34
2	14	17	11	12	15	6	28	27
3	16	17	11	10	16	4	29	23
4	16	18	11	11	17	6	26	21
6	16	18	12	12	17	5	21	19
8	17	18	12	12	16	4	22	18
11	16	18	11	10	18	4	20	17
12	18	20	11	12	17	4	21	19
13	16	19	11	10	18	4	19	17
14	17	20	10	9	17	4	20	17
16	17	20	11	11	17	5	20	18

Table E.3 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	10	12	9	12	10	28	10	25	11	20	13	13
2	9	12	10	13	10	21	10	23	11	20	12	13
3	10	12	10	13	10	23	10	25	12	21	13	14
4	10	13	9	13	11	20	10	23	11	21	12	13
5	9	12	10	11	11	20	10	24	11	20	12	15
6	9	12	10	11	11	20	11	25	12	22	11	14
7	9	12	10	12	12	19	10	23	13	20	12	12
8	10	12	11	12	11	17	12	24	13	21	11	15
9	9	14	11	10	12	19	11	24	12	20	11	13
10	9	12	11	12	11	19	10	26	13	21	12	15
11	10	13	10	11	13	19	10	24	14	21	11	12
12	9	12	11	11	12	18	10	25	12	21	11	14
13	9	13	12	12	13	19	11	25	14	21	10	15
14	11	13	10	12	12	18	11	24	14	22	11	14
15	11	13	11	12	12	17	12	24	13	21	11	14
16	10	12	11	11	13	17	12	25	12	20	11	13

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	10	22	28	13	11	13	16	10	10	18	12
2	12	18	22	13	12	12	14	11	10	17	12
3	11	21	23	12	13	13	14	9	10	14	12
4	10	21	20	11	13	13	13	9	10	15	10
5	10	21	24	11	12	10	14	10	8	16	10
6	10	19	21	12	13	12	15	11	10	15	11
7	10	20	21	12	12	12	13	9	9	15	11
8	10	19	20	12	14	12	14	10	9	14	12
9	11	22	21	13	13	11	15	11	9	14	12
10	10	21	21	12	13	11	13	10	10	13	12
11	10	21	20	13	13	11	13	8	11	14	13
12	11	19	19	12	13	12	13	9	10	14	10
13	9	21	21	12	16	12	13	9	9	12	11
14	9	21	22	12	13	12	13	9	9	13	12
15	10	22	20	12	12	11	13	10	9	15	13
16	9	19	23	12	13	13	13	9	9	13	12

Table E.4 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	10	15	13	14	13	25	12	24	15	22	15	17
2	11	15	14	13	13	22	14	25	15	21	15	15
3	11	15	14	13	14	21	14	25	14	21	15	16
4	11	15	13	14	16	20	13	25	14	22	14	17
5	12	15	13	15	15	20	14	24	16	20	14	17
6	12	16	14	16	15	18	14	24	17	21	14	18
7	13	14	14	13	15	18	14	23	17	21	13	16
8	13	16	14	13	14	18	15	25	16	21	13	17
9	13	16	14	14	15	20	16	24	16	21	14	16
10	12	15	15	14	15	18	14	23	17	21	13	16
11	13	17	15	13	16	18	15	25	17	21	14	16
12	12	17	15	12	16	18	15	23	16	21	14	17
13	13	16	15	12	16	19	15	28	16	22	12	16
14	13	17	16	14	17	17	16	23	16	22	14	15
15	14	17	15	13	16	19	17	23	17	22	14	15
16	14	17	15	13	16	18	15	27	17	22	12	16

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	13	23	23	12	15	19	21	14	13	20	14
2	12	19	21	12	15	15	17	13	11	17	14
3	13	21	22	12	15	15	16	11	11	19	14
4	13	20	22	13	16	14	18	12	12	17	13
5	14	21	22	12	15	15	15	12	11	15	14
6	12	21	23	13	15	13	16	11	11	17	14
7	11	23	23	12	16	15	16	11	11	16	11
8	11	21	22	12	15	13	16	11	11	17	12
9	11	22	24	11	14	14	15	11	13	15	13
10	12	22	26	13	14	14	14	10	11	16	12
11	11	21	22	12	16	14	14	10	9	16	12
12	12	23	23	13	16	13	15	11	10	17	12
13	12	22	25	14	15	14	14	11	10	15	11
14	12	23	24	12	15	13	15	10	10	14	12
15	11	24	27	13	16	14	14	10	10	15	13
16	11	25	22	13	14	14	14	11	11	15	12

F Critical Path Delay Measurements

Table F.1 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	7.16e-08	8.14e-08	6.25e-08	7.60e-08	6.28e-08	1.42e-07	6.79e-08	1.48e-07	6.89e-08	1.04e-07	5.09e-08	7.26e-08
2	8.37e-08	9.13e-08	7.14e-08	8.29e-08	6.46e-08	1.48e-07	6.27e-08	1.38e-07	7.31e-08	1.24e-07	5.99e-08	7.15e-08
3	7.53e-08	8.69e-08	6.52e-08	7.92e-08	7.71e-08	1.52e-07	7.70e-08	1.38e-07	6.26e-08	1.13e-07	5.28e-08	6.62e-08
4	7.93e-08	8.92e-08	6.49e-08	9.11e-08	6.55e-08	1.59e-07	6.29e-08	1.38e-07	7.02e-08	1.28e-07	6.81e-08	7.30e-08
5	9.62e-08	9.67e-08	6.43e-08	8.61e-08	6.51e-08	1.65e-07	7.09e-08	1.43e-07	7.43e-08	1.40e-07	5.43e-08	6.95e-08
6	8.11e-08	1.03e-07	7.67e-08	8.07e-08	6.63e-08	1.64e-07	6.35e-08	1.38e-07	7.68e-08	1.25e-07	5.33e-08	8.44e-08
7	8.58e-08	8.35e-08	8.08e-08	1.05e-07	7.01e-08	1.51e-07	7.09e-08	1.62e-07	7.62e-08	1.29e-07	5.25e-08	8.12e-08
8	8.35e-08	1.08e-07	6.59e-08	8.94e-08	6.57e-08	1.53e-07	6.97e-08	1.59e-07	7.28e-08	1.60e-07	5.84e-08	7.85e-08
9	8.14e-08	9.56e-08	6.77e-08	8.67e-08	7.58e-08	1.67e-07	8.46e-08	1.48e-07	8.00e-08	1.35e-07	5.91e-08	7.44e-08
10	9.03e-08	9.33e-08	7.13e-08	9.40e-08	6.96e-08	1.77e-07	7.33e-08	1.47e-07	1.13e-07	1.42e-07	5.36e-08	6.64e-08
11	8.09e-08	1.02e-07	7.49e-08	8.89e-08	7.10e-08	1.47e-07	7.41e-08	1.41e-07	7.55e-08	1.32e-07	7.24e-08	6.68e-08
12	7.98e-08	9.86e-08	8.08e-08	8.77e-08	6.52e-08	1.51e-07	6.91e-08	1.41e-07	7.72e-08	1.44e-07	5.61e-08	7.29e-08
13	8.51e-08	9.26e-08	7.61e-08	8.67e-08	6.65e-08	1.55e-07	8.01e-08	1.44e-07	7.27e-08	1.21e-07	5.95e-08	7.90e-08
14	8.04e-08	1.02e-07	7.94e-08	8.89e-08	7.17e-08	1.61e-07	9.23e-08	1.52e-07	8.05e-08	1.36e-07	6.37e-08	7.45e-08
15	8.35e-08	9.58e-08	8.44e-08	8.92e-08	7.00e-08	1.65e-07	8.32e-08	1.74e-07	7.38e-08	1.42e-07	5.23e-08	7.08e-08
16	7.35e-08	1.06e-07	7.19e-08	8.92e-08	6.79e-08	1.56e-07	7.03e-08	1.42e-07	1.05e-07	1.31e-07	6.97e-08	7.56e-08

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	5.90e-08	9.35e-08	1.15e-07	1.12e-07	6.57e-08	6.85e-08	1.01e-07	6.54e-08	7.77e-08	1.00e-07	6.70e-08
2	4.93e-08	1.06e-07	1.19e-07	1.15e-07	6.41e-08	7.34e-08	9.05e-08	5.53e-08	7.41e-08	1.16e-07	6.64e-08
3	5.42e-08	9.36e-08	1.18e-07	1.21e-07	6.23e-08	8.22e-08	9.44e-08	5.96e-08	8.35e-08	9.00e-08	7.53e-08
4	5.64e-08	9.28e-08	1.23e-07	1.20e-07	6.90e-08	8.24e-08	1.08e-07	5.82e-08	8.16e-08	1.07e-07	8.02e-08
5	5.82e-08	8.68e-08	1.15e-07	1.14e-07	6.88e-08	7.56e-08	1.11e-07	5.07e-08	7.77e-08	9.93e-08	7.59e-08
6	5.28e-08	1.02e-07	1.37e-07	1.21e-07	7.13e-08	6.55e-08	1.16e-07	5.46e-08	8.30e-08	9.84e-08	7.41e-08
7	5.26e-08	9.54e-08	1.11e-07	1.13e-07	6.71e-08	6.75e-08	1.14e-07	5.78e-08	7.44e-08	1.15e-07	6.17e-08
8	7.03e-08	9.77e-08	1.31e-07	1.56e-07	6.52e-08	7.32e-08	1.03e-07	6.03e-08	7.60e-08	1.12e-07	7.13e-08
9	6.80e-08	1.02e-07	1.30e-07	1.20e-07	6.35e-08	7.03e-08	9.24e-08	5.52e-08	8.81e-08	1.09e-07	7.19e-08
10	5.33e-08	1.00e-07	1.19e-07	1.22e-07	6.46e-08	7.52e-08	1.06e-07	6.44e-08	8.12e-08	8.64e-08	6.88e-08
11	5.84e-08	9.09e-08	1.27e-07	1.18e-07	6.70e-08	6.91e-08	1.01e-07	5.73e-08	7.50e-08	9.97e-08	7.26e-08
12	5.37e-08	9.45e-08	1.34e-07	1.14e-07	6.70e-08	6.83e-08	1.03e-07	6.70e-08	8.50e-08	1.03e-07	6.36e-08
13	5.32e-08	1.15e-07	1.24e-07	1.19e-07	6.53e-08	7.22e-08	9.09e-08	5.97e-08	8.48e-08	1.01e-07	7.09e-08
14	6.02e-08	1.05e-07	1.40e-07	1.23e-07	6.77e-08	7.00e-08	1.10e-07	6.73e-08	7.68e-08	1.05e-07	7.35e-08
15	6.38e-08	9.26e-08	1.34e-07	1.23e-07	6.50e-08	7.97e-08	9.45e-08	6.14e-08	7.06e-08	9.79e-08	7.72e-08
16	5.96e-08	1.02e-07	1.30e-07	1.21e-07	6.70e-08	7.14e-08	1.01e-07	5.31e-08	8.53e-08	1.02e-07	7.56e-08

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	8.71e-08	7.69e-08	3.01e-07	8.24e-08	1.44e-07	1.91e-07	1.97e-07
2	8.05e-08	7.73e-08	3.43e-07	9.21e-08	1.50e-07	2.24e-07	1.78e-07
3	8.71e-08	7.95e-08	2.89e-07	8.55e-08	1.38e-07	1.88e-07	1.75e-07
4	8.35e-08	9.11e-08	3.24e-07	8.72e-08	1.59e-07	2.04e-07	1.96e-07
6	9.91e-08	9.14e-08	2.77e-07	1.02e-07	1.54e-07	2.04e-07	1.90e-07
8	8.10e-08	8.28e-08	3.03e-07	1.02e-07	1.37e-07	2.18e-07	1.73e-07
11	7.59e-08	7.58e-08	3.19e-07	9.18e-08	1.48e-07	2.10e-07	1.87e-07
12	8.86e-08	7.58e-08	3.17e-07	9.85e-08	1.42e-07	1.99e-07	1.97e-07
13	7.66e-08	7.42e-08	3.21e-07	8.73e-08	1.57e-07	2.19e-07	1.90e-07
14	7.26e-08	7.60e-08	2.82e-07	9.53e-08	1.46e-07	1.81e-07	2.05e-07
16	6.67e-08	7.12e-08	2.78e-07	9.46e-08	1.69e-07	1.76e-07	1.89e-07

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	6.05e-08	1.57e-07	6.17e-08	1.16e-07	8.26e-08	2.49e-08	1.10e-07	9.73e-08
2	6.42e-08	1.79e-07	5.55e-08	1.28e-07	7.86e-08	2.08e-08	1.15e-07	1.03e-07
3	6.83e-08	1.75e-07	5.25e-08	1.38e-07	8.69e-08	2.44e-08	1.18e-07	1.02e-07
4	7.39e-08	1.95e-07	5.69e-08	1.09e-07	7.65e-08	2.32e-08	1.16e-07	1.06e-07
6	6.64e-08	1.99e-07	5.13e-08	1.44e-07	8.67e-08	2.15e-08	1.14e-07	1.09e-07
8	7.02e-08	1.83e-07	5.76e-08	1.46e-07	8.28e-08	2.43e-08	1.26e-07	1.09e-07
11	7.55e-08	1.87e-07	5.35e-08	1.15e-07	9.13e-08	2.26e-08	1.24e-07	1.11e-07
12	7.10e-08	1.62e-07	7.09e-08	1.27e-07	9.36e-08	2.43e-08	1.15e-07	1.15e-07
13	7.18e-08	1.76e-07	4.78e-08	1.41e-07	9.17e-08	2.21e-08	1.11e-07	1.19e-07
14	7.04e-08	1.48e-07	6.54e-08	1.31e-07	9.29e-08	2.44e-08	1.07e-07	1.11e-07
16	6.45e-08	1.65e-07	4.58e-08	1.41e-07	9.47e-08	2.44e-08	1.10e-07	1.17e-07

Table F.2 - Partitioning Condition: t1 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	7.59e-08	8.76e-08	7.53e-08	8.65e-08	7.07e-08	1.36e-07	7.86e-08	1.34e-07	6.77e-08	1.10e-07	5.60e-08	7.45e-08
2	8.64e-08	1.01e-07	7.51e-08	9.21e-08	6.81e-08	1.38e-07	7.32e-08	1.25e-07	8.63e-08	1.10e-07	5.73e-08	7.08e-08
3	8.11e-08	1.01e-07	6.72e-08	8.76e-08	7.23e-08	1.51e-07	7.67e-08	1.41e-07	7.86e-08	1.17e-07	5.45e-08	7.26e-08
4	1.02e-07	9.71e-08	7.49e-08	8.19e-08	7.82e-08	1.53e-07	8.88e-08	1.53e-07	8.00e-08	1.27e-07	5.80e-08	7.54e-08
5	8.95e-08	1.03e-07	7.37e-08	9.14e-08	6.51e-08	1.45e-07	8.06e-08	1.67e-07	7.65e-08	1.27e-07	8.16e-08	8.02e-08
6	8.99e-08	9.22e-08	7.44e-08	9.97e-08	7.61e-08	1.65e-07	8.70e-08	1.31e-07	7.86e-08	1.27e-07	6.06e-08	7.21e-08
7	9.36e-08	9.80e-08	7.21e-08	9.11e-08	7.76e-08	1.79e-07	8.59e-08	1.44e-07	8.74e-08	1.35e-07	5.42e-08	7.37e-08
8	8.98e-08	1.00e-07	8.52e-08	9.14e-08	7.14e-08	1.43e-07	8.40e-08	1.35e-07	8.27e-08	1.48e-07	5.57e-08	7.81e-08
9	9.29e-08	9.86e-08	7.68e-08	9.37e-08	7.61e-08	1.51e-07	8.02e-08	1.50e-07	8.17e-08	1.28e-07	5.91e-08	7.51e-08
10	7.98e-08	1.03e-07	8.34e-08	8.44e-08	7.51e-08	1.52e-07	7.81e-08	1.38e-07	8.72e-08	1.51e-07	6.37e-08	7.26e-08
11	8.27e-08	1.13e-07	8.86e-08	8.64e-08	7.43e-08	1.61e-07	7.32e-08	1.43e-07	8.62e-08	1.47e-07	5.90e-08	7.70e-08
12	8.28e-08	9.67e-08	7.74e-08	8.67e-08	7.28e-08	1.56e-07	7.98e-08	1.44e-07	8.06e-08	1.42e-07	5.72e-08	7.54e-08
13	9.26e-08	1.01e-07	7.85e-08	8.30e-08	7.49e-08	1.46e-07	7.79e-08	1.66e-07	7.90e-08	1.43e-07	6.67e-08	7.22e-08
14	7.68e-08	1.10e-07	1.07e-07	8.78e-08	6.63e-08	1.45e-07	7.98e-08	1.45e-07	8.96e-08	1.44e-07	5.10e-08	8.54e-08
16	8.16e-08	1.00e-07	9.05e-08	9.02e-08	8.62e-08	1.79e-07	8.38e-08	1.92e-07	9.19e-08	1.31e-07	5.30e-08	7.43e-08

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	6.46e-08	8.67e-08	1.35e-07	1.14e-07	6.77e-08	6.88e-08	1.02e-07	5.90e-08	7.63e-08	9.69e-08	7.27e-08
2	6.55e-08	1.07e-07	1.14e-07	1.28e-07	6.47e-08	8.45e-08	9.37e-08	7.86e-08	8.13e-08	1.09e-07	7.05e-08
3	5.59e-08	1.03e-07	1.24e-07	1.18e-07	7.39e-08	7.65e-08	1.07e-07	6.44e-08	8.43e-08	1.03e-07	6.82e-08
4	5.16e-08	1.02e-07	1.21e-07	1.19e-07	6.58e-08	7.33e-08	1.04e-07	5.61e-08	8.54e-08	1.00e-07	7.65e-08
5	5.09e-08	8.68e-08	1.24e-07	1.18e-07	6.65e-08	7.12e-08	1.00e-07	6.82e-08	7.75e-08	9.86e-08	6.97e-08
6	5.67e-08	9.22e-08	1.23e-07	1.25e-07	6.88e-08	7.04e-08	1.13e-07	6.73e-08	7.41e-08	9.74e-08	8.00e-08
7	5.65e-08	9.73e-08	1.27e-07	1.43e-07	6.52e-08	7.96e-08	1.11e-07	5.73e-08	7.35e-08	1.12e-07	7.14e-08
8	6.35e-08	9.89e-08	1.24e-07	1.59e-07	7.11e-08	7.87e-08	1.19e-07	5.59e-08	7.94e-08	9.64e-08	7.55e-08
9	5.09e-08	1.07e-07	1.45e-07	1.33e-07	6.65e-08	7.48e-08	9.67e-08	6.19e-08	8.63e-08	1.09e-07	6.32e-08
10	6.01e-08	9.52e-08	1.34e-07	1.15e-07	6.98e-08	7.31e-08	1.01e-07	6.02e-08	8.75e-08	8.97e-08	6.95e-08
11	5.66e-08	1.04e-07	1.28e-07	1.68e-07	5.86e-08	6.80e-08	9.68e-08	6.68e-08	7.24e-08	1.06e-07	7.41e-08
12	5.02e-08	9.57e-08	1.15e-07	1.18e-07	6.88e-08	7.31e-08	9.45e-08	5.53e-08	7.95e-08	9.45e-08	7.59e-08
13	5.70e-08	1.08e-07	1.35e-07	1.20e-07	6.83e-08	7.78e-08	9.70e-08	6.35e-08	8.54e-08	9.67e-08	7.78e-08
14	6.91e-08	1.24e-07	1.27e-07	1.17e-07	6.76e-08	7.14e-08	1.10e-07	5.88e-08	7.88e-08	1.01e-07	7.29e-08
16	5.33e-08	9.35e-08	1.21e-07	1.13e-07	6.74e-08	1.03e-07	1.12e-07	5.46e-08	9.82e-08	1.03e-07	1.29e-07

Cluster	code_seq dp	dcu dpath	ex dpath	exponent dp	icu dpath	incmod	imdr dpath
1	8.33e-08	7.66e-08	2.89e-07	1.02e-07	1.62e-07	1.89e-07	2.12e-07
2	8.26e-08	7.59e-08	3.27e-07	9.35e-08	1.59e-07	1.83e-07	1.96e-07
3	7.62e-08	7.91e-08	2.70e-07	9.14e-08	1.33e-07	1.96e-07	1.72e-07
4	8.61e-08	8.22e-08	3.16e-07	9.53e-08	1.57e-07	1.77e-07	1.84e-07
6	7.50e-08	7.38e-08	3.05e-07	9.71e-08	1.36e-07	1.76e-07	1.98e-07
8	8.91e-08	7.52e-08	2.85e-07	9.59e-08	1.49e-07	1.82e-07	1.91e-07
11	7.38e-08	9.32e-08	2.89e-07	1.03e-07	1.69e-07	1.97e-07	2.01e-07
12	7.82e-08	6.95e-08	2.97e-07	9.15e-08	1.63e-07	2.02e-07	1.59e-07
13	6.93e-08	7.57e-08	2.97e-07	9.01e-08	1.67e-07	2.19e-07	1.90e-07
14	7.44e-08	6.61e-08	3.02e-07	8.73e-08	1.58e-07	1.85e-07	1.76e-07
16	7.34e-08	6.67e-08	2.65e-07	8.52e-08	1.42e-07	1.95e-07	1.93e-07

Cluster	mantissa dp	multmod dp	pipe dpath	smu dpath	ucode dat	ucode reg	s38417	s38584.1
1	7.68e-08	1.63e-07	6.82e-08	1.63e-07	8.27e-08	1.79e-08	1.31e-07	8.80e-08
2	7.12e-08	1.93e-07	4.96e-08	1.10e-07	8.63e-08	1.91e-08	1.12e-07	1.06e-07
3	7.53e-08	1.91e-07	6.00e-08	1.53e-07	8.51e-08	2.08e-08	1.34e-07	9.03e-08
4	6.69e-08	1.89e-07	5.52e-08	1.44e-07	8.89e-08	2.20e-08	1.12e-07	1.18e-07
6	6.51e-08	1.89e-07	5.17e-08	1.42e-07	8.19e-08	2.09e-08	1.15e-07	1.05e-07
8	6.99e-08	1.89e-07	5.40e-08	1.23e-07	8.85e-08	2.32e-08	1.19e-07	1.01e-07
11	8.59e-08	1.83e-07	5.83e-08	1.34e-07	9.50e-08	2.26e-08	1.20e-07	1.13e-07
12	7.17e-08	2.07e-07	5.40e-08	1.40e-07	8.84e-08	2.20e-08	1.26e-07	1.11e-07
13	7.97e-08	1.66e-07	4.90e-08	1.15e-07	8.20e-08	2.32e-08	1.21e-07	1.11e-07
14	7.56e-08	1.82e-07	6.64e-08	1.26e-07	8.72e-08	2.49e-08	1.11e-07	1.19e-07
16	7.74e-08	1.96e-07	5.57e-08	1.48e-07	9.46e-08	2.21e-08	1.39e-07	1.09e-07

Table F.3 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Minimum Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	7.01e-08	7.63e-08	6.90e-08	7.79e-08	6.81e-08	1.28e-07	5.67e-08	1.30e-07	8.50e-08	1.12e-07	4.75e-08	6.84e-08
2	6.91e-08	8.56e-08	6.64e-08	8.18e-08	6.28e-08	1.37e-07	7.03e-08	1.42e-07	6.73e-08	1.26e-07	4.77e-08	6.93e-08
3	6.99e-08	8.78e-08	6.83e-08	7.91e-08	7.59e-08	1.45e-07	6.53e-08	1.52e-07	6.45e-08	1.22e-07	5.13e-08	7.34e-08
4	7.21e-08	8.79e-08	6.36e-08	8.39e-08	8.14e-08	1.60e-07	6.52e-08	1.49e-07	7.90e-08	1.18e-07	5.74e-08	7.91e-08
5	7.86e-08	9.39e-08	6.79e-08	9.12e-08	6.58e-08	1.56e-07	6.93e-08	1.41e-07	8.28e-08	1.59e-07	5.54e-08	7.18e-08
6	7.27e-08	9.02e-08	6.54e-08	8.24e-08	6.41e-08	1.50e-07	6.49e-08	1.49e-07	7.02e-08	1.16e-07	5.37e-08	7.20e-08
7	7.64e-08	9.06e-08	7.86e-08	8.45e-08	6.70e-08	1.47e-07	7.06e-08	1.47e-07	8.11e-08	1.24e-07	5.59e-08	8.17e-08
8	7.80e-08	9.34e-08	7.02e-08	8.86e-08	7.24e-08	1.44e-07	6.61e-08	1.52e-07	6.90e-08	1.27e-07	5.82e-08	7.51e-08
9	7.70e-08	1.00e-07	7.04e-08	9.09e-08	6.79e-08	1.48e-07	7.04e-08	1.59e-07	7.40e-08	1.25e-07	5.24e-08	7.83e-08
10	7.95e-08	9.04e-08	6.70e-08	8.95e-08	6.87e-08	1.61e-07	7.09e-08	1.47e-07	7.66e-08	1.23e-07	5.52e-08	7.54e-08
11	6.98e-08	9.12e-08	7.50e-08	8.62e-08	6.84e-08	1.47e-07	6.81e-08	1.45e-07	7.50e-08	1.28e-07	6.08e-08	7.87e-08
12	7.47e-08	9.00e-08	7.32e-08	8.44e-08	7.05e-08	1.42e-07	6.74e-08	1.54e-07	7.61e-08	1.29e-07	5.62e-08	7.57e-08
13	7.47e-08	9.15e-08	7.15e-08	9.16e-08	7.33e-08	1.50e-07	7.37e-08	1.50e-07	7.70e-08	1.21e-07	5.83e-08	7.19e-08
14	7.67e-08	9.27e-08	8.27e-08	9.40e-08	6.65e-08	1.56e-07	7.54e-08	1.60e-07	8.75e-08	1.18e-07	5.71e-08	8.22e-08
15	7.81e-08	1.02e-07	7.21e-08	9.78e-08	7.22e-08	1.58e-07	8.73e-08	1.68e-07	7.56e-08	1.46e-07	5.20e-08	7.38e-08
16	7.75e-08	9.57e-08	7.25e-08	8.49e-08	7.55e-08	1.41e-07	7.24e-08	1.60e-07	8.21e-08	1.24e-07	5.85e-08	7.62e-08

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	5.58e-08	8.57e-08	1.26e-07	1.00e-07	6.10e-08	7.31e-08	1.05e-07	6.12e-08	7.54e-08	1.06e-07	6.64e-08
2	5.87e-08	1.18e-07	1.23e-07	1.11e-07	6.56e-08	7.23e-08	9.48e-08	6.25e-08	8.43e-08	1.08e-07	6.74e-08
3	5.23e-08	1.08e-07	1.30e-07	1.15e-07	6.71e-08	8.01e-08	1.06e-07	6.31e-08	8.18e-08	9.97e-08	7.71e-08
4	7.08e-08	9.99e-08	1.07e-07	1.16e-07	7.48e-08	8.79e-08	1.03e-07	5.73e-08	8.07e-08	8.89e-08	7.60e-08
5	5.62e-08	9.69e-08	1.32e-07	1.13e-07	6.59e-08	9.06e-08	1.14e-07	6.20e-08	8.47e-08	1.04e-07	6.99e-08
6	5.86e-08	1.08e-07	1.46e-07	1.00e-07	6.74e-08	7.09e-08	9.74e-08	6.61e-08	7.65e-08	1.06e-07	7.35e-08
7	6.11e-08	1.01e-07	1.32e-07	1.20e-07	7.88e-08	7.48e-08	9.20e-08	6.38e-08	7.77e-08	1.05e-07	7.38e-08
8	5.55e-08	9.46e-08	1.23e-07	1.14e-07	7.71e-08	7.90e-08	9.68e-08	5.81e-08	7.63e-08	9.11e-08	9.35e-08
9	5.58e-08	9.67e-08	1.32e-07	1.16e-07	6.41e-08	6.77e-08	1.09e-07	5.94e-08	8.29e-08	9.24e-08	7.04e-08
10	5.68e-08	1.07e-07	1.31e-07	1.31e-07	7.18e-08	7.06e-08	1.02e-07	6.20e-08	8.12e-08	9.97e-08	8.64e-08
11	5.33e-08	1.18e-07	1.34e-07	1.20e-07	7.01e-08	7.46e-08	9.16e-08	6.45e-08	8.11e-08	9.98e-08	6.88e-08
12	5.12e-08	1.07e-07	1.25e-07	1.20e-07	6.74e-08	7.71e-08	9.86e-08	6.32e-08	8.09e-08	1.05e-07	7.09e-08
13	5.70e-08	9.77e-08	1.35e-07	1.20e-07	6.84e-08	7.97e-08	1.08e-07	5.52e-08	8.29e-08	9.68e-08	7.46e-08
14	5.49e-08	9.06e-08	1.30e-07	1.12e-07	6.52e-08	8.53e-08	1.22e-07	6.09e-08	8.45e-08	1.04e-07	7.47e-08
15	5.72e-08	8.87e-08	1.19e-07	1.21e-07	6.87e-08	7.64e-08	1.03e-07	6.02e-08	8.45e-08	1.12e-07	7.51e-08
16	5.35e-08	9.17e-08	1.42e-07	1.16e-07	6.89e-08	7.15e-08	9.81e-08	6.11e-08	8.06e-08	1.09e-07	8.90e-08

Table F.4 - Partitioning Condition: t2 and $Desired\ Wirelength_{approx}$: Initial Wirelength

Cluster	alu4	apex2	apex4	des	ex5p	ex1010	misex3	pdc	seq	spla	bigkey	diffeq
1	8.06e-08	8.27e-08	7.82e-08	9.00e-08	7.41e-08	1.43e-07	7.38e-08	1.27e-07	7.12e-08	1.18e-07	5.95e-08	6.82e-08
2	8.73e-08	9.24e-08	7.74e-08	8.65e-08	8.17e-08	1.33e-07	7.32e-08	1.58e-07	7.57e-08	1.17e-07	5.78e-08	7.73e-08
3	7.85e-08	9.82e-08	7.67e-08	9.26e-08	8.39e-08	1.42e-07	7.26e-08	1.34e-07	9.11e-08	1.19e-07	6.79e-08	7.81e-08
4	8.61e-08	8.86e-08	7.76e-08	9.17e-08	7.03e-08	1.36e-07	8.62e-08	1.51e-07	7.94e-08	1.32e-07	5.39e-08	8.19e-08
5	8.54e-08	8.86e-08	7.77e-08	8.75e-08	8.10e-08	1.59e-07	8.35e-08	1.47e-07	7.54e-08	1.16e-07	7.86e-08	7.38e-08
6	8.92e-08	9.68e-08	9.81e-08	8.98e-08	6.91e-08	1.42e-07	7.91e-08	1.63e-07	7.82e-08	1.33e-07	7.39e-08	7.24e-08
7	8.15e-08	9.09e-08	7.77e-08	8.88e-08	7.14e-08	1.53e-07	7.70e-08	1.47e-07	7.79e-08	1.29e-07	6.41e-08	7.86e-08
8	9.69e-08	1.08e-07	8.21e-08	9.13e-08	7.37e-08	1.49e-07	9.95e-08	1.64e-07	8.47e-08	1.18e-07	6.17e-08	7.06e-08
9	7.62e-08	1.09e-07	8.48e-08	8.49e-08	8.05e-08	1.41e-07	8.19e-08	1.64e-07	8.52e-08	1.38e-07	6.74e-08	7.67e-08
10	9.58e-08	9.91e-08	7.32e-08	9.83e-08	7.40e-08	1.44e-07	7.47e-08	1.55e-07	1.08e-07	1.40e-07	5.72e-08	7.56e-08
11	8.13e-08	1.01e-07	7.43e-08	8.47e-08	7.18e-08	1.52e-07	7.73e-08	1.46e-07	7.95e-08	1.19e-07	5.78e-08	9.39e-08
12	9.12e-08	9.48e-08	7.83e-08	9.12e-08	6.75e-08	1.50e-07	8.56e-08	1.48e-07	8.50e-08	1.26e-07	6.43e-08	7.81e-08
13	7.67e-08	1.10e-07	7.43e-08	9.63e-08	8.81e-08	1.43e-07	8.08e-08	1.41e-07	8.30e-08	1.32e-07	8.66e-08	7.38e-08
14	8.65e-08	1.00e-07	9.50e-08	9.54e-08	7.68e-08	1.56e-07	7.61e-08	1.61e-07	9.14e-08	1.29e-07	7.38e-08	7.33e-08
15	8.67e-08	1.06e-07	7.34e-08	1.28e-07	7.23e-08	1.58e-07	7.62e-08	1.49e-07	8.99e-08	1.43e-07	7.04e-08	7.72e-08
16	8.06e-08	1.05e-07	7.62e-08	1.04e-07	7.65e-08	1.50e-07	8.05e-08	1.43e-07	8.27e-08	1.33e-07	6.83e-08	8.97e-08

Cluster	dsip	elliptic	frisc	s298	tseng	display chip	img interp	input chip	peak chip	scale125 chip	scale2 chip
1	4.96e-08	9.56e-08	1.35e-07	1.14e-07	5.94e-08	7.04e-08	1.03e-07	5.58e-08	7.53e-08	9.61e-08	6.47e-08
2	6.11e-08	1.08e-07	1.23e-07	1.36e-07	6.89e-08	8.06e-08	1.10e-07	6.37e-08	7.71e-08	1.08e-07	6.97e-08
3	5.85e-08	1.09e-07	1.19e-07	1.21e-07	6.75e-08	7.18e-08	9.91e-08	6.52e-08	8.95e-08	9.73e-08	7.39e-08
4	5.52e-08	9.32e-08	1.20e-07	1.26e-07	7.78e-08	6.82e-08	1.15e-07	6.22e-08	7.30e-08	1.09e-07	6.72e-08
5	6.21e-08	1.04e-07	1.14e-07	1.38e-07	7.00e-08	7.43e-08	9.88e-08	6.26e-08	8.00e-08	9.56e-08	7.17e-08
6	6.43e-08	9.39e-08	1.17e-07	1.16e-07	6.57e-08	7.08e-08	1.05e-07	5.27e-08	7.06e-08	1.17e-07	7.88e-08
7	5.95e-08	8.96e-08	1.47e-07	1.19e-07	6.89e-08	7.47e-08	1.03e-07	6.27e-08	7.84e-08	9.80e-08	7.17e-08
8	7.01e-08	8.98e-08	1.22e-07	1.15e-07	7.01e-08	7.80e-08	1.02e-07	5.55e-08	7.74e-08	1.03e-07	7.88e-08
9	5.39e-08	9.90e-08	1.38e-07	1.32e-07	7.09e-08	6.94e-08	1.36e-07	5.72e-08	8.12e-08	9.77e-08	9.65e-08
10	5.99e-08	8.97e-08	1.24e-07	1.17e-07	6.65e-08	7.70e-08	9.82e-08	6.49e-08	8.85e-08	1.02e-07	7.50e-08
11	5.26e-08	1.05e-07	1.50e-07	1.19e-07	6.87e-08	7.49e-08	1.28e-07	5.85e-08	8.41e-08	9.75e-08	7.09e-08
12	5.20e-08	1.14e-07	1.72e-07	1.23e-07	6.92e-08	6.85e-08	9.83e-08	6.45e-08	9.07e-08	1.07e-07	7.72e-08
13	5.46e-08	1.04e-07	1.21e-07	1.22e-07	6.46e-08	7.41e-08	9.63e-08	6.32e-08	7.30e-08	9.69e-08	8.77e-08
14	6.85e-08	9.73e-08	1.37e-07	1.21e-07	7.01e-08	7.57e-08	1.01e-07	6.05e-08	7.33e-08	9.19e-08	7.50e-08
15	5.37e-08	1.02e-07	1.23e-07	1.12e-07	6.97e-08	7.42e-08	1.23e-07	6.60e-08	7.95e-08	1.00e-07	7.88e-08
16	5.26e-08	1.07e-07	1.48e-07	1.16e-07	6.24e-08	8.16e-08	1.03e-07	5.62e-08	8.13e-08	1.04e-07	8.84e-08

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