# NEAREST NEIGHBOUR INTERCONNECT ARCHITECTURE IN DEEP-SUBMICRON FPGAS

By

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Graduate Department of Electrical & Computer Engineering
University of Toronto

# *Nearest Neighbour Interconnect Architecture in Deep-Submicron FPGAs*

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*2002*

# Abstract

As FPGAs become mainstream system implementation vehicles, the desire to make their speed performance greater is stronger. In this work we seek to increase the speed of FPGAs by exploring the use of high speed *Nearest Neighbour (NN) interconnections*. Several commercial FPGA architectures provide these fast connections between adjacent logic blocks because they decrease the *best-case* delay between circuit elements with the goal of increasing overall performance. This work explores the architecture of these NN interconnects to determine topologies, quantities and distances that are good for performance and area. We develop an augmented architecture generation tool and CAD flow that enumerates and targets various portions of the NN architecture space. We show that certain architectures can achieve a 7.7% performance improvement at the cost of a 6.8% increase in total FPGA area when fully populated. We also show that a 6.4% improvement can be achieved for a more modest cost of 3.8% increase in area.

# Acknowledgements

I would like to thank my supervisor, Professor Jonathan Rose, for his guidance and instruction during my period of study. Through him I have learned much about the field of FPGA research and engineering in general.

I would also like to thank friends and fellow lab mates in LP392 and SF2202, Paul, Elias, Mike, Tomasz, Ahmed, Andy, William, Rob, Kostas, Ted, Peter, Sirish, Warren, Vincent, Marcus, Guy, Tor, Yadi, Anish, Mehrdad and Tooraj for providing an atmosphere that was both social and educational.

I also extend my gratitude to members of staff Jennifer Rodrigues and Eugenia Distefano for all your help in various tasks over the years.

I would also like to thank Dr. Vaughn Betz and Alexander Marquardt for providing the CAD framework that made this research possible.

Last, but certainly not least, I would like to thank my family. My parents, Kamala and Krishna Roopchansingh, and my brothers, Vinai and Yuva, who have always given me the support, guidance and encouragement I needed over the years.

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# *Chapter 1*

# Introduction

## 1.1 Motivation

FPGAs have become a multi-billion dollar industry that generates increasing demand for cheaper and faster devices. This motivates intensified research effort towards improving both the architecture of these devices and the CAD tools employed in their use. This research focuses on the architectural design of FPGAs and seeks to improve their performance.

The delay of a circuit implemented in an FPGA can be broken down into two major components: the routing delay and the logic delay. Previous studies have shown that depending on the architecture, anywhere from 60% to 80% of the circuit delay in an FPGA is due to the delay in the routing fabric [1][8][9]. As integrated circuit manufacturing process geometries shrink into the deep-submicron region, the resistance and capacitance of wires and switching elements in an FPGA become increasingly significant, creating routing delays that are an even greater proportion of the total delay. Thus, minimizing the routing delay through the development of new and faster routing architectures is an active area of research and provides the motivation for this work.

## 1.2 Goal

The goal of this research is to explore ways of decreasing FPGA circuit delay by focusing on a specific type of routing resource called a *Nearest Neighbour (NN) Interconnect*. NN interconnects are direct, fast connections between adjacent logic blocks as shown in Figure 1.1.

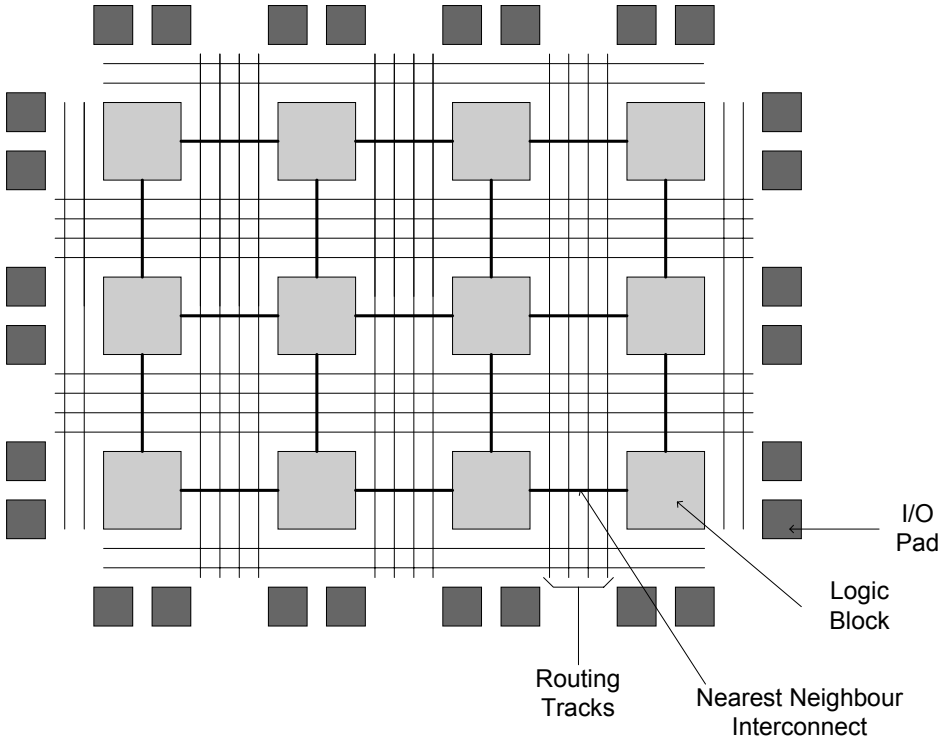


*Figure 1.1 - NN Interconnects in the FPGA Routing Architecture*

Although several commercial architectures [21-29] have employed NN interconnects, there are no published studies that investigate NN interconnect quantity or patterns and their speed and area tradeoffs. This work deals with three fundamental aspects of NN interconnect architectures. Firstly, we are interested in patterns which dictate which neighbouring logic blocks a given block can connect to. Secondly, we determine what distances the NN interconnects from a given block can extend to. For example, Figure 1.1 shows NN interconnects that connect only immediate neighbours however we wish to determine if there

is any merit to connecting to logic blocks further away. Finally we focus on exploring how many NN interconnects are required to achieve good area and delay results.

## 1.3 Dissertation Organization

This dissertation is organized as follows: Chapter 2 describes the FPGA framework that this research is based on. This includes the base architecture and CAD flow employed and brief descriptions of placement and routing algorithms. We also review previous NN interconnect architectures. Chapter 3 gives a detailed description of NN interconnect architectural parameters that we explore and their circuit design. Chapter 4 presents our experimental results and Chapter 5 gives conclusions and future work.

# *Chapter 2*

# Background

This chapter describes the basic FPGA architecture built upon in this work. This is followed by a description of the CAD flow used to evaluate new architectures and includes a brief description of the timing-driven placement and routing algorithms. It concludes with an overview of the NN interconnect architectures that exist in current commercial FPGAs.

## 2.1 Basic FPGA Architecture

This section briefly describes the basic FPGA architecture developed by Betz [1] and defines the terminology used in the architectural parameterization of this FPGA. This architecture forms the basis for the present work.

The basic FPGA architecture uses a symmetric "island-style" structure in which logic blocks are surrounded by routing channels, with I/O pads evenly distributed around the perimeter as illustrated in Figure 2.1.

Each logic block is made up of *N* basic logic elements (BLEs), fed by *I* inputs as illustrated in Figure 2.2. Each BLE consists of a *K*-input lookup table (LUT) and a register. A two-input multiplexer is used to provide either a registered or unregistered BLE output as shown in Figure 2.3. Each logic block is "*fully connected*", which means that all *I* inputs and *N* BLE outputs can connect to each of the *K* inputs on every LUT. This connectivity is implemented using multiplexer on each of the BLE inputs as shown in Figure 2.2.

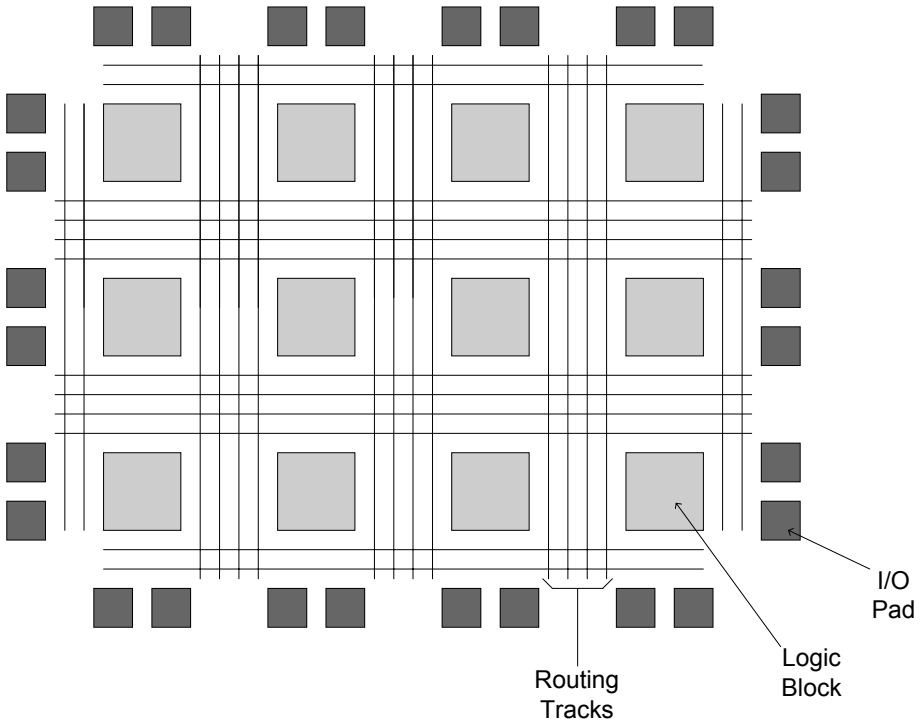


*Figure 2.1 - Island-Style FPGA*

The experiments conducted in this research use logic blocks with $N = 4$ BLEs, $I = 10$ inputs and $K = 4$-input LUTs. The 10 inputs are distributed evenly around the perimeter of the block with 3 inputs each on the bottom and left sides of the block and 2 inputs each on the top and right sides as shown in Figure 2.2. Each of the $I$ inputs can connect to 60% of the tracks in the channel adjacent to it (this is defined as the Input Connection Block Flexibility, Fc_input = 0.6) and each of the $N$ outputs connects to 25% of the tracks in the channel adjacent to them (this is defined as the Output Connection Block Flexibility, Fc_output = 0.25).

The routing channel uses metal wires that span four logic blocks, called segments of length four. Wires in the routing channel are connected together by two kinds of programmable switches: buffered switches (which is a buffer followed by a N-channel pass transistor gate) or by pass transistor switches (which are simple N-channel pass transistor gates). In the basic Betz architecture, buffered switches connect 50% of the wires in the routing channel while

the other 50% are connected by pass transistors switches. The routing channel switch block uses a "planar" topology, meaning that once a signal is routed on to track *i*, it cannot be switched onto any other track other than *i*. Finally, at a switch-block, each track can be switched onto 3 other tracks (which is called the Switch Block Flexibility, Fs = 3).

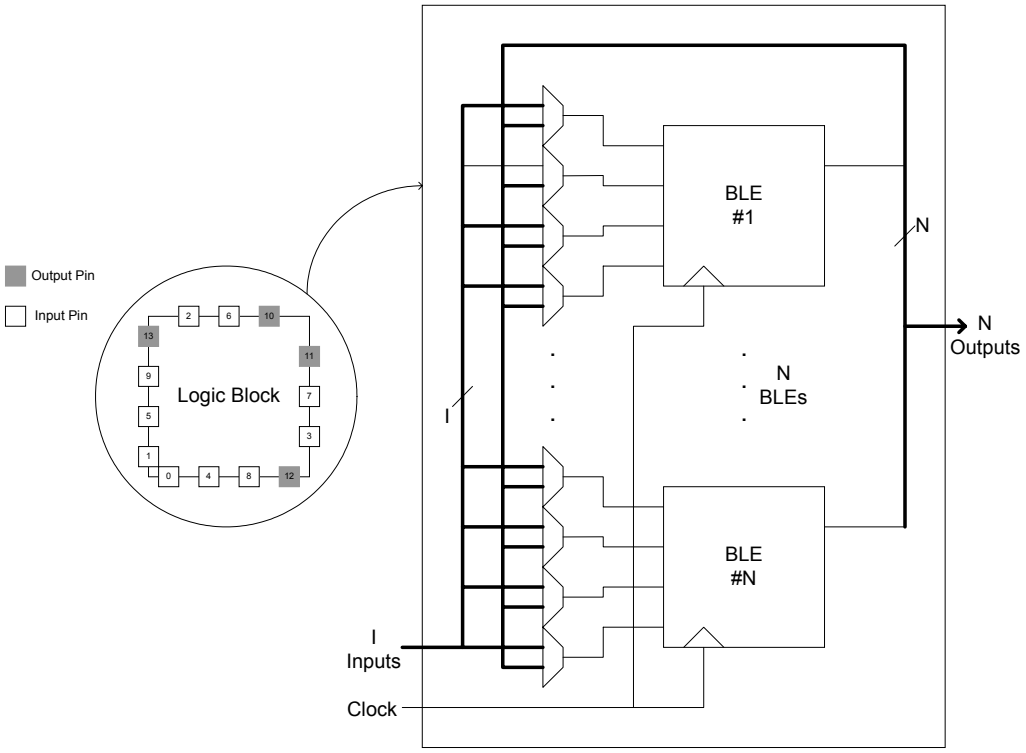


*Figure 2.2 - Logic Block and Pin Positions*

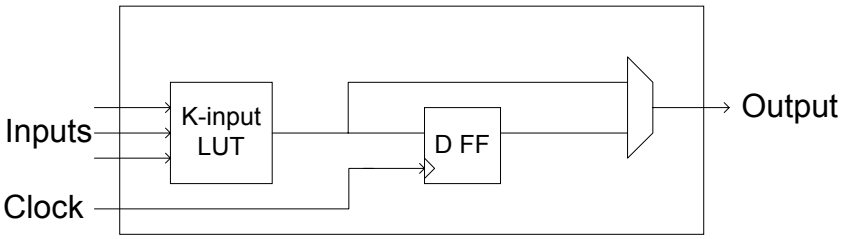


*Figure 2.3 - Basic Logic Element (BLE)*

The electrical and process level design of the FPGA is now described here. The initial work done on this architecture by Betz [1] was modelled in a 0.35µm design process. Subsequent

to this, Wilton, Ahmed and Sheng [31][7][9] remodelled the architecture for a 0.18μm process which was used in this research.

The metal routing tracks use minimum width wires and their spacing is set to double that of the minimum allowable for the process. Pass transistor switches are sized at 10 times the minimum size transistor allowed by the process while the size of the routing buffer is set to 5 times that of the minimum-size buffer [1].

## 2.2 CAD Flow

To evaluate new FPGA architectures, real circuits were synthesized, using a CAD flow, into the architecture and then the resulting area and delay was measured [1]. Experiments in this work used the 20 largest MCNC circuits [18] plus 8 new circuits created at the University of Toronto [32]. This benchmark suite of 28 circuits ranges in sizes from 800 BLEs to 10,000 BLEs. All circuits were put through the CAD flow depicted in Figure 2.4. They first undergo technology-independent logic optimization using SIS [15] and are then technology mapped into 4-input LUTs using Flowmap and Flowpack [16]. T-VPACK [1][5] is then used to pack LUTs and Registers into N = 4 clusters with I = 10 inputs. Versatile Place & Route (VPR) [1] is then used to do timing driven placement and timing driven routing of the circuits.

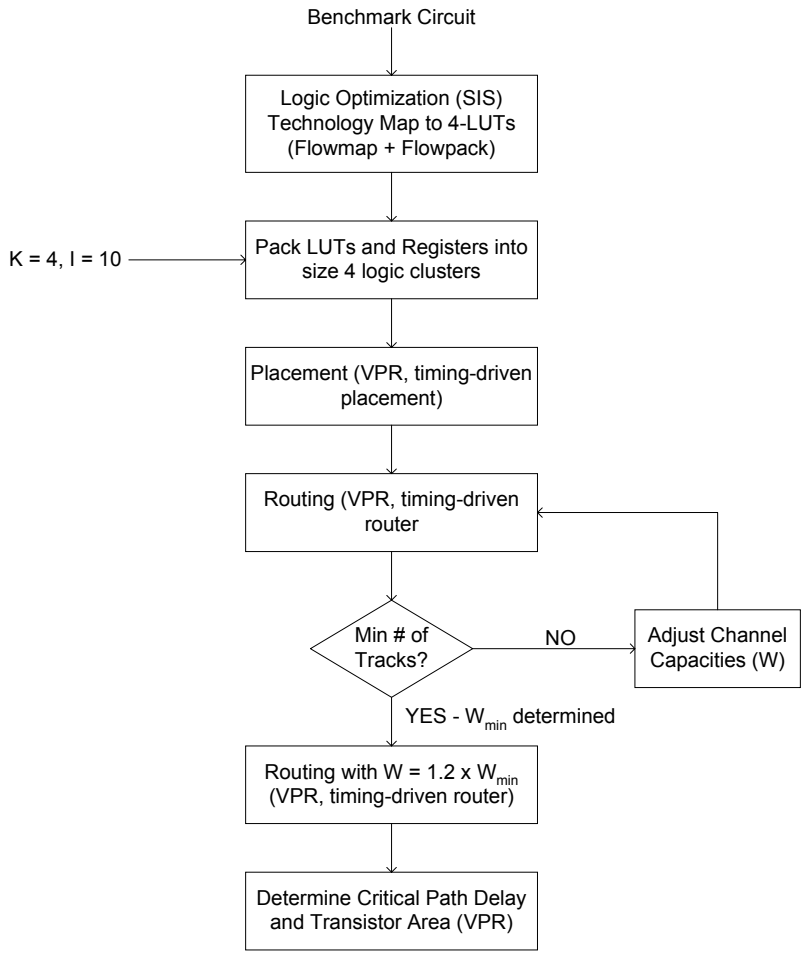


*Figure 2.4 - Architectural Evaluation Flow*

Note in this somewhat standard FPGA architectural exploration flow the track count in the FPGA is allowed to vary for each circuit. The flow illustrated in Figure 2.4 shows how to measure the minimum number of tracks per channel, $W_{min}$, required to just route the circuit. By allowing the track count to vary and measuring total area based on this track count, each circuit's wiring demand is measured. The alternative, simply determining routing success for a fixed channel width, provides much less information.

When the routing is performed at $W_{min}$ track width, it is referred to as a "*high-stress*" route [1] since at this track count the circuit is barely routable. Since most real circuits are not implemented under barely routable conditions, we measure the critical path delay under a

"*low-stress*" condition which is achieved by adding 20% more tracks than the minimum to the architecture. We believe this is legitimate because designers will attempt to avoid high-stress conditions by re-designing, partitioning their circuits or using larger devices.

### 2.2.1 Area Model

To accurately model FPGA area, a detailed circuit level design of all circuit elements (e.g. LUT, multiplexer, buffer, pass transistor, SRAM bit, etc) is required [1]. Each component is designed and properly sized at the transistor level, using SPICE, for reasonable area-delay trade-off [1] and is modelled in a TSMC 0.18µm CMOS process [30].

In order to measure area, the number of equivalent *minimum-width transistor areas* required to implement the FPGA is used as a metric [1]. This allows us to be somewhat process independent in determining area. The definition of a minimum width transistor area is the smallest possible layout area of a transistor that can be processed for a specific technology plus the minimum spacing surrounding the transistor as shown in Figure 2.5.

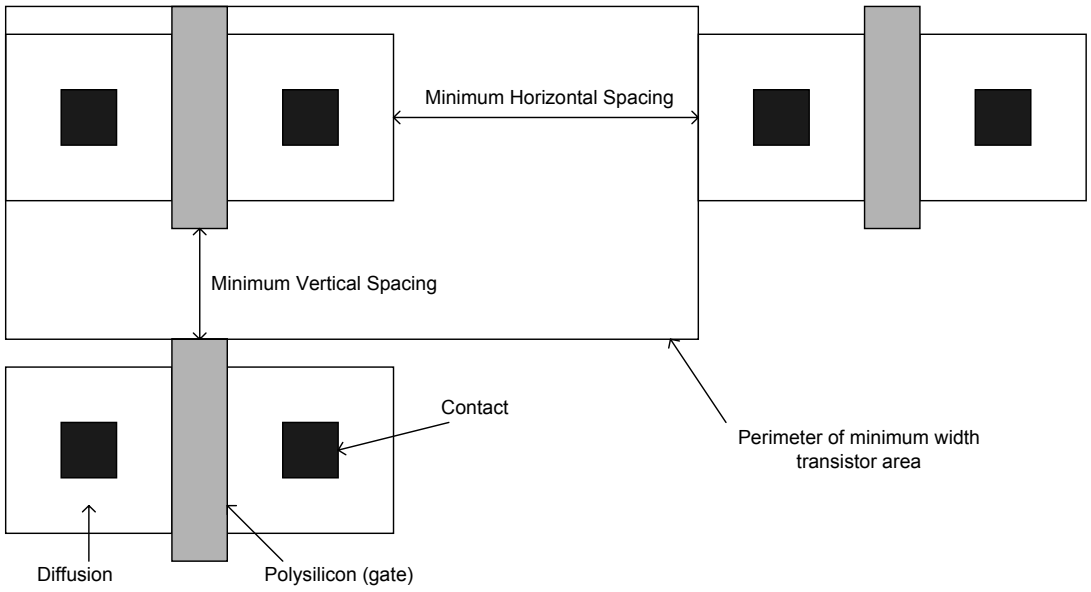


*Figure 2.5 - Definition of a Minimum-Width Transistor Area* [1]

Any transistors in the circuitry that are larger than the minimum are counted as a greater number of minimum-width transistors, taking into account the fact that a double size transistor takes less than twice the layout area.

Once the number of logic blocks and the minimum number of tracks required to route a circuit is known (recall that this was earlier defined as a *high-stress* route), the equivalent number of minimum width transistors needed to realize this architecture can then be determined. This metric does not take into account wire area; however communication with FPGA vendors indicates that most layouts are active-area limited [1].

It is also important to note that although each circuit is mapped to a square M x M grid, the total area counted is not the total grid area, but rather the area used by the exact number of logic blocks. Thus, a circuit that requires 390 logic blocks will be routed in a 20 x 20 grid which results in 400 blocks, however when counting area, only 390 blocks are counted as opposed to the 400.

### 2.2.2 Delay Model

Performance is measured under the low-stress conditions described above. All buffer delays, logic block delays, metal resistances and capacitances are designed and measured in 0.18μm CMOS technology [30].

## 2.3 Timing-Driven Routing

Since the design of an NN interconnect makes it faster than typical routing resources, it is important to have a router that will understand this difference and seek to take advantage of faster resources by routing the more critical nets on them. VPR contains such a timing-aware router [1].

VPR models the FPGA as a directed graph (which is called a *routing-resource graph*), where all logic block pins and routing wires are modelled as nodes and switches are modelled as directed edges. Resistance, capacitance and delay components are all annotated onto the nodes and edges of the graph. Thus, the routing problem becomes one of finding paths in the routing-resource graph between nodes which represent the logic block pins that are to be connected [1]. Figure 2.6 shows how a portion of an FPGA is mapped to a routing resource graph.

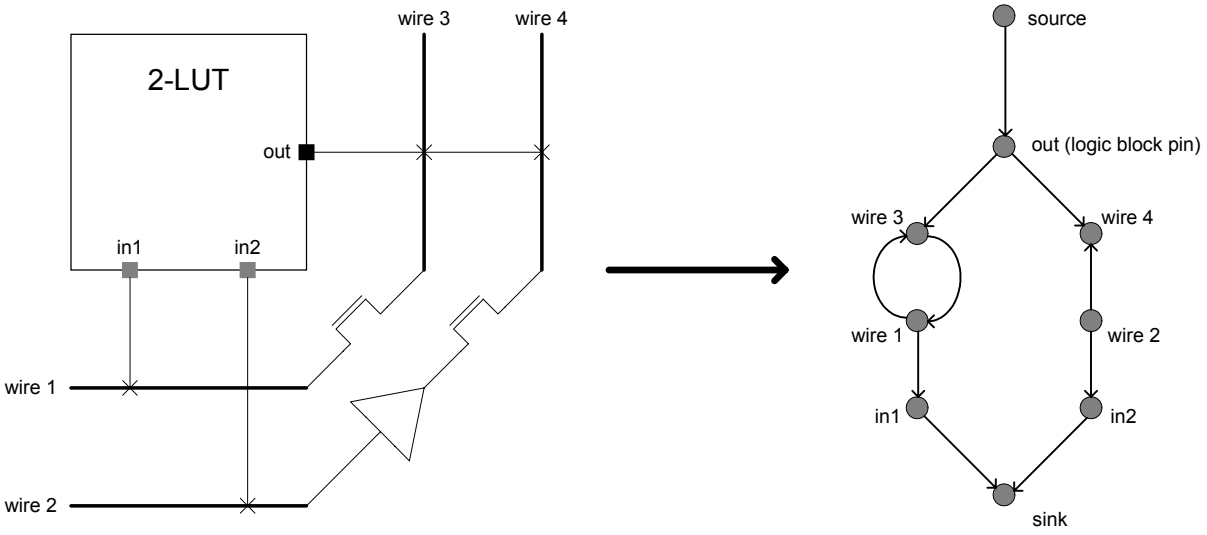


*Figure 2.6 – Modelling the FPGA Routing Architecture as a Directed Graph* [1]

VPR's routing algorithm is based on the Pathfinder negotiated congestion-delay algorithm [1][17]. This algorithm firstly routes all nets on the given FPGA and will give each net the fastest routing resource possible even if nets were previously routed on these resources. Thus, resources become overused and results in *congestion*. This overuse of resources is of course an initial illegal solution to the routing problem. However, this allows the router to extract timing information about each net and also gives the router an idea of the demand for a particular routing resource (the more nets sharing a resource, the greater its demand). With this information in mind, the router then repeatedly rips up and reroutes all nets and attempts to resolve the congestion while still paying attention to timing. Each attempt to route all nets,

legally or illegally, is known as a *routing iteration*. Several routing iterations are done in an attempt to remove all congestion by gradually resolving the competition for overused resources. Critical nets will favour faster resources and other non-critical nets will be routed onto resources that are not in high demand. The pseudo-code for this algorithm is given in Figure 2.7.

```
Let: RT(i) be the set of nodes, n, in the current routing of net(i).

Crit(i,j) = 1 for all nets i and sinks j;
while (overused resources exist) {     /* Illegal routing? */

        for (each net, i) {
                rip-up routing tree RT(i) and update affected p(n) values;
                RT(i) = NetSource(i);

                for (each sink, j, of net(i) in decreasing crit(i,j) order) {
                        Route net and add used nodes, n, to RT;
                        Update present congestion costs for all nodes (n);
                }
        }

        Update historical congestion costs for all n;
        Perform timing analysis and update Crit(i,j) for all nets i and sinks j;
}   /* End of one routing iteration */
```

*Figure 2.7 - Pseudo-code for the Pathfinder Algorithm [1]*

This algorithm uses a complex cost function to evaluate the *goodness* of a route. It takes into consideration both congestion and delay factors when routing a net. The cost of including a routing resource node n, in the routing of net i to one of its sinks, j, is given by:

$$\mathrm{Cost}(n) = \mathrm{Crit}(i,j) \cdot \mathrm{delay}_{\mathrm{Elmore}}(n) + [1 - \mathrm{Crit}(i,j)] \cdot b(n) \cdot h(n) \cdot p(n) \qquad (\mathbf{2.1})$$

The criticality of a connection crit(i,j) is a number between 0 and 1 which is a measure of how timing-critical that source-sink connection is. It is given by:

$$\mathrm{Crit}(i,j) = \max\left(\left[\mathrm{MaxCrit} - \frac{\mathrm{slack}(i,j)}{D_{max}}\right]^{\eta}, 0\right) \quad (\mathbf{2.2})$$

where $D_{max}$ is the circuit critical path delay and slack(i,j) is the slack of the connection between the source and sink j of net i (the slack of a connection is the amount of delay that can be added to the connection without increasing the critical path delay of the circuit. Thus a connection with a slack of 0 is *on* the critical path). $\eta$ and MaxCrit are parameters that control how connection's slack impacts the congestion-delay trade-off in the cost function in Equation 2.1. The first term in Equation 2.1 is the delay-sensitive term and the second term is the congestion-sensitive term. b(n) is the base cost of a node, h(n) is the historical congestion of a node (it is increased after every routing iteration in which the node n is overused and gives the router *congestion memory*) and p(n) is the present congestion of the node (in early iterations, p(n) increases slowly with overuse and then rapidly in later iterations) [1].

## 2.4 Timing-Driven Placement

As discussed above with the router, it is also important that the placement step in the CAD flow be aware of special resources such as the Nearest Neighbour interconnect. VPR utilizes a timing-driven placer which is based on the simulated annealing algorithm [20]. Simulated annealing mimics the annealing process used to gradually cool molten metal to produce strong, low energy metal objects [20]. VPR uses a variant of this algorithm which incorporates timing information into the process and thus tries to minimize the critical path delay during placement. The pseudo-code for this algorithm is given in Figure 2.8.

```
S = RandomPlacment();
T = InitialTemperature();
R_limit = InitialR_limit();
Criticality_Exponent = ComputeNewExponent();

ComputeDelayMatrix();

while (ExitCriterion() == False) {     /* Outer Loop */

        TimingAnalyze();       /* Perform a timing analysis and update each net's
                                  criticality */
        Previous_Cost_linear congestion = Cost_linear congestion(S) /* wirelength minimization
                                                                       normalization term */
        Previous_Timing_Cost = Timing_Cost(S)    /* delay minimization normalization
                                                    term */

        while (InnerLoopCriterion() == False) {      /* Inner Loop */

                S_new = GenerateViaMove(S, R_limit);
                ΔTiming_Cost = Timing_Cost(S_new) - Timing_Cost(S);
                ΔCost_linear congestion = Cost_linear congestion(S_new) - Cost_linear congestion(S);
                ΔC = λ·(ΔTiming_Cost / Prev_Timing_Cost) +
                                (1 - λ)·(Δ Cost_linear congestion / Previous_ Cost_linear congestion);
                if (ΔC < 0) {
                        S = S_new;        /* Move is good, accept */
                }
                else {
                        r = random (0,1);
                        if (r < e^(-ΔC/T)) {
                                S = S_new;        /* Move is bad, accept anyway */
                        }
                }
        }       /* End Inner Loop */

        T = UpdateTemp();
        R_limit = UpdateR_limit();
        Criticality_Exponent = ComputeNewExponent();

}       /* End Outer Loop */
```

*Figure 2.8 - Timing-Driven Simulated-Annealing-Based Placement Algorithm [4]*

In order to do timing driven placement, the placement tool needs precise delay information about the distance between various paths in the FPGA. This is done in the step *ComputeDelayMatrix* in Figure 2.8. Since all (x, y) locations in a tile-based FPGA are constructed from identical tiles, delay between two logic block can be computed as a function only of the distance ($\Delta x$, $\Delta y$) between them [3][4]. VPR uses its router to determine exact, best-case delays for blocks that are $\Delta x$, $\Delta y$ apart and stores these values in a *delay lookup matrix* for easy access. Thus when evaluating how a particular move made during the annealing process affects the overall circuit delay, the estimated delay for all affected nets can quickly determined.

Recording the delay between all $\Delta x$ and $\Delta y$ positions in the FPGA in this manner makes the placer aware of the speeds of the various connections that will be available to the router. This algorithm has the goal of minimizing wire-length and reducing critical path delay, thus nets that are critical tend to be placed closer together to minimize delay.

Having new faster nearest neighbour connections will tend to increase this clustering effect as the placer will now realize that it is more attractive from a delay perspective to place blocks in certain positions that were otherwise not so attractive. Timing driven placement will be shown to have a significant effect on the performance benefits of using NN interconnects.

## 2.5 Previous NN Interconnect Architectures

This section discusses the several commercial FPGAs that employ NN interconnects in their routing fabric. The concept existed as far back as 1984 when they were used in the Xilinx 2000 series of FPGAs and was later employed in 1987 in the Xilinx 3000 FPGAs and in 1989 in the Algotronix CAL1024 FPGA. They are still used today in the more recent Atmel AT40K and Xilinx Virtex series of FPGAs. The following discussion contains brief descriptions of the NN interconnect architectures present in these and other past and present FPGAs.

### 2.5.1 Algotronix CAL1024 [21]

The Algotronix CAL1024 routing array consisted entirely of NN interconnects, save for a few global lines which were used to route clock signals. Logic blocks could *only* connect to neighbouring blocks that were North, South, East and West of them. Figure 2.9 shows the basic setup.

Each block has 4 neighbour inputs from other blocks and 4 neighbour outputs. Each output has its own multiplexer that selects either the function unit output or the other neighbour inputs (thus allowing the logic block to be used as a route-through). The obvious drawback of this architecture is that long nets had to be routed through a chain of neighbouring logic blocks which results in poor circuit delay.

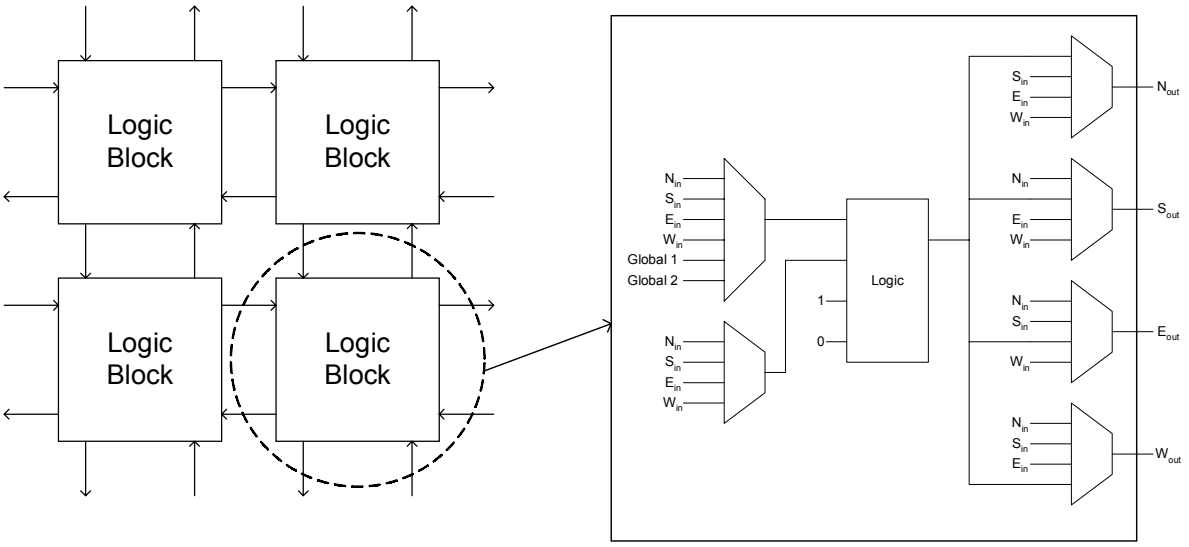


*Figure 2.9 – Algotronix CAL1024 Array Structure*

Xilinx subsequently acquired Algotronix and the CAL1024 evolved into the Xilinx 6200 [27] series of FPGAs. The Xilinx 6200 routing architecture can be viewed as a hierarchy. At the lowest level of this hierarchy is a 4 x 4 array of simple logic blocks that are connected via

Nearest Neighbour interconnects only. The scheme used is very similar to the CAL1024 routing scheme. The logic blocks are however able to accept inputs from higher-level routing resources as well which enable them to connect to blocks long distances away without having to pass through a chain of neighbouring blocks.

This NN interconnect scheme, is best classified under our nomenclature as a Manhattan Radius 1 architecture with four NN interconnects. Refer to Section 3.2 for a definition of this terminology.

### 2.5.2 Xilinx 3000 [26]

The Xilinx 3000 routing fabric consisted of 3 types of programmable interconnect:

1. General Purpose Interconnect
2. Longlines
3. Direct Connections (Nearest Neighbour Interconnects)

Each Xilinx 3000 logic block has 5 logic inputs (A to E) and 2 outputs (X and Y). For each block, the X output can connect to the B input of the Block to the immediate right or the C input of the block to the immediate left. The Y output can be directly connected to the D input of the block on the immediate top and the A input of the block on the immediate bottom. This connectivity is shown in Figure 2.10.

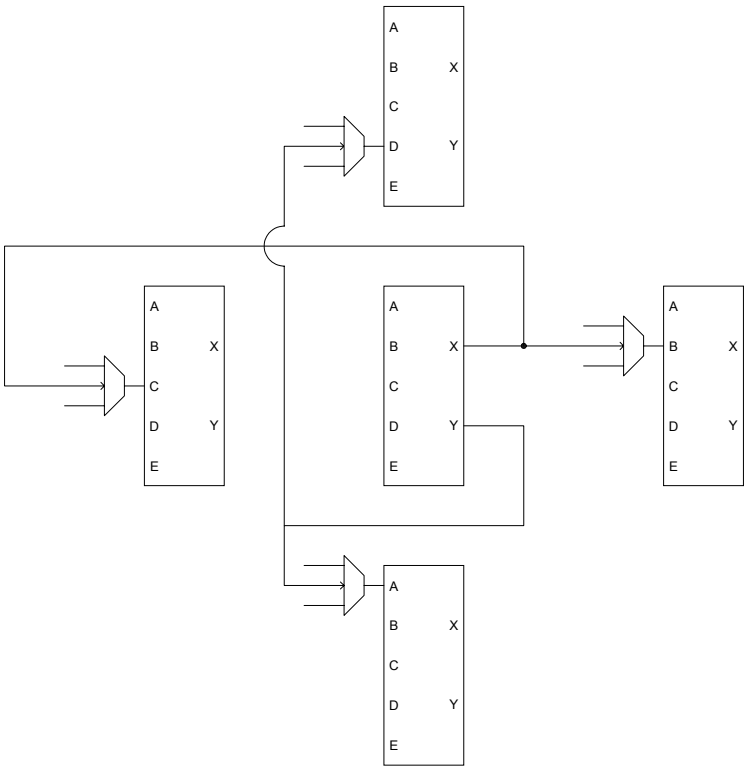


*Figure 2.10 - Xilinx 3000 Nearest Neighbour Connectivity*

This is also best classified, using the nomenclature of Section 3.2 as a Manhattan Radius 1 architecture with four NN interconnects.

### 2.5.3 Atmel AT6000 [25]

The Atmel AT6000 uses both Nearest Neighbour interconnects and general purpose routing wires in its routing fabric. Each logic block has 8 neighbour inputs and 2 outputs A and B, each of which fans out to the north, south, east and west directions. This connectivity is illustrated in Figure 2.11.

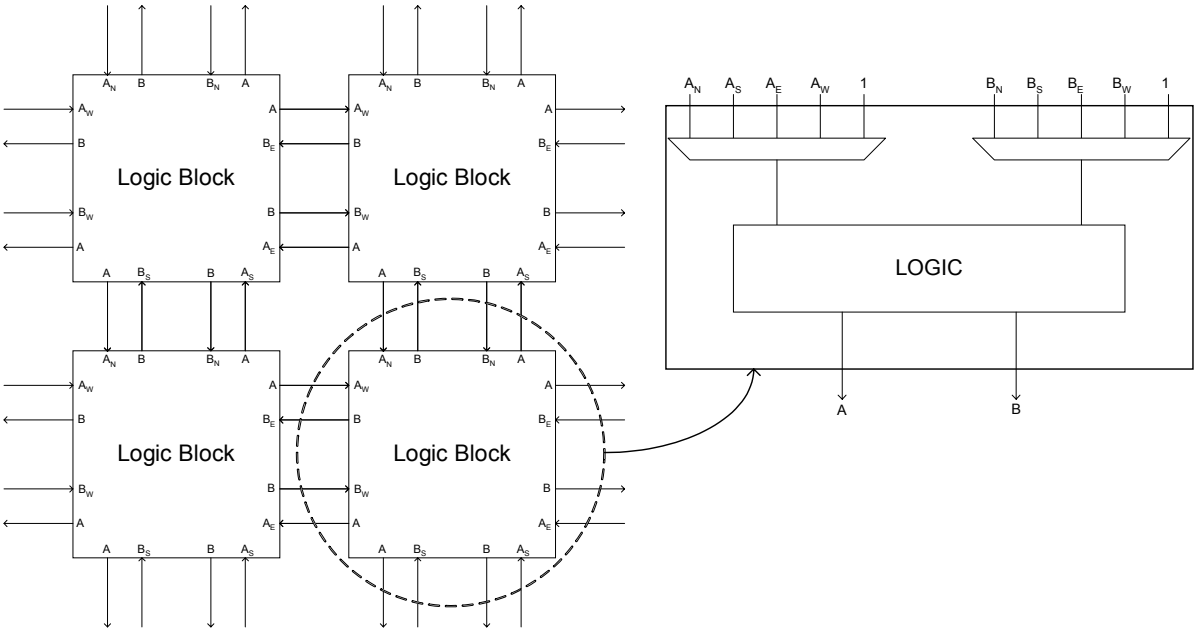


*Figure 2.11 – Atmel AT6000 Nearest Neighbour Connectivity*

This is best captured in our terminology (which is defined in Section 3.2) as a Manhattan Radius 1 architecture with 8 NN interconnects.

### 2.5.4 Xilinx Virtex, Virtex-E [28] and Virtex II [29]

The Xilinx Virtex and Virtex-E FPGAs both have a similar NN interconnect setup. Each Virtex logic block has 4 outputs. The outputs are fed into an output connection switch box. From here two NN interconnects go to the input switch box of the logic block on the immediate left, and another two go to the input switch box of the block on the right. Any of the four outputs can be switched onto any of the four NN interconnects. Figure 2.12 shows this setup.

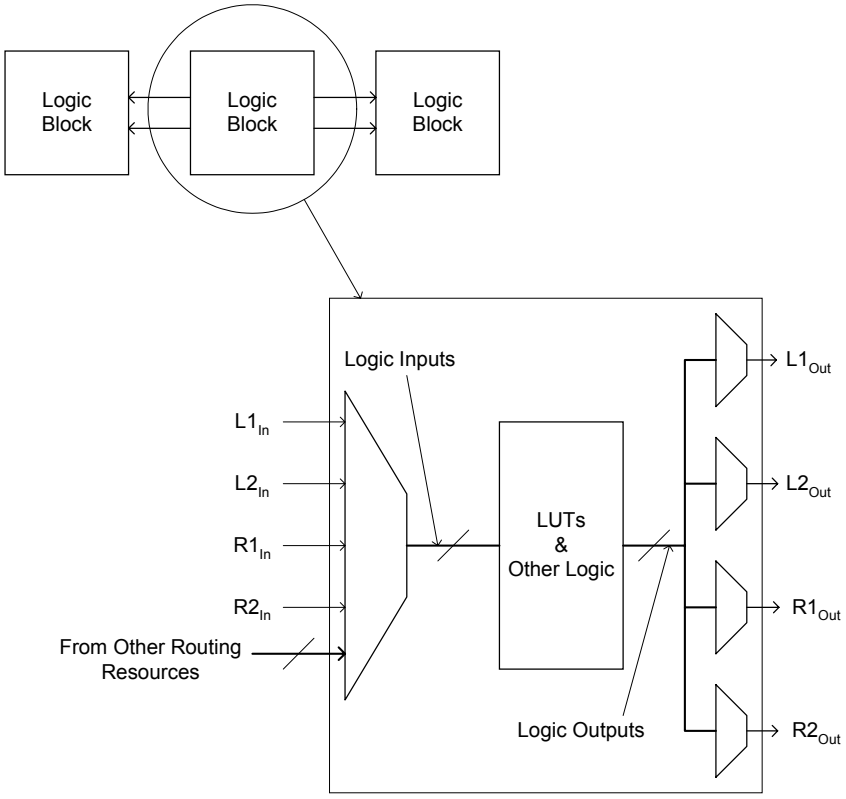


*Figure 2.12 - Xilinx Virtex and Virtex-E NN Interconnect Setup*

This NN interconnect architecture is not characterized under our terminology.

Subsequently, Xilinx introduced the Virtex II series of FPGAs which has 16 NN interconnects that go to all 8 surrounding neighbours. The NN interconnect setup is highly flexible as all logic outputs can be connected onto any of the 16 NN interconnects and incoming NNs can be connected to many (but not all) of the inputs of the internal BLEs. Figure 2.13 shows the NN interconnect setup for the Virtex II.

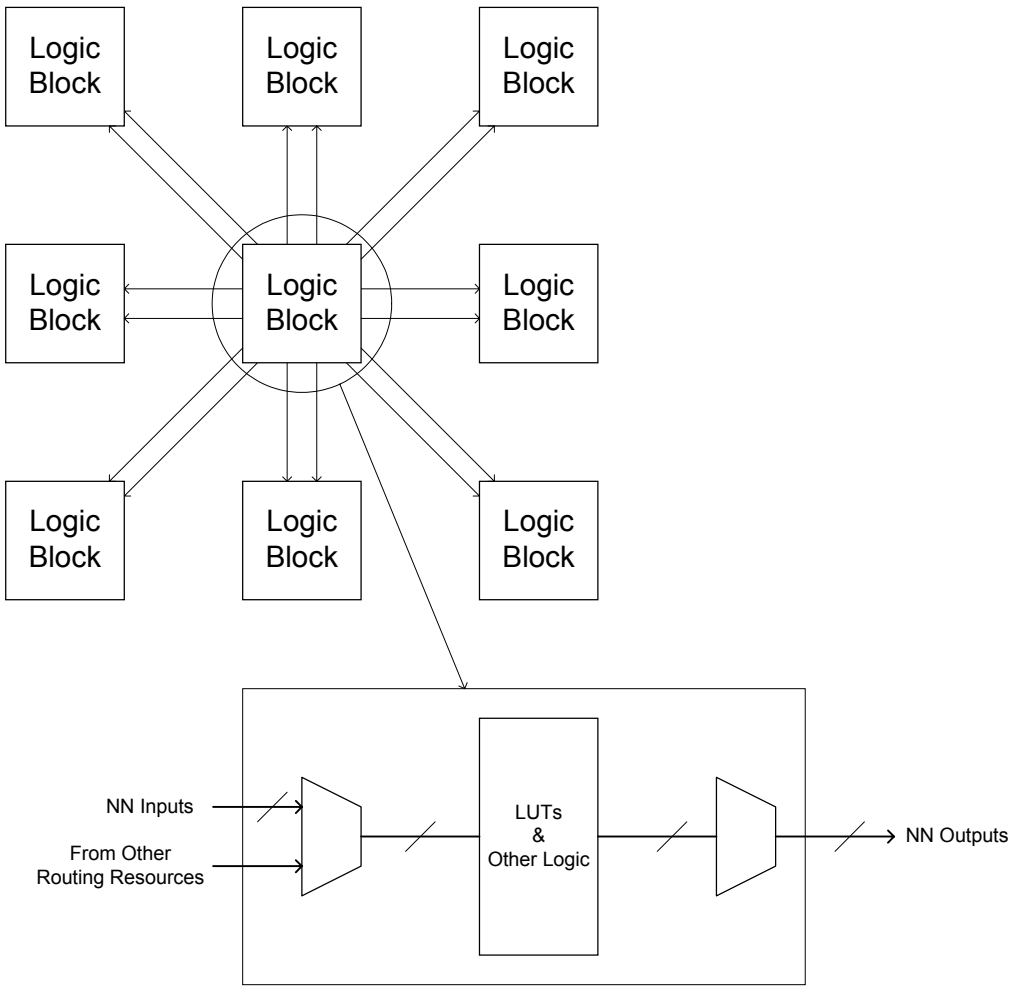


*Figure 2.13 – Xilinx Virtex II NN Interconnectivity*

This NN architecture is classified under our NN architectures as a Full Radius 1 architecture with 16 NN interconnects.

### 2.5.5 Altera Flex 6000 [23] and Apex 20K [22]

These FPGAs have a Nearest Neighbour connectivity very similar to that of the Xilinx Virtex and Virtex-E FPGAs, in that they connect only to the logic blocks to the left and to the right of them. The logic blocks in the 6000 and 20K each have 10 outputs. These 10 outputs can

be connected to any of the inputs on the logic blocks on the immediate left or right. Figure 2.14 shows this NN connectivity.

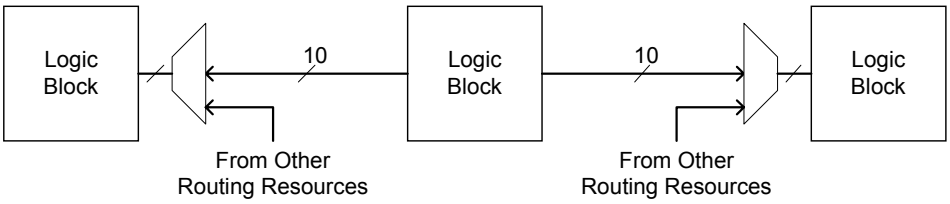


*Figure 2.14 – Altera Flex 6000 & Apex 20K NN Interconnectivity*

As with the Virtex and Virtex-E FPGAs, no proper characterization exists under our nomenclature to describe this topology.

### 2.5.6 Atmel AT40K [24]

The AT40K has NN interconnects to all of its 8 surrounding neighbours. Each logic block has two outputs, X and Y. The Y output goes to the North, South, East and West neighbours while the X output fans out to the NE, SE, NW and SW neighbours. Figure 2.15 illustrates this connectivity.

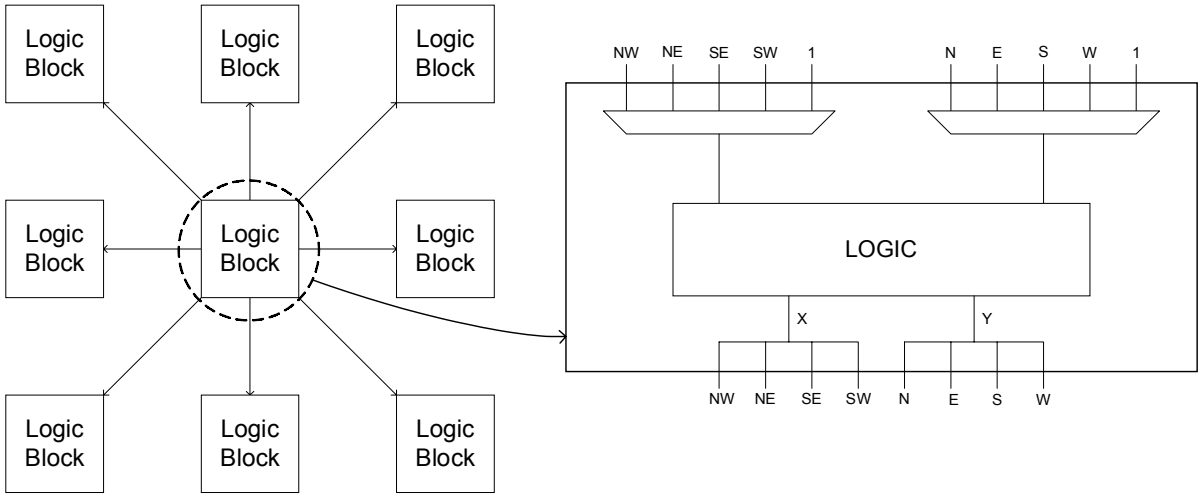


*Figure 2.15 – Atmel AT40K Nearest Neighbour Connectivity*

This is best classified under our nomenclature as a Full Radius 1 architecture with 8 NN interconnects. Refer to Section 3.2 for a definition of this terminology.

# *Chapter 3*

# Nearest Neighbour Interconnect Design, Architecture & Experimental Methodology

This chapter defines the Nearest Neighbour interconnect architecture that will be explored, and provides the circuit design required in this domain. It also describes modifications to the basic experimental methodology presented in Chapter 2 needed to explore this space. Section 3.1 deals with the detailed level circuit design. Section 3.2 then describes the architectural space to be explored and Section 3.3 gives the methodology.

## 3.1 Circuit Design

As mentioned in Chapter 1, Nearest Neighbour interconnects are short fast connections that exist between adjacent logic blocks. NN interconnects form a connection from the BLE output to the input multiplexer on adjacent blocks, bypassing the general routing resources. Figure 3.1 shows the detailed circuit modelling of an NN interconnect.

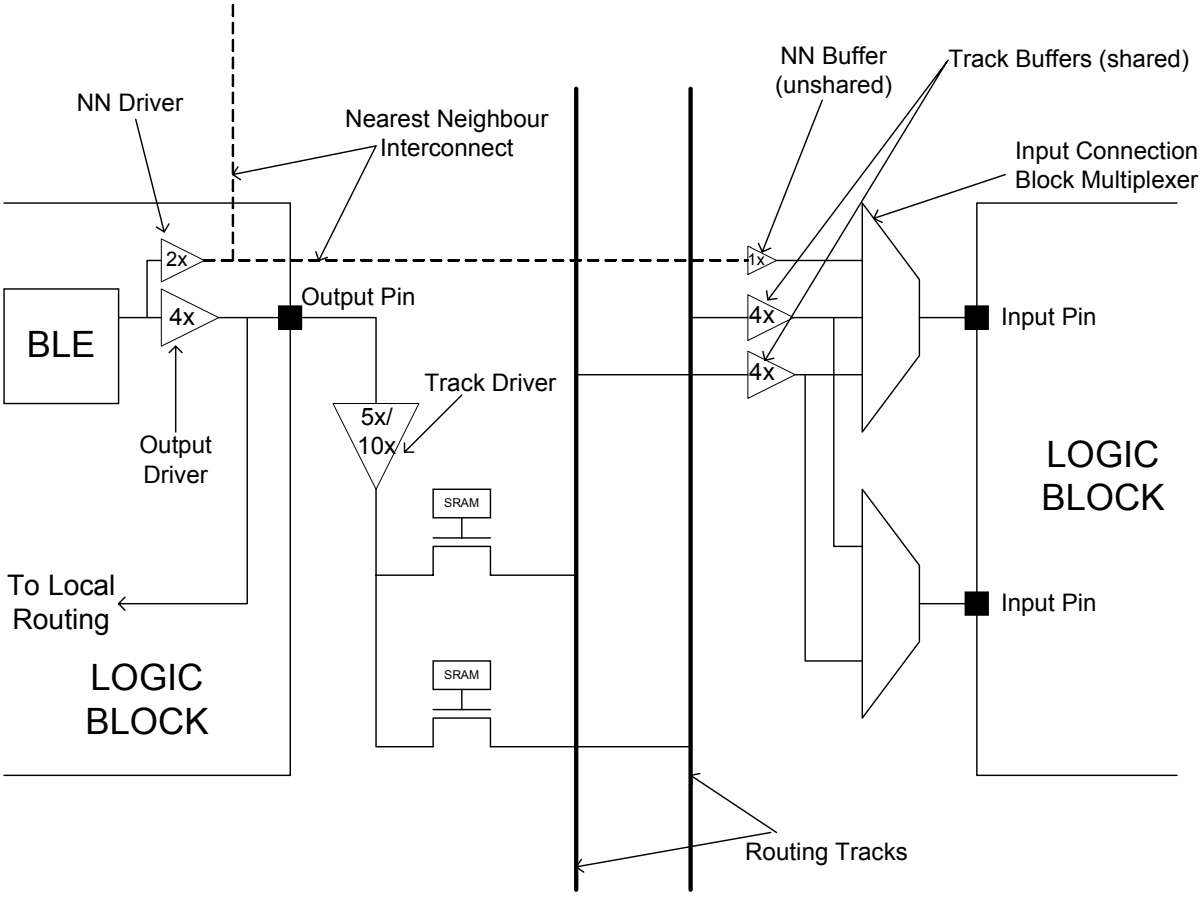


*Figure 3.1 – Circuit Design of a Nearest Neighbour Interconnect*

Nets connected through NN interconnects are faster for three major reasons:

i. The NN driver is smaller (and therefore faster) than the output driver. The output driver is sized as a 4x buffer since it must also drive the internal feedback to the logic block which consists of 16 LUT inputs (recall each block consists of four 4-input LUTs). This has been shown to produce good area and delay results [1]. In the NN architectures explored in this work, the maximum fanout of an NN interconnect is 8, and this is only in the case of large, fully populated architectures (as discussed later in Section 3.2), thus it is safe to make the NN driver half the size of the output driver. Note also, since NN interconnects travel only a short distance, a track driver is not needed. These two factors account for the majority

of the delay advantage of using an NN interconnect rather than a conventional routing track to route signals between adjacent logic blocks.

ii. The conventional routing wires have many routing switches connected to them and are thus more heavily loaded than the NN interconnect wires which experience almost no loading at all.

iii. Track and NN buffers must be used to isolate the wires from the high capacitive load of the input multiplexer which is implemented as a pass transistor tree. The track buffer must fan out to all input multiplexers to which that track connects, which can be up to four in the base architecture. The NN Buffer however, is a dedicated buffer and thus can be made smaller and is sized at one quarter the size of the track buffer.

VPR uses accurate resistance, capacitance and delay values modelled in HSpice to determine path delay of various connections. Table 3.1 shows how NN interconnect delay was improved through buffer resizing. The first line shows the NN interconnect delay if no resizing was done. The second line shows how the delay improves upon resizing the NN driver from a 4x to a 2x driver, while the third line shows how resizing the NN buffer from a 4x to a 1x buffer further improved NN interconnect speed. Refer to Table A.28 in Appendix A for information on the propagation delay through various sized buffers as measured by HSpice using 0.18µm CMOS technology.

| | **Path Delay to Immediate Neighbour (ps)** |
|---|---|
| No Buffer resizing | 377 |
| Resized NN Driver | 354 |
| Resized NN Driver and NN Buffer | 297 |

*Table 3.1 – Effect of Buffer Resizing on NN Interconnect Delay*

Experiments were also ran to compare the speed of an NN interconnect to that of conventional routing resources. Figure 3.2 illustrates the various paths that were tested.

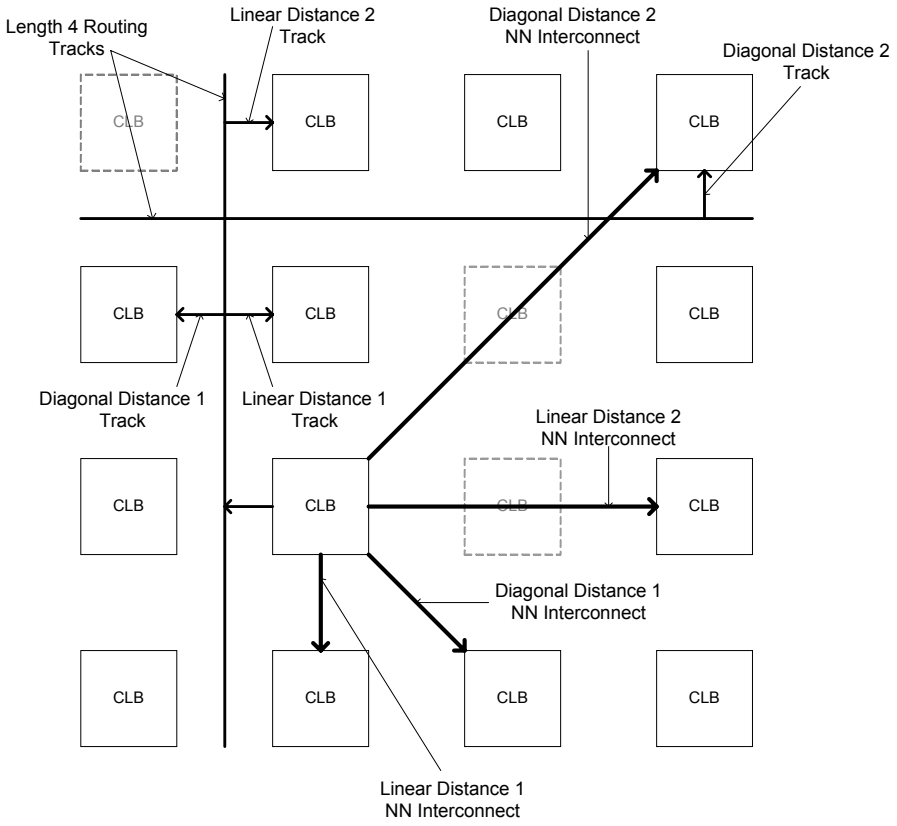


*Figure 3.2 – Conventional Routing Paths vs NN Interconnect Paths*

Table 3.2 shows the best-case path delay between logic blocks for the paths illustrated in Figure 3.2, using a conventional routing track and an NN interconnect. The fourth column shows the Conventional delay to NN delay ratio which tells us how much faster an NN interconnect is over a conventional routing track.

| **Path** | **Delay Using Conventional Routing (ps)** | **NN Interconnect Delay (ps)** | **Conventional/NN Ratio** |
|---|---|---|---|
| Linear Distance 1 | 676 | 297 | 2.3 |
| Linear Distance 2 | 676 | 299 | 2.3 |
| Diagonal Distance 1 | 676 | 299 | 2.3 |
| Diagonal Distance 2 | 897 | 303 | 3.0 |

*Table 3.2 - Delay of Conventional Routing vs NN Interconnect*

Note that the first 3 lines of the table have the same delay for the conventional routing case since, in the best case, only one track is required to get to any of these positions. However, routing a signal to the diagonal distance 2 needs at least two tracks, resulting in a much longer path delay. It can be seen that the NN interconnect ranges from 2.3 to 3 times as fast as a conventional routing track.

## 3.2 Architectural Parameters

This section parameterizes the Nearest Neighbour interconnect architectural space and defines the variables explored in the experiments conducted in this work. This is followed by a discussion that shows precisely how architectures are populated with NN interconnects.

### 3.2.1 Parameterization of NN Interconnect Architecture

Three parameters are used to define the NN Interconnect architecture:

1. Topology
2. Distance/Radius
3. Quantity

NN *Topology* describes the general fan-out pattern of NN interconnects, defining which neighbouring blocks a given block can connect to. Three basic topologies exist and are defined as follows:

i. *Manhattan* – A block has NN interconnects connecting it to the neighbours that are North, South, East and West of it.
ii. *Cross* – A block has NN interconnects connecting it to the neighbours that are NE, NW, SE and SW of it.

iii. *Full* – A block has NN interconnects connecting it to all 8 surrounding neighbours, which is a combination of both the Manhattan and Cross topologies.

Figure 3.3 illustrates these NN interconnect topologies.

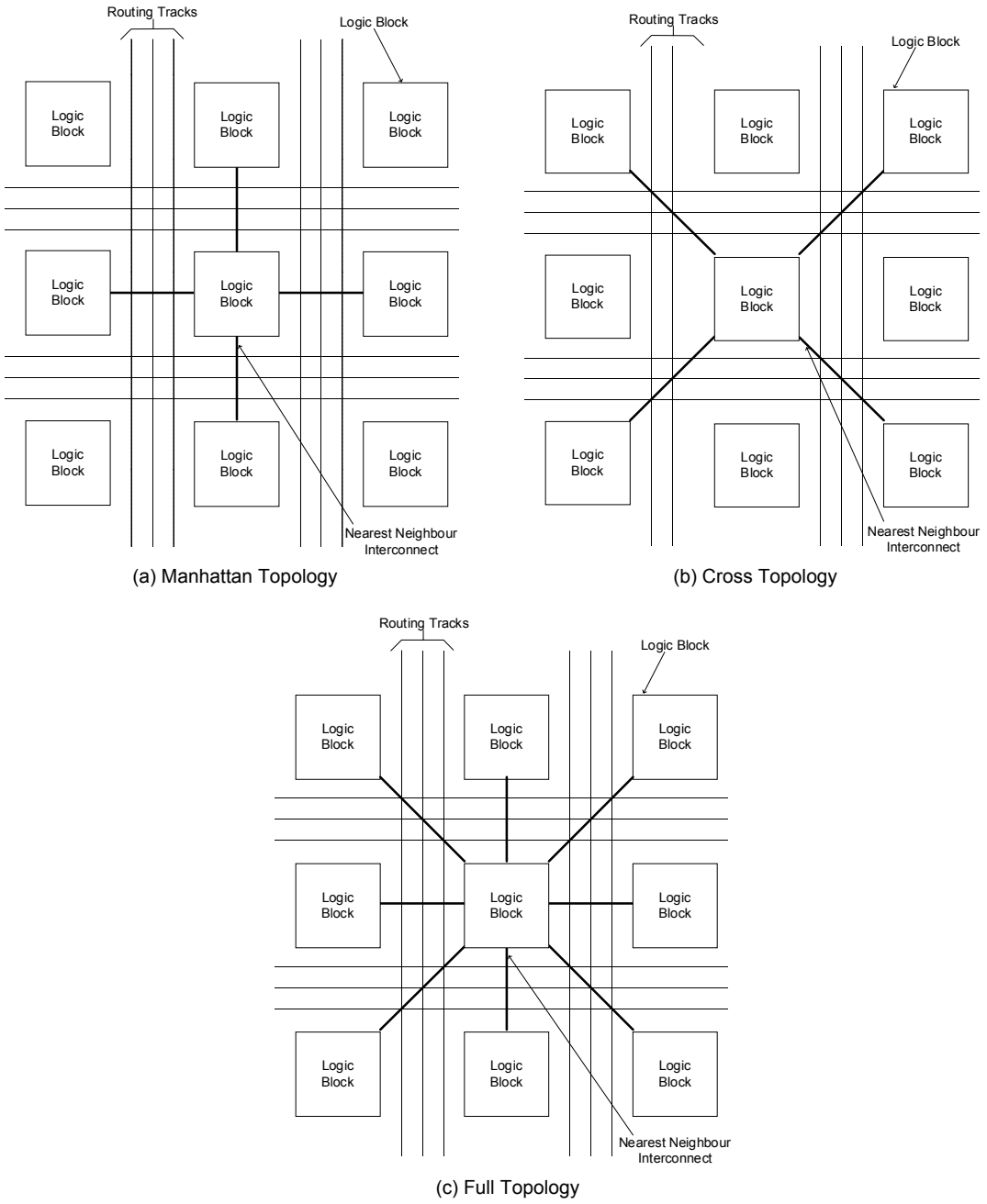


*Figure 3.3 – Manhattan, Cross & Full Topology*

The *Distance* or *Radius* defines the distance of the neighbouring logic blocks to which NN interconnects from a given block can extend to. NN interconnects that go to the immediate neighbours are considered Radius 1. Note that in a Cross or Full topology, the immediate diagonal neighbours are defined as Radius 1, even though the Manhattan distance is 2 (one horizontal plus one vertical logic block away). Figure 3.4 illustrates NN interconnects at various radii.

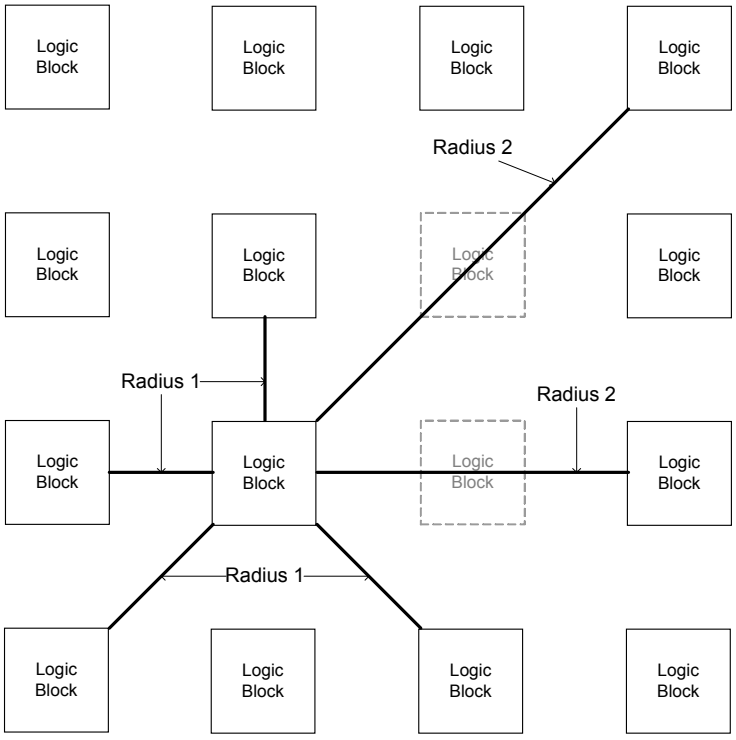


*Figure 3.4 – NN Interconnect at Various Radii*

Finally, the *quantity* of NN interconnects that exist in a specific topology at a given radius must also be defined. Note that each topology, at a given radius, will have a limit to the number of NN interconnects that can be present. Thus, when the architecture contains the maximum number of NN interconnects allowed for that topology at that radius, it is termed *fully populated*. For example, since the base architecture has only four output pins per logic block, a Manhattan Radius 1 topology can have at most 16 NN interconnects (4 outputs each fanning out in 4 directions). Figure 3.5 illustrates a fully populated Manhattan Radius 1

topology (the number labelled on each NN interconnect in Figure 3.5 shows which logic block that NN interconnect goes to). Note also that the Manhattan and Cross topologies will have the same maximum number of NN interconnects for each radius, 16. In a Full Radius 1 topology however, there are 4 outputs each fanning out in 8 directions for a total of 32 possible NN interconnects. In Radius 2 of a Full topology, there are 4 outputs each fanning out in 16 directions = 64 possible NN interconnects. Thus, in a Full Radius 1 and 2 architecture, there are 64 + 32 = 96 possible NN interconnects.

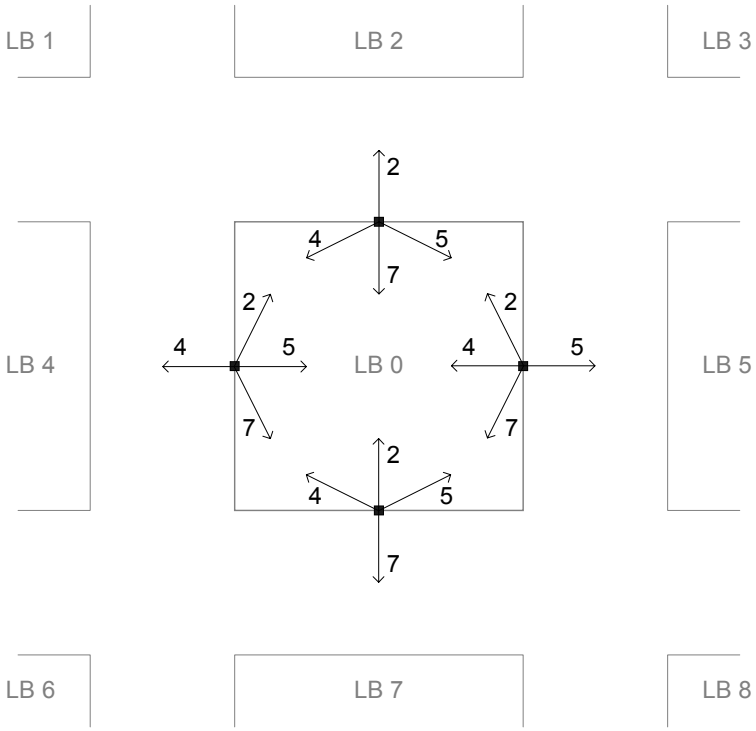


*Figure 3.5 – A Fully Populated Manhattan Radius 1 Architecture*

These 3 parameters, *Topology*, *Radius* and *Quantity* define the architectural space explored in this research.

### 3.2.2 Populating The NN Interconnect Architecture

The experiments conducted in this research evaluate the "*goodness*" of an NN architecture by choosing a particular topology and radius (or radii) for the architecture, varying the quantity of NN interconnects present and then measuring the effect on area and delay. For the purposes of this exploration (in which we wish to determine both good topologies and quantities of interconnects), the order in which NN interconnects are added to the architecture needs to be done in a sensible manner. For example, consider the fully populated scenario depicted in Figure 3.5 where the number of NN interconnects is at its maximum of 16 for that architecture. However it is not immediately clear exactly how this connection pattern will look if we wished to employ only a total of eight NN interconnects, or any other partially depopulated quantity. This section will describe the order in which NN interconnects are inserted into the architecture giving the reader a clearer view of exactly how the architecture was populated between NN = 1 to NN = 16. The two major issues to consider are:

1. Distributing NN interconnects intelligently among output pins
2. Hooking up NN interconnects intelligently among input pins

#### 3.2.2a NN Interconnect Distribution Among Output Pins

NN interconnects need to be connected between the output pin of a logic block and the input pin of a neighbouring logic block. Recall from Section 2.1 that logic blocks have four output pins. Thus, an efficient method of distributing NN interconnects evenly among the output pins is required. This is best explained using the example of Figure 3.5.

One possibility is that the first 4 NN interconnects be added to the first output pin, then the second 4 added to the second output pin and so on as shown in Figure 3.6a. In this figure, the number attached to the NN interconnect in this diagram indicates the *order* in which it was added to the architecture and has nothing to do with the logic block it was directed to as

in Figure 3.5. An alternative arrangement is that the first four be assigned to each of the four outputs, then the second four added as fan-out to each output as depicted in Figure 3.6b.

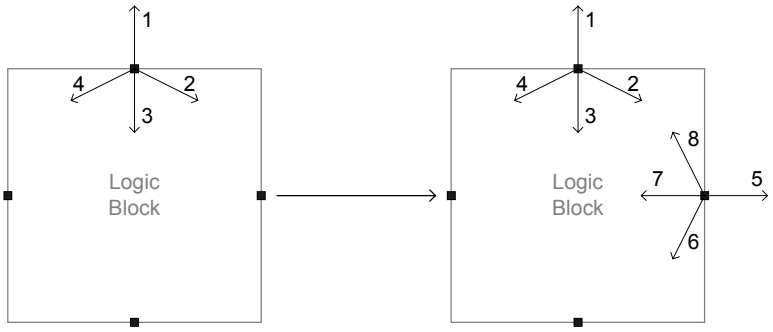


*Figure 3.6(a) – Output Fan-out Scenario 1*

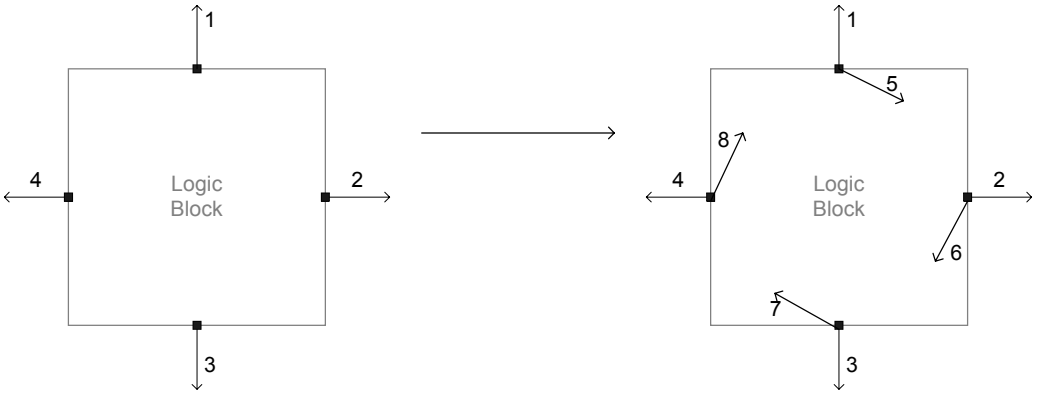


*Figure 3.6(b) – Output Fan-out Scenario 2 (Cyclic Pattern)*

Note that each scenario leads to the same final pattern depicted in Figure 3.5, however the manner of population will greatly affect the intermediate results. It is clear that the population scheme depicted in Figure 3.6b offers greater flexibility by allowing more nets to initially have access to NN interconnects. In Figure 3.6a, if the net that grabs the output pin does not fan out, then the 3 other NN interconnects attached to that output will be unused and wasted.

A second issue in the ordering question would be to determine if there is any benefit to adding fan out in certain directions first before adding them in others. For example, Figure

3.6b shows fan out being added in a cyclic order (thus we call this a *cyclic fan out pattern*), however fan out can be added differently as illustrated in Figure 3.7 (we call this a *180 degree fan out pattern*).

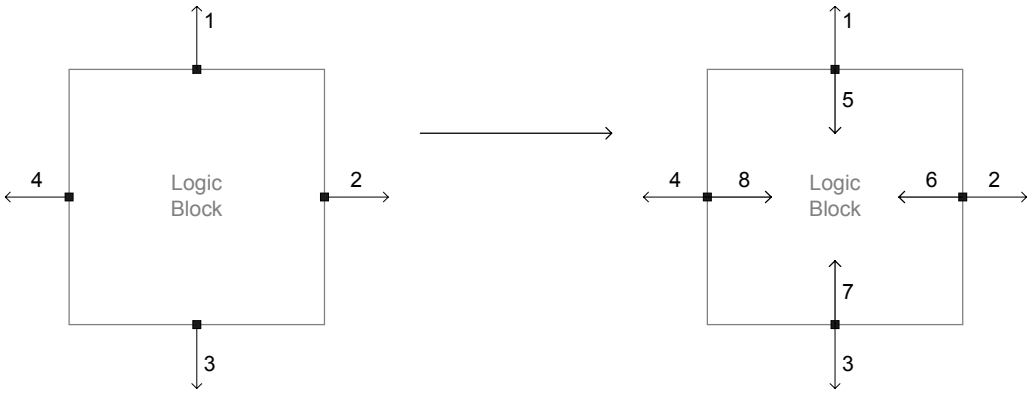


*Figure 3.7 – Output Fan-out Scenario 3 (180 Degree Pattern)*

Figure 3.8 shows how the average critical path delay (across 28 circuits) varies for both output schemes as the number of NN interconnects in a small Manhattan Radius 1 architecture is varied from 0 to the maximum of 16.

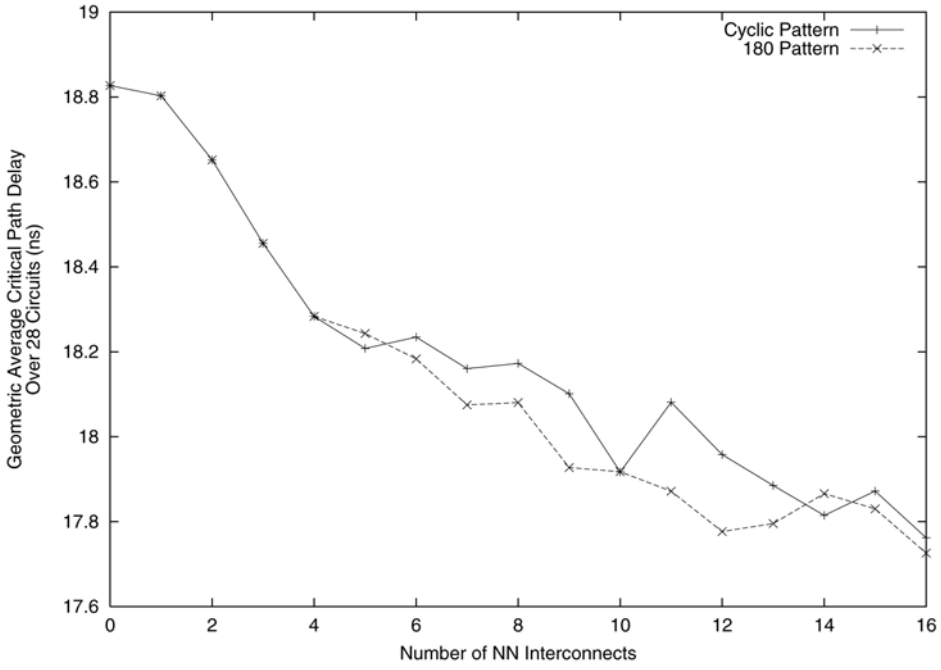


*Figure 3.8 - Delay vs. # of NN interconnects for*

*Two Output Schemes Using a Manhattan Radius 1 Architecture*

It is clear from this graph that there is marginal difference in the performance results of both schemes. The data for this graph can be found in Appendix A, Tables A.1 and A.4 respectively. Figure 3.9 shows the results for both schemes under a larger Manhattan Radius 1 and 2 architecture as the number of NN interconnects is varied from 0 to the maximum of 32.

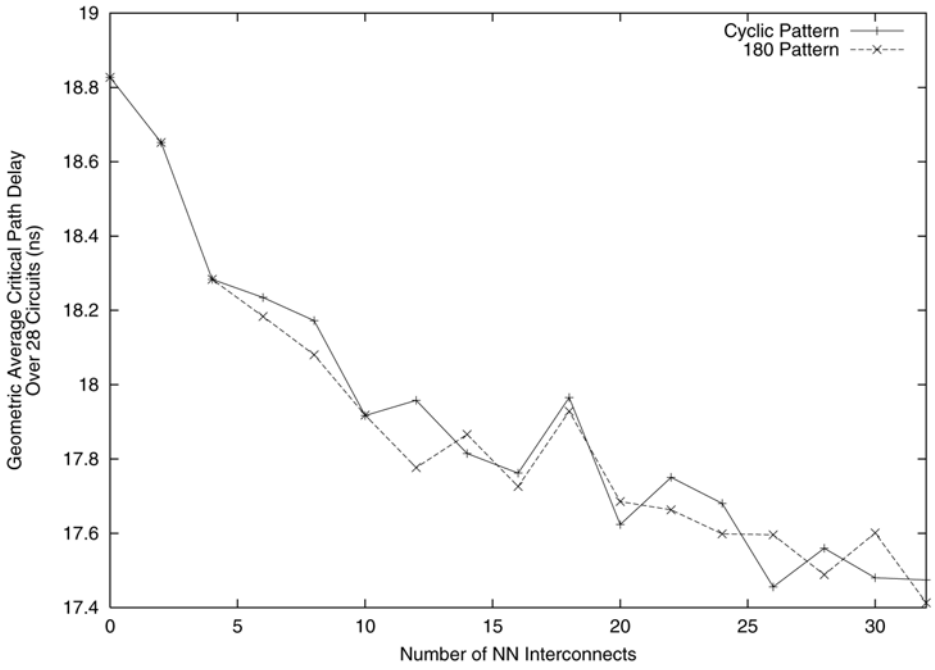


*Figure 3.9 - Delay vs. # of NN interconnects for*

*Two Output Schemes Using a Manhattan Radius 1 & 2 Architecture*

Again, observe that both graphs show little or no difference for the two output schemes, thus it can be safely concluded that there is no real benefit in using one pattern over the other. Tables A.14 and A.16 of Appendix A contains the data for these plots.

Since our choice of output pattern has little bearing on performance, subsequent experiments use the *cyclic* population scheme depicted in Figure 3.6b.

### 3.2.2b NN Interconnect Distribution Among Input Pins

As discussed above, the exact topology of connecting NN interconnects to the input pins also needs careful consideration. Recall from Section 2.1 that there are 10 input pins and 4 output pins on a logic block. These pins are distributed evenly around the perimeter of the block as shown in Figure 3.10. Notice that the top and right sides of the block have only 2 input pins while the left and bottom sides each have 3.

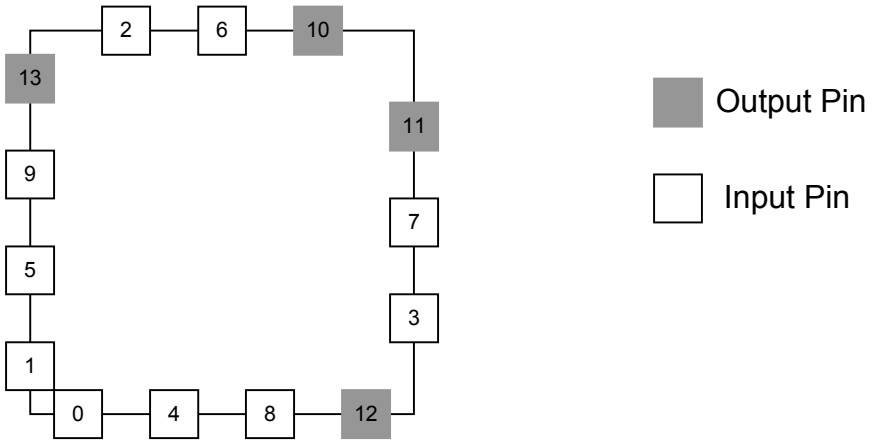


*Figure 3.10 – Pin Distribution Around A Logic Block*

Again consider the output fan out scenario depicted in Figure 3.5. Note that each block, which has 16 outgoing NN interconnects to its four Manhattan neighbours, will also have 16 NN interconnects coming *into* it from *its* neighbours, thus an appropriate scheme for connecting these inputs must be devised. The two general schemes considered were:

1. Attaching the NN interconnect to the nearest possible input pin (from the source block) resulting in shortest possible physical NN interconnect wire length. For example, an NN interconnect originating from output pin 12, attached to a southern neighbour, would have to be connected to input pins 2 or 6. Similarly, a NN interconnect from pin 11 attached to a western neighbouring block would be attached to either pins 3 or 7. Thus, the NN interconnect must attach itself to an input pin on the side of the neighbouring block closest to it. We call this the

*Nearest-Side* input pin connection strategy. The drawback to this strategy is that NN interconnects may not always be evenly distributed across all input pins. Figure 3.11a shows a VPR screen capture of an architecture where when the number of NN interconnects in the Manhattan Radius 1 architecture is 9, input pin 2 has a fan-in of two NN interconnects while inputs 8 and 9 have none. This excessive connectivity at pin 2 and lack of connectivity at pins 8 and 9 will clearly impact routability, because it offers fewer choices to the router.

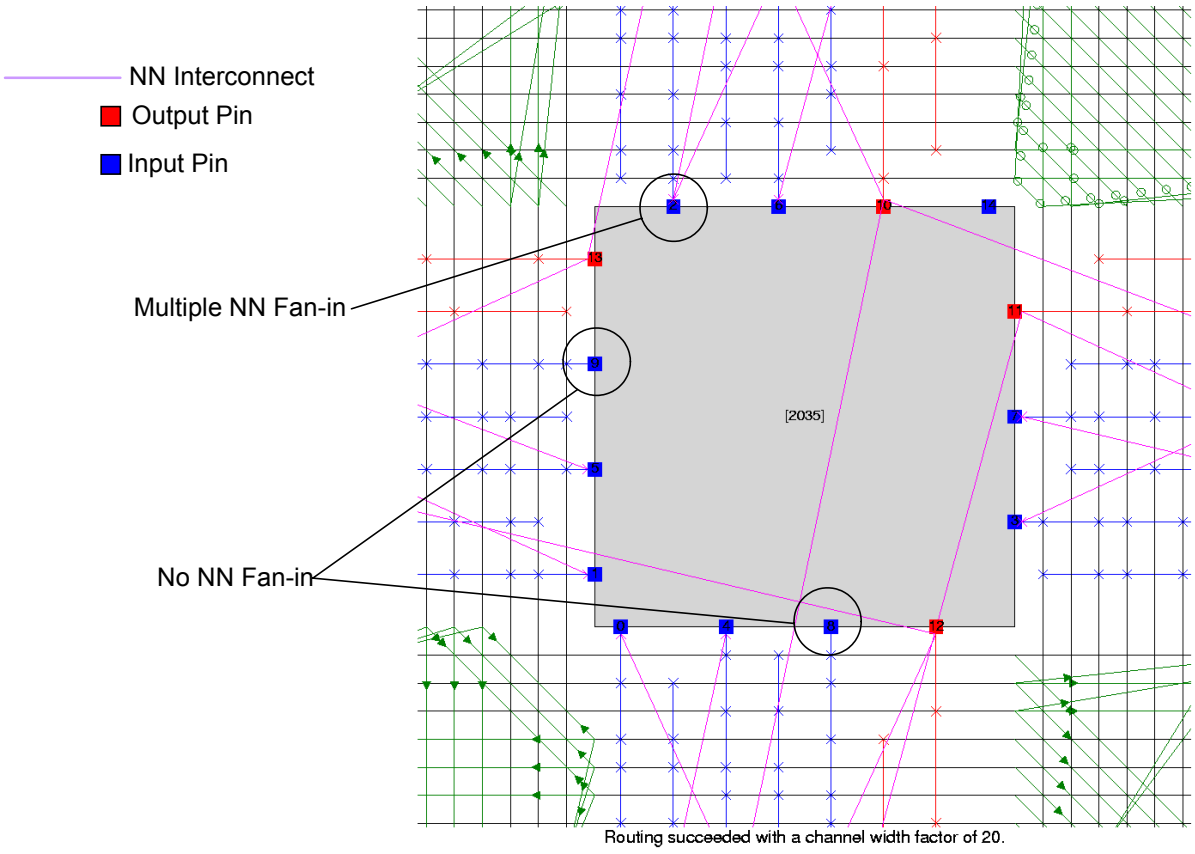


*Figure 3.11a – Manhattan Radius 1, # of NNs = 9*

*Nearest-Side Input Pin Connection Strategy*

2. Another approach is to evenly distribute the NN interconnects among all input pins by ensuring that extra fan-in is not added to an input pin until all other input pins have at least the same amount of fan-in. This is called the *Even-Distribution* Input Pin Connection Strategy. The drawback of this strategy is that NN

interconnect physical wire length is not minimized, however the uneven connectivity problem encountered in Figure 3.11a is alleviated. Figure 3.11b shows a VPR screen capture of the exact scenario of Figure 3.11a, using the Even-Distribution input pin connection strategy.

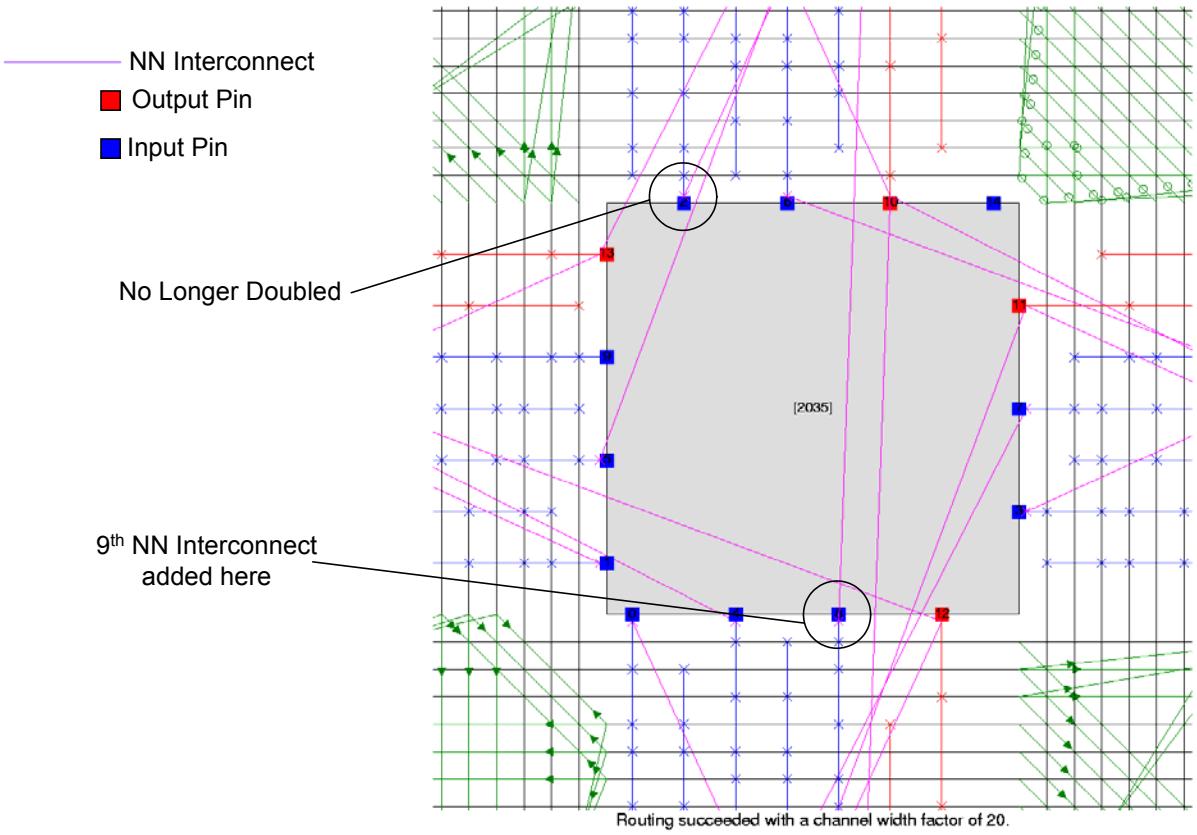


*Figure 3.11b – Manhattan Radius 1, # of NNs = 9*

*Even-Distribution Input Pin Connection Strategy*

Each input pin connection strategy was tested by evaluating its performance for various NN interconnect architectures. Figure 3.12 shows how the average critical path delay (across 28 circuits) varies as we increase the number of NN interconnects present in a small Cross Radius 1 architecture from 0 to the maximum of 16, for the two input pin connection schemes.

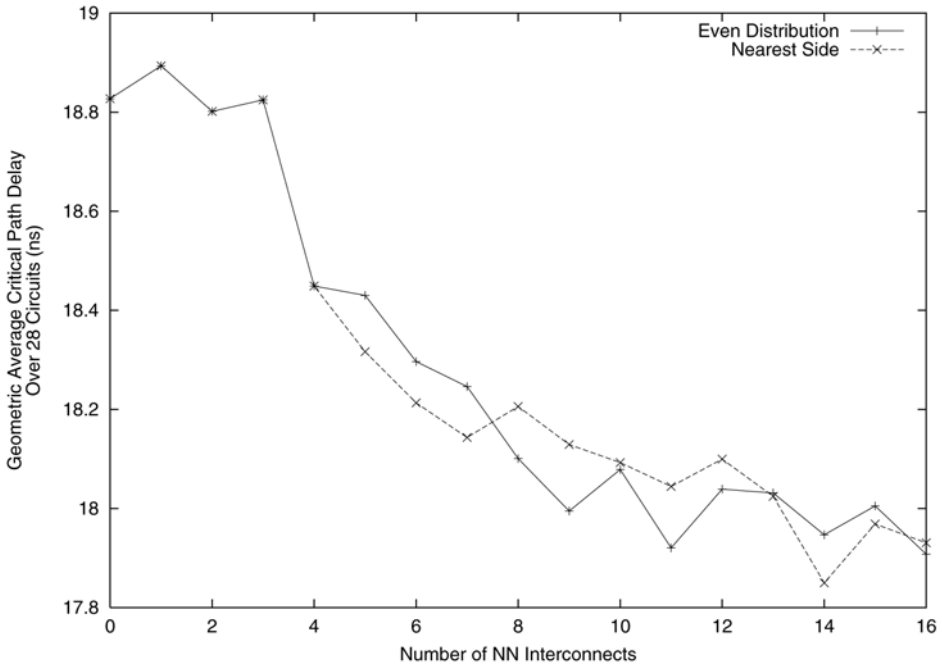


*Figure 3.12 - Delay vs. # of NN interconnects for*

*Two Input Schemes Using a Cross Radius 1 Architecture*

Observe that there is little difference between the two schemes. Refer to Tables A.8 and A.11 of Appendix A for the raw data. Figure 3.13 shows results for the larger Full Radius 1 architecture as the number of NN interconnects is increased from 0 to 32.

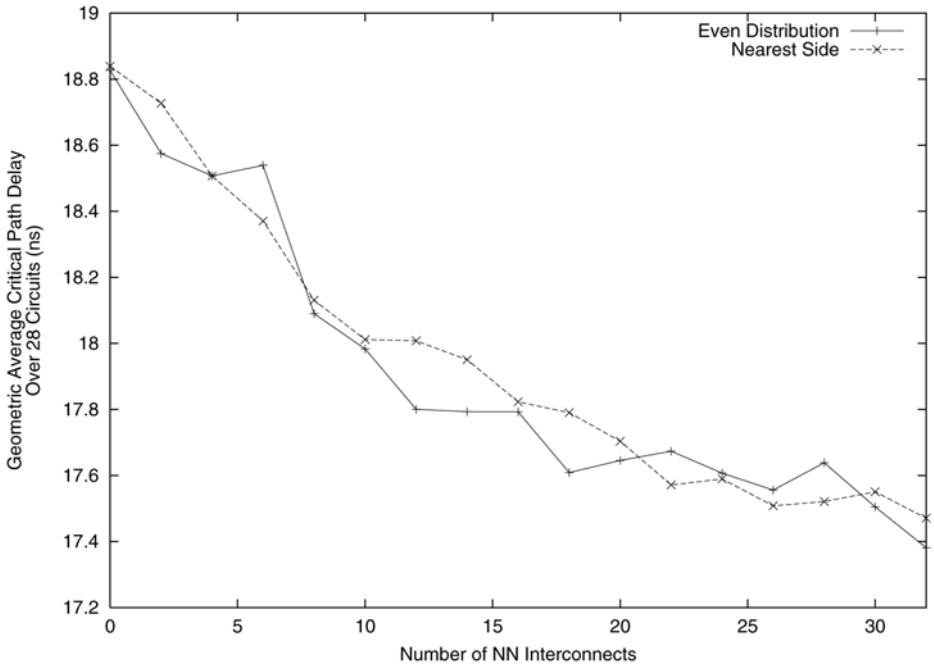


*Figure 3.13 - Delay vs. # of NN interconnects for*

*Two Input Schemes Using a Full Radius 1 Architecture*

Again, note that there is little difference between the two schemes. Tables A.23 and A.25 in Appendix A contains the raw data for this graph. Thus it can be concluded that for the architectures explored, there is little difference in performance between input pin connection strategies, however we believe it is a more intelligent approach to alleviate the problems of uneven assignment since if very large NN architectures (e.g. Radius 3 or 4) were to be explored, uneven distribution on the input pin would pose a problem, thus the experiments in this work use the Even-Distribution strategy.

It was also determined that the additional wire resistance and capacitance due to increased NN interconnect length (which was the width of two logic blocks more in the worst case) in the Even Distribution strategy had negligible impact on the path delay of an NN interconnect, thus not having the NN interconnect wire length minimized was not a major issue. Figure 3.14 shows the best case and worst-case logical NN interconnect length that can occur between adjacent logic blocks. This corresponds to physical distances of approximately 90 microns and 200 microns of length as measured in a 0.18µm CMOS process.

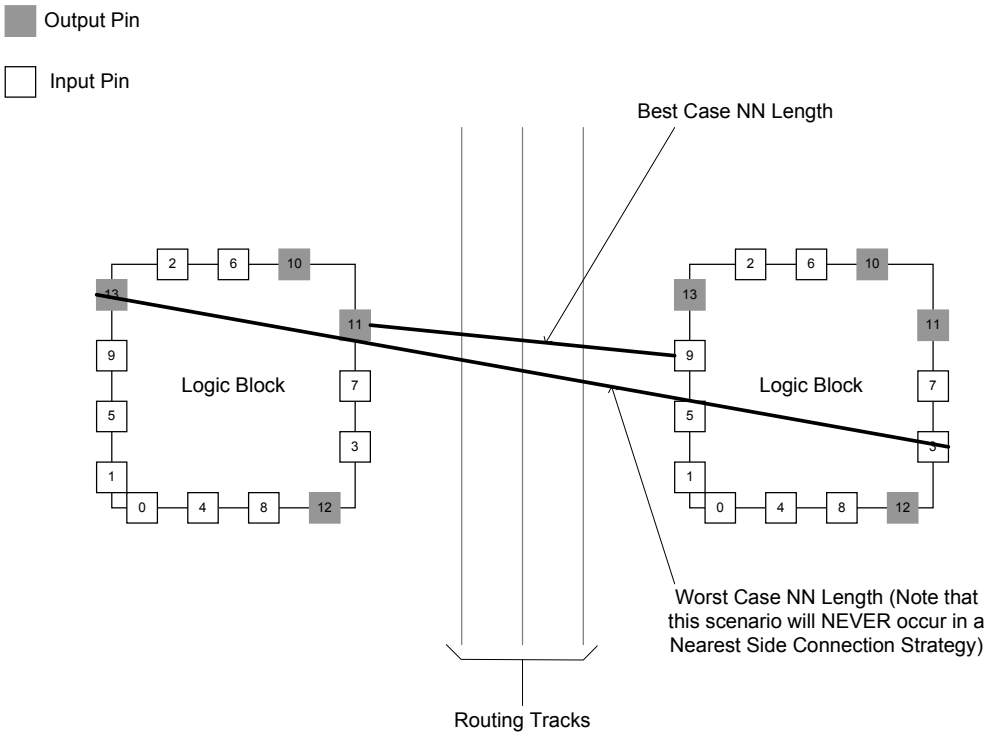


*Figure 3.14 – Best Case and Worst Case NN Lengths for Adjacent Logic Blocks*

In an Even-Distribution connection strategy, both connection scenarios are likely to occur, however in a Nearest-Side strategy, the worst case scenario will never occur. The wire resistance and capacitance were both accurately modelled using SPICE simulations. Table 3.3 shows the measured difference in path delay for the two scenarios.

| | **Path Delay to Immediate Neighbour (ps)** |
|---|---|
| Best Case | 297 |
| Worst Case | 299 |

*Table 3.3 - Path Delay of Best Case vs Worst Case NN interconnect Length*

As we can see there is a negligible 2ps difference in delay between the best and worst case scenarios, thus attempting to minimize wire length through using the Nearest-Side strategy will not have any visible affect on the overall circuit delay.

### 3.2.3 Summary

This section presented a detailed look at the NN interconnect architectural space and the parameters that define that space. We also explored the various methods of populating the architectures. Figures 3.15a, 3.15b and 3.15c shows VPR screen captures for a fully populated Manhattan Radius 1, a fully populated Cross Radius 1 and a ½ populated Full Radius 1 architecture. Each of these architectures contains 16 total NN interconnects and uses the *Cyclic* output fan-out pattern and *Even-Distribution* input connection pattern.

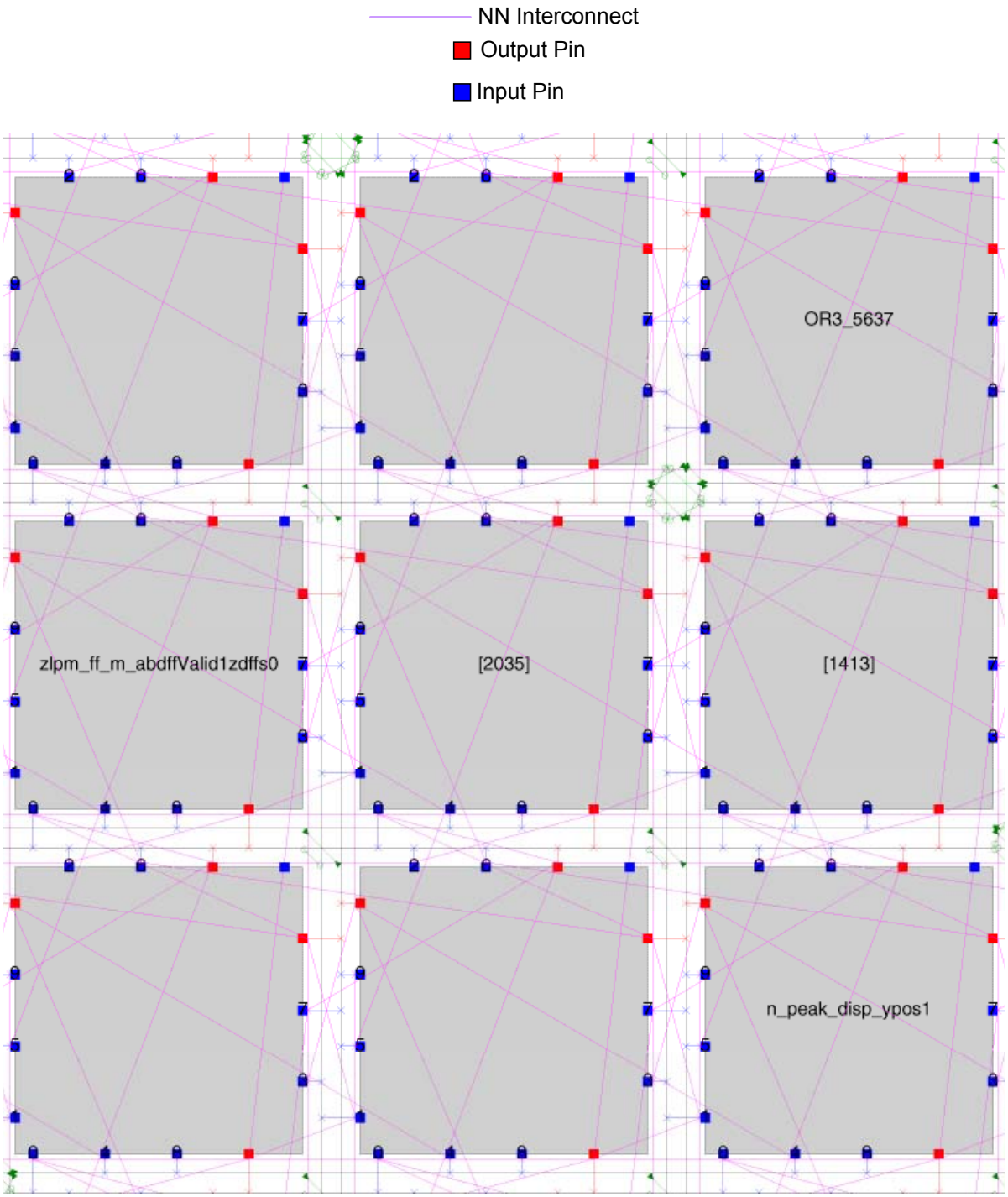


*Figure 3.15(a) – Fully Populated Manhattan Radius 1 Architecture*

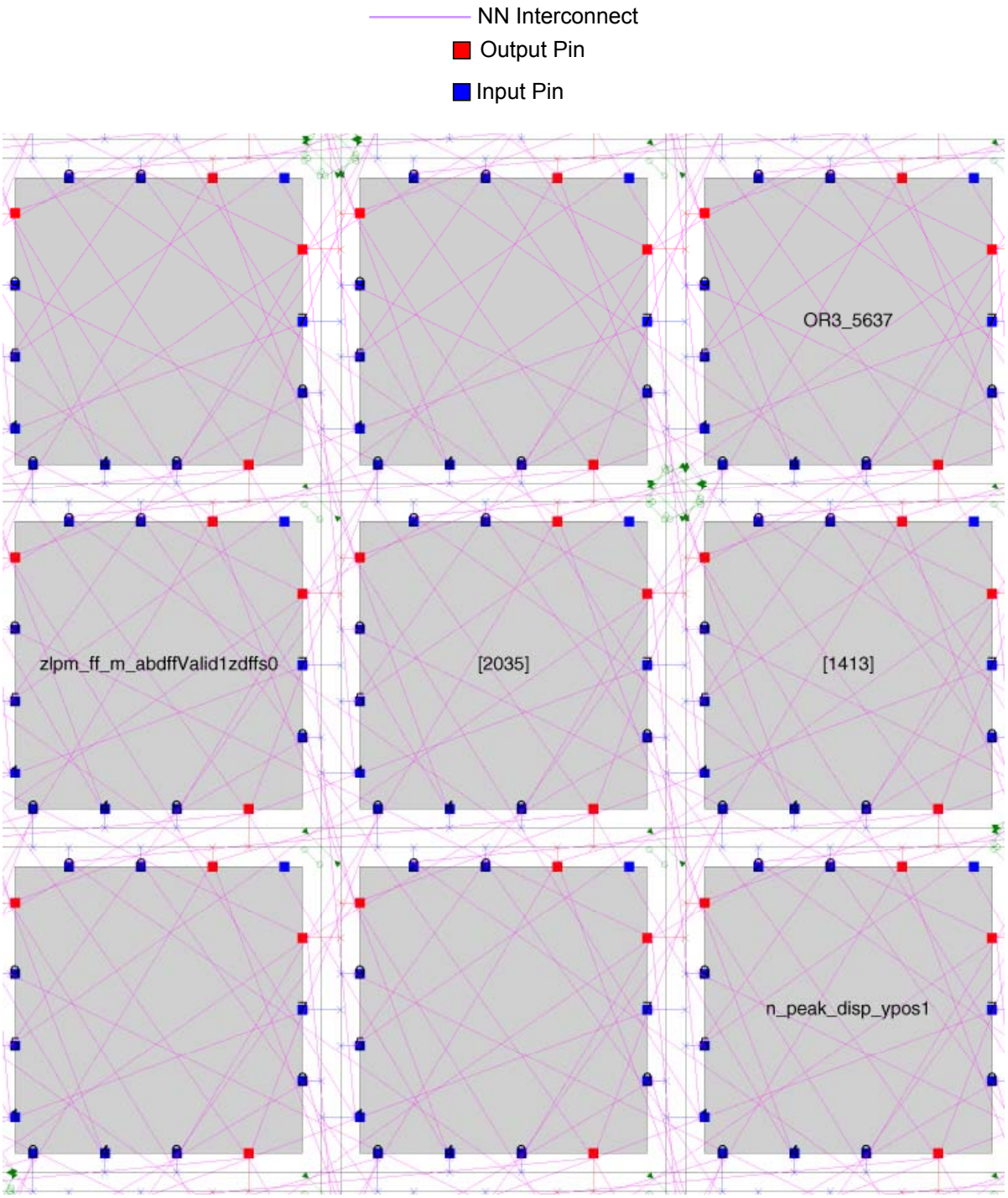


*Figure 3.15(b) – Fully Populated Cross Radius 1 Architecture*

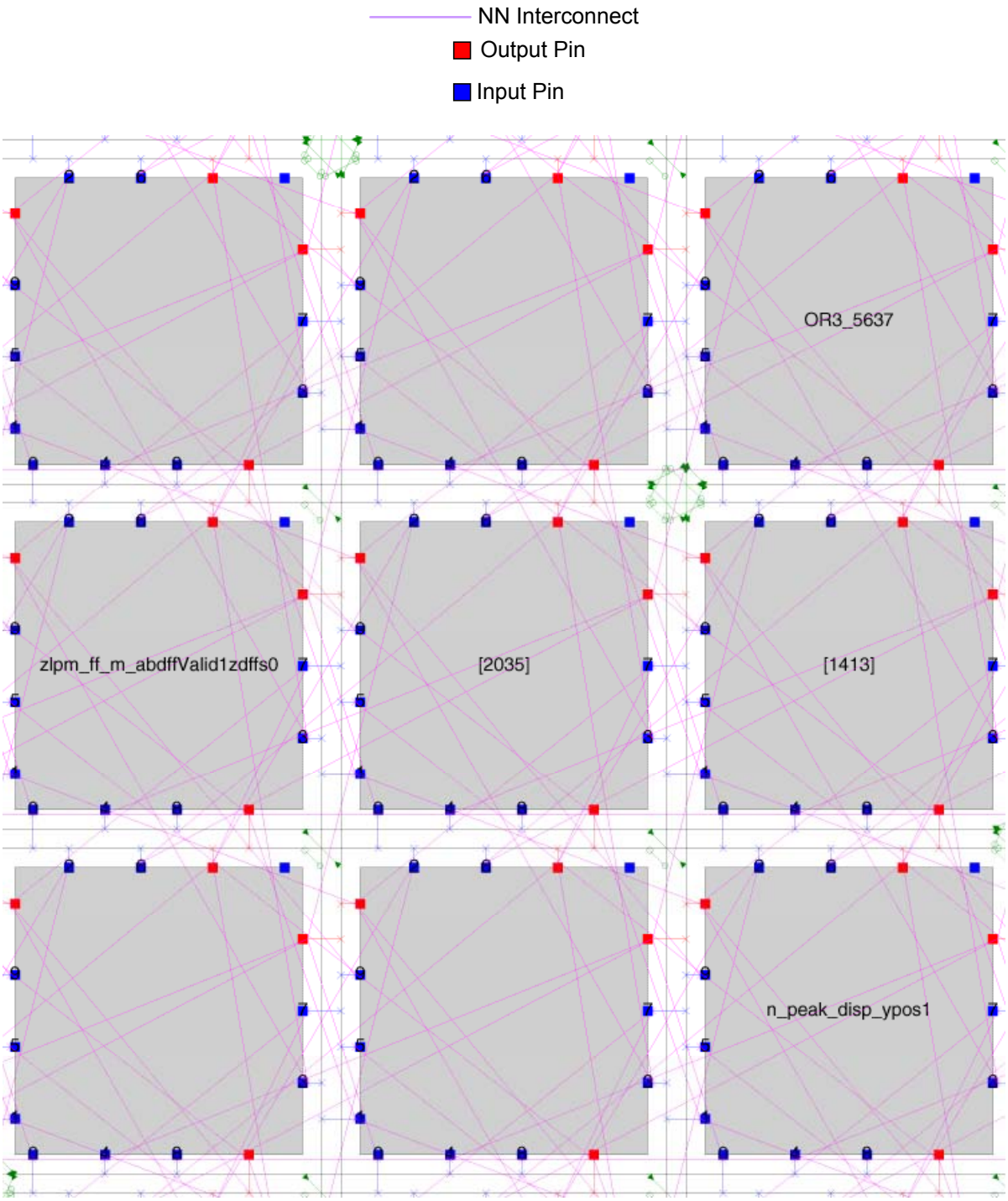


*Figure 3.15(c) – ½ Populated Full Radius 1 Architecture*

## 3.3 Experimental Methodology

Recall the CAD flow described in Section 2.2. This section discusses the modifications made to the original CAD flow previously described.

### 3.3.1 Placement

In order to properly leverage the speed gains of NN interconnects over the conventional routing, it is necessary for the timing driven placement algorithm to be aware of the advantage. The timing-aware nature of the placer described in Section 2.4 should leverage this advantage by placing more critical connections closer together so that they can be routed onto NN interconnects. Thus, during the placement stage, we provide the placer with the architectural details of a fully populated NN interconnect architecture, producing an "*architecture-aware*" placement. Generally, a new placement should be done for each different NN architecture with different quantities of NN interconnections. However, we found that it was only necessary to use a placement targeted to a fully populated architecture, which gave equivalent results and therefore provided an experimental efficiency. We thus avoided the tedious and lengthy task of having to place for every partially depopulated NN value. Thus in subsequent experiments, whenever the number of NN interconnects in the architecture is greater than zero, a placement that was done with knowledge of the presence of a fully populated NN interconnect architecture was used. For example, in a Manhattan Radius 1 architecture, the placer assumes a fully populated (# of NNs = 16) architecture, and this placement is held constant as the number of NNs is varied from 1 to 16 and its effect on delay measured. The benefits of using architecture-aware over architecture-oblivious placement are shown in Figure 3.16.

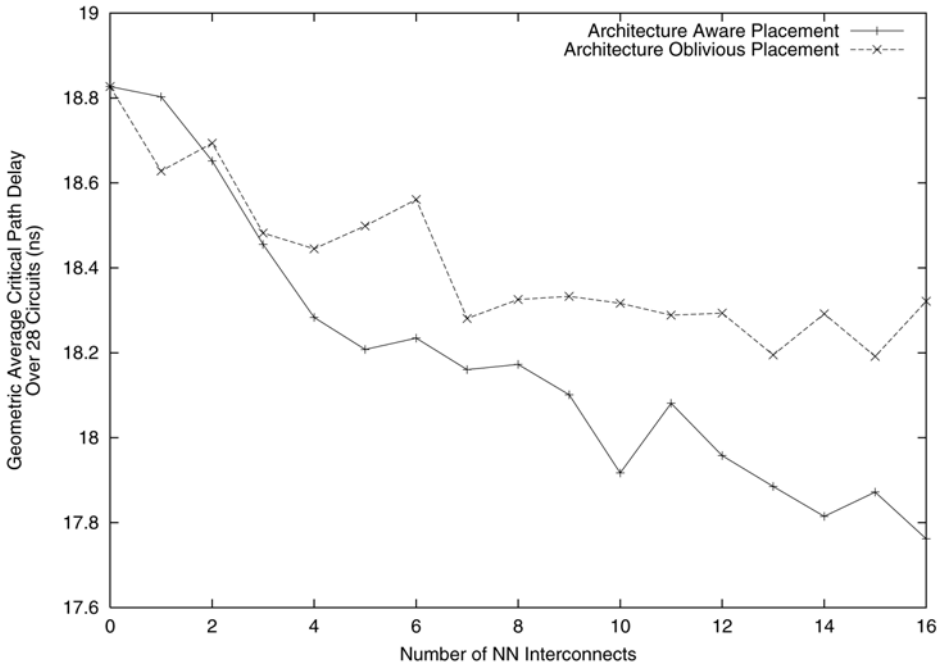


*Figure 3.16 – Delay vs # of NN Interconnects for Architecture-Aware and Architecture-Oblivious Placement in a Manhattan Radius 1 Architecture*

Figure 3.16 shows the geometric average delay across 28 circuits for a Manhattan Radius 1 architecture as the number of NN interconnects is increased from 0 to 16 for both an architecture-aware and architecture-oblivious placement. Observe that an architecture-aware placement results in a 5.7% performance improvement for a fully populated architecture while an architecture-oblivious placement only resulted in 3.4% improvement. See Tables A.1 and A.3 of Appendix A for raw data.

Figure 3.17 shows similar results for a Cross Radius 1 architecture.

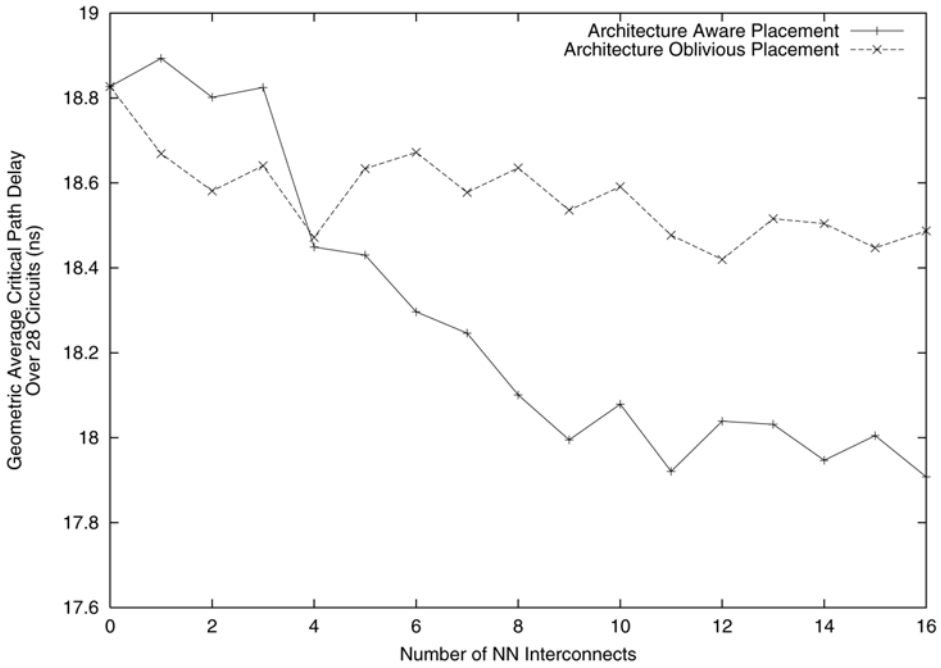


*Figure 3.17 – Delay vs. # of NN interconnects for Architecture-Aware and Architecture-Oblivious Placement in a Cross Radius 1 Architecture*

The architecture-aware placement results in a 4.9% performance gain for a fully populated architecture as opposed to a 1.8% improvement for the architecture-oblivious placement. Tables A.8 and A.10 in Appendix A contains the actual data for this graph.

The benefits of using architecture-aware placement can be explained by observing the critical path of circuits. We performed an experiment in which each placement is analyzed and the average number of short connections along the critical path that fall within the NN Radius of that architecture is computed. For example, in a Manhattan Radius 1 architecture, the number of critical source-sink connections in the circuit that are within this architecture is tallied. This gives us an idea of the number of critical path connections that can be routed onto NN interconnects. Figure 3.18 shows the how the number of critical source sink connections in a Manhattan Radius 1 architecture varies with the number of NN interconnects for both an architecture-aware and architecture-oblivious placement. Figure 3.19 shows this comparison for a Cross Radius 1 architecture.

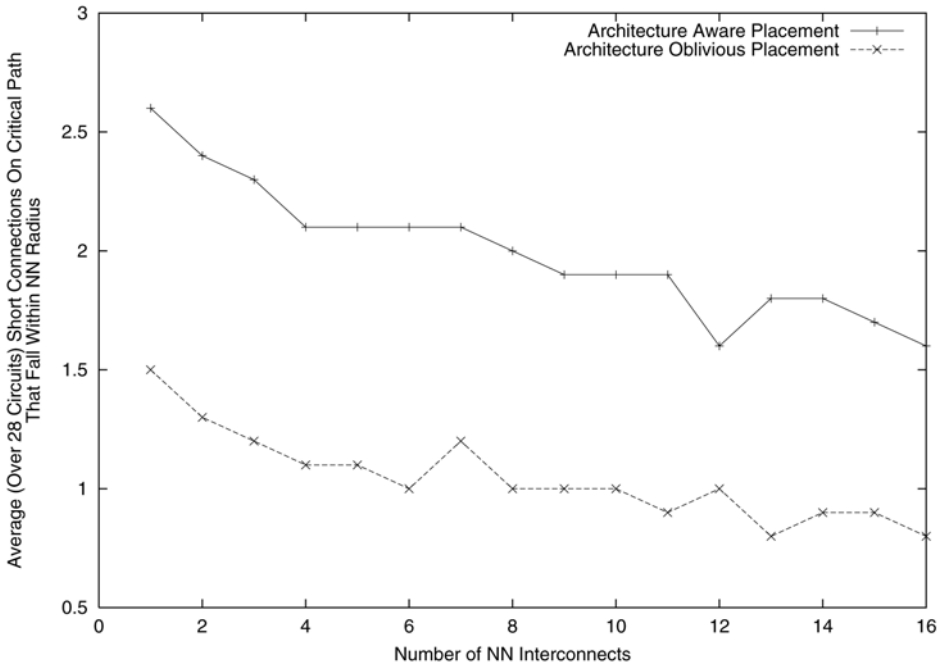


*Figure 3.18 – # of Short Connections Along Critical Path That Fall Within A Manhattan Radius 1*

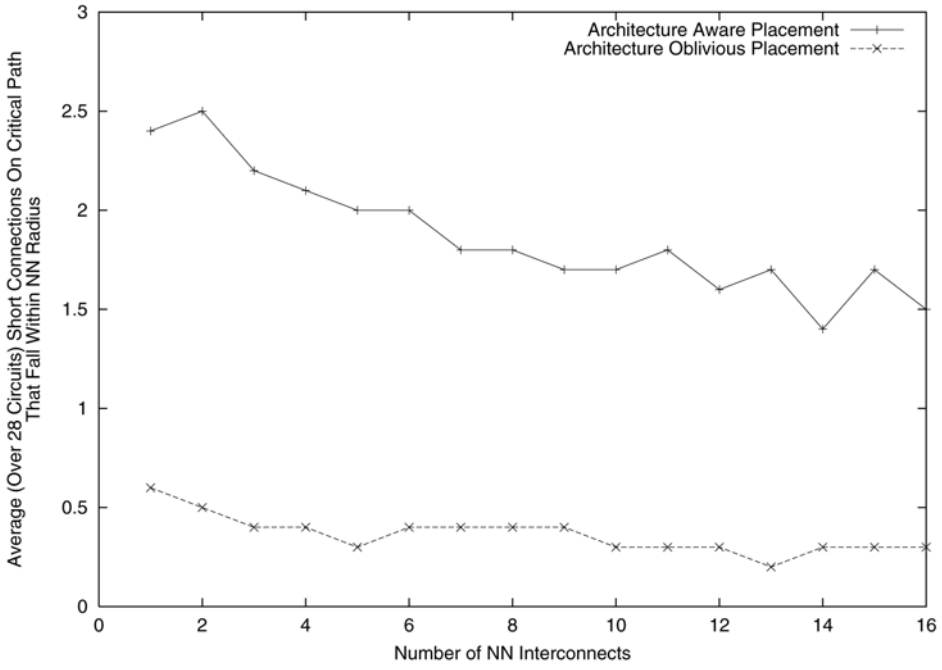


*Figure 3.19 – # of Short Connections Along Critical Path That Fall Within A Cross Radius 1*

It is clear to see that a placement that is cognisant of the architecture will place more nets within the NN radius. This allows for better NN interconnect utilization and increases circuit performance. Also note the slight downward trend of the curves. This downward trend implies that as we increase the number of NN interconnects in the architecture, the number of short connections on the critical path decreases. This is interesting as it implies that the critical path in the circuit changes once nets have been absorbed onto NN interconnects. Thus, the new critical path will be one that consists of more long connections that cannot be absorbed. Tables A.5, A.6, A.12 and A.13 in Appendix A contain the data for these figures.

This trend is true for all other architectures discussed in this work.

### 3.3.2 Noise Elimination

Initial experiments showed that VPR sometimes produced widely varying delay results for a specific quantity of NN interconnects in various architectures. Delay results measured in VPR are inherently noisy due to the fact that complex congestion negotiations are occurring within the router, and that routing is a difficult combinatorial optimization problem. Two methods of eliminating noise are typically employed:

1. Perform multiple placements for a given circuit and architecture and then average the delay results. The results of experiments in this research are averaged over five different placements for each circuit.
2. Modify the routing schedule to resolve congestion more slowly.

The first method is employed in all experiments throughout this work. Figure 3.20 shows how performance varies with the number of NN interconnects in a Manhattan Radius 1 architecture, using only a single placement and then averaging the results over 5 placements.

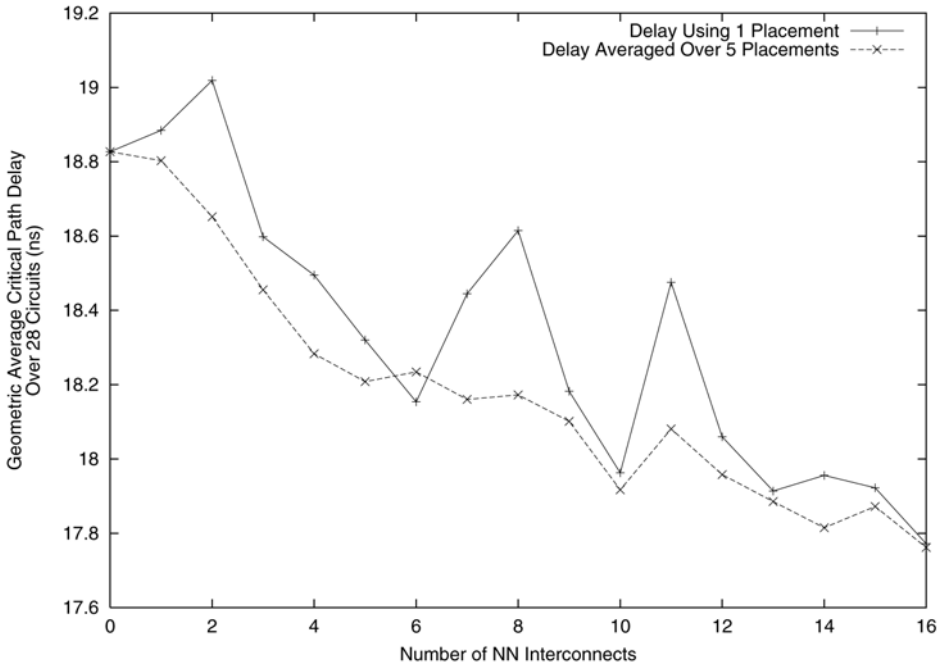


*Figure 3.20 – Effect of Averaging Results Across Multiple Placement Seeds for a Manhattan Radius 1 Architecture*

It can be seen that averaging the results over 5 different placements substantially reduces the noise in the performance characteristics of this graph. Refer to Tables A.1 and A.7 in Appendix A for raw data.

The second option substantially increases the time taken to find a successful route which is not practical. Recall Equation 2.1 from Section 2.3 which gives the cost of including a node in the routing:

$$\mathrm{Cost}(n) = \mathrm{Crit}(i,j)\cdot \mathrm{delay}_{\mathrm{Elmore}}(n) + [1 - \mathrm{Crit}(i,j)]\cdot b(n)\cdot h(n)\cdot p(n)$$

p(n) is the present congestion penalty of the node. It is given by:

$$p(n) = 1 + \max(0, [occupancy(n) + 1 - capacity(n)]\cdot p_{fac})$$

Typically, $p_{fac}$ is initially kept at 0.5 for the first routing iteration then is increased by a factor of 2 times its previous value for subsequent iterations [1]. This factor is called the *$p_{fac}$ multiplier*. This causes the penalty of congestion to grow slowly at first, then rapidly in later iterations. If a value less than 2 is used then $p_{fac}$ grows more slowly, thus congestion takes a longer time to clear up. This increases the effort of the router and typically produces better results since gradual resolution of congestion allows the router to explore more routing paths and possibilities. However it increases the number of routing iterations required to completely route a circuit and consequently, the time required.

By observing the router, we were able to devise a method of eliminating noise due to congestion resolution while still giving us an acceptable routing time. Recall that the routing algorithm is based on the Pathfinder algorithm [1]. In performing a route, VPR will initially route all nets ignoring congestion, then iteratively rip up and re-route all nets gradually resolving congestion while still attempting to optimize the critical path. A route is complete when VPR has resolved the last bit of congestion or has determined that the circuit cannot be routed. It was noted that with some circuits, the final route on which all congestion is cleared, sometimes introduces a new and much longer critical path that can no longer be optimized since the route ends after that iteration. Thus, the algorithm was modified to attempt to keep optimizing the critical path, even after a successful route is found.

Furthermore, the algorithm now continuously calculates a running average of this estimated critical path value and compares it with the current critical path delay. A difference of 5% between the two values is considered an acceptable variation. Thus once a successful route has satisfied that constraint, further attempts to route are terminated. If not, the entire routing is destroyed and VPR will begin again by decreasing the $p_{fac}$ multiplier and increasing the number of routing iterations allowed. This algorithm is given in Figure 3.21.

```
main() {

   do{
      attempt_route();  /* Pathfinder given in Figure 2.7 */

      if (route successful but final crit path delay > avg crit path
          delay by 5%) {

         decrease p_fac multiplier and increase max_router_iterations;
                                          /* increase router effort */

         if (p_fac multiplier too small)
            exit loop and give up, keeping last solution;
                                  /* Taking too long.  Give up. */

      }

   } while (successful route but final crit path delay > avg crit path
            delay by 5%)
}


attempt_route(){

   for (1 to max_router_iterations){

            try_route();      /* Pathfinder */

            if (route is successful)
                  successful_routes++;

      if (route is successful && final crit path delay is within
          5% of avg crit path delay){
         return with full success flag;
      }else if (route is successful && final crit path delay >
                avg crit path delay by 5%){
         if (successful_routes > 5) /* Try up to 5 iterations
                                       after resolving congestion */
            return with partial success flag;
      }else
         return fail;
      }

   }

}
```

*Figure 3.21 – Modified Router Algorithm for Noise Elimination*

Note that under the new algorithm, VPR tries up to 5 more iterations after resolving all congestion before ending, and the exit parameter is set so that the final result must be within

5% of the running estimated average, else the enter routing is destroyed and restarted with increased effort.

The geometric average circuit delay across the 28 benchmark circuits for a typical routing architecture (with no NN interconnects) was 20.3ns. After these modifications the average circuit delay was 18.8ns. This represents a 7.4% improvement in delay in addition to which the noise in performance experiments was greatly reduced.

## 3.4 Summary

In this chapter the NN interconnect architecture was explored in great detail. We presented a circuit level design which was accurately modelled and implemented. We also defined the architectural space to be explored and created generic terminology to describe that space. We then discussed the topological issues of NN interconnect distribution among output pins and input pins, and then finally we presented a modified experimental methodology which will be used in the next chapter to evaluate the NN interconnect architectures presented here.

# *Chapter 4*

# Experimental Results

This chapter presents experiments, using the methodology described in Chapters 2 and 3, that show the performance and area for various NN interconnect architectures. In these experiments, the quantity of NN interconnects present in each of the NN topologies at a given radius is varied and the effect of area and delay is measured. The first set of results focuses primarily on performance (although the effects on area are also shown) while the second set of results focuses primarily on area. The raw data for all results presented in subsequent sections can be found in Appendix I.

Recall from Section 2.2 that the benchmark suite of circuits is comprised of the 20 largest MCNC circuits as well as 8 new circuits created at the University of Toronto. Table 4.1 shows the characteristics of all 28 benchmark circuits used in the experiments in this research. It shows the number of primary inputs and outputs per circuit, the number of LUTs and latches and finally the number of BLEs and total nets after packing.

| Circuit | Primary Inputs | Primary Outputs | LUTs | Latches | BLEs | Total Nets |
|---|---|---|---|---|---|---|
| Alu4 | 14 | 8 | 1522 | 0 | 1522 | 1536 |
| Apex2 | 39 | 3 | 1878 | 0 | 1878 | 1917 |
| Apex4 | 9 | 19 | 1262 | 0 | 1262 | 1271 |
| Bigkey | 263 | 197 | 1707 | 224 | 1707 | 1936 |
| Clma | 383 | 82 | 8381 | 33 | 8383 | 8445 |
| Des | 256 | 245 | 1591 | 0 | 1591 | 1847 |
| Diffeq | 64 | 39 | 1494 | 377 | 1497 | 1561 |
| Display_chip | 35 | 134 | 1781 | 603 | 1794 | 1828 |
| Dsip | 229 | 197 | 1370 | 224 | 1370 | 1599 |
| Elliptic | 131 | 114 | 3602 | 1122 | 3604 | 3735 |
| Ex1010 | 10 | 10 | 4598 | 0 | 4598 | 4608 |
| Ex5p | 8 | 63 | 1064 | 0 | 1064 | 1072 |
| Frisc | 20 | 116 | 3539 | 886 | 3556 | 3576 |
| Img_calc | 39 | 44 | 10093 | 1836 | 10141 | 10180 |
| Img_interp | 43 | 195 | 2667 | 718 | 2727 | 2769 |
| Input_chip | 34 | 47 | 793 | 291 | 807 | 841 |
| Misex3 | 14 | 14 | 1397 | 0 | 1397 | 1411 |
| Pdc | 16 | 40 | 4575 | 0 | 4575 | 4591 |
| Peak_chip | 33 | 22 | 800 | 316 | 809 | 840 |
| S298 | 4 | 6 | 1930 | 8 | 1931 | 1935 |
| S38417 | 29 | 106 | 6096 | 1463 | 6406 | 6435 |
| S38584.1 | 39 | 304 | 6281 | 1260 | 6447 | 6485 |
| Scale125_chip | 24 | 89 | 2608 | 1236 | 2632 | 2654 |
| Scale2_chip | 15 | 96 | 1168 | 370 | 1189 | 1202 |
| Seq | 41 | 35 | 1750 | 0 | 1750 | 1791 |
| Spla | 16 | 46 | 3690 | 0 | 3690 | 3706 |
| Tseng | 52 | 122 | 1046 | 385 | 1047 | 1099 |
| Warping | 41 | 257 | 1275 | 318 | 1353 | 1394 |

*Table 4.1 - Characteristics of Benchmark Circuits*

## 4.1 Performance Results

Recall from Section 2.2.2, that performance results are measured under low stress routing conditions. This means that the smallest FPGA (in terms of both grid size and track count) required to fit the circuit is first found and then 20% more tracks are added to it. Also recall from Section 3.3 that we average the results over 5 different architecture-aware placements.

The delay results are divided into two sections. In the first section the smaller Manhattan and Cross Radius 1 architectures (where the maximum number of NN interconnects is 16) are discussed. In the second section we present results for the larger Manhattan and Cross Radius 1 and 2, as well as the Full Radius 1 architecture where the maximum number of NN interconnects is 32. Radii beyond this are not explored since the area penalty becomes too heavy thus cancels any performance benefits that may be netted from extending to Radius 3, 4, etc.

Note that the results presented here employ a *cyclic* output fan-out pattern and an *even-distribution* input connection pattern as discussed in Section 3.2.2

### 4.1.1 Manhattan & Cross Radius 1

Figure 4.1 shows the geometric average critical path delay (measured as discussed in Section 2.2.2) across 28 circuits for a Manhattan Radius 1 architecture as the number of NN interconnects is increased from 0 to 16. It also shows how total area (measured in terms of minimum-width transistors areas, as described in Section 2.2.1) increases as NN interconnects are added to the architecture. Recall that a Manhattan Radius 1 architecture employs NN interconnects that connect to the immediate North, South, East and West neighbours, distance 1 logic block away, as illustrated in Figure 3.3a.

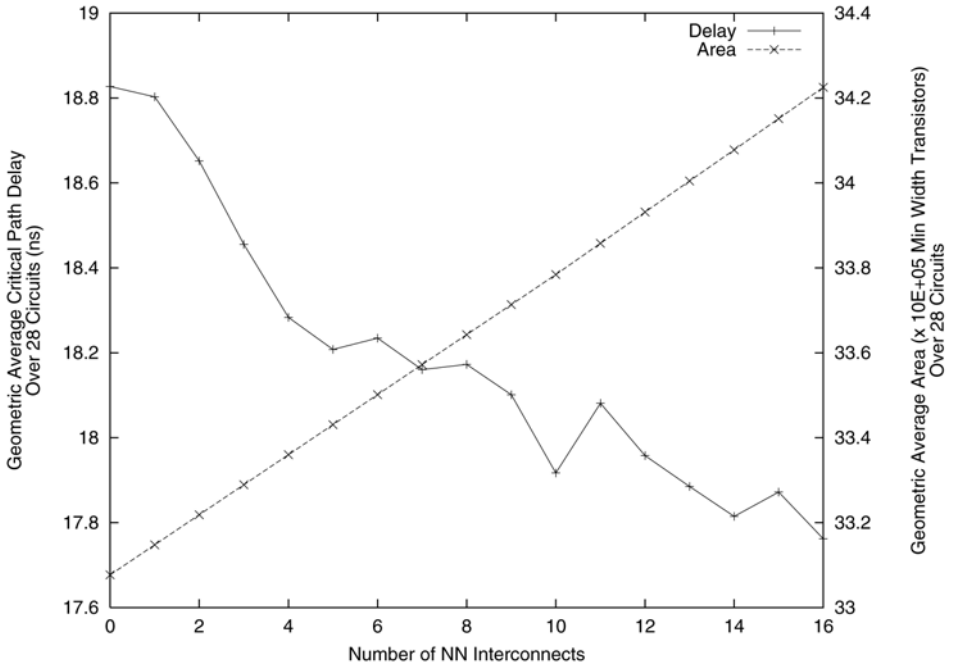


*Figure 4.1 – Delay & Area vs. # of NN interconnects for Manhattan Radius 1*

Observe that a 5.7% performance improvement is achieved for a fully populated architecture. The resulting cost in total area for a fully populated architecture is 3.5%. Note that using 10 NN interconnects nets the majority of the performance improvement. At this point, a 4.8% speedup for a cost of 2.1% in area can be obtained. See Tables A.1 and A.2 in Appendix A for the raw data.

Figure 4.2 gives a similar result for the Cross Radius 1 architecture, in which logic blocks connect only to their NE, SE, SW and NW neighbours as illustrated in Figure 3.3b.

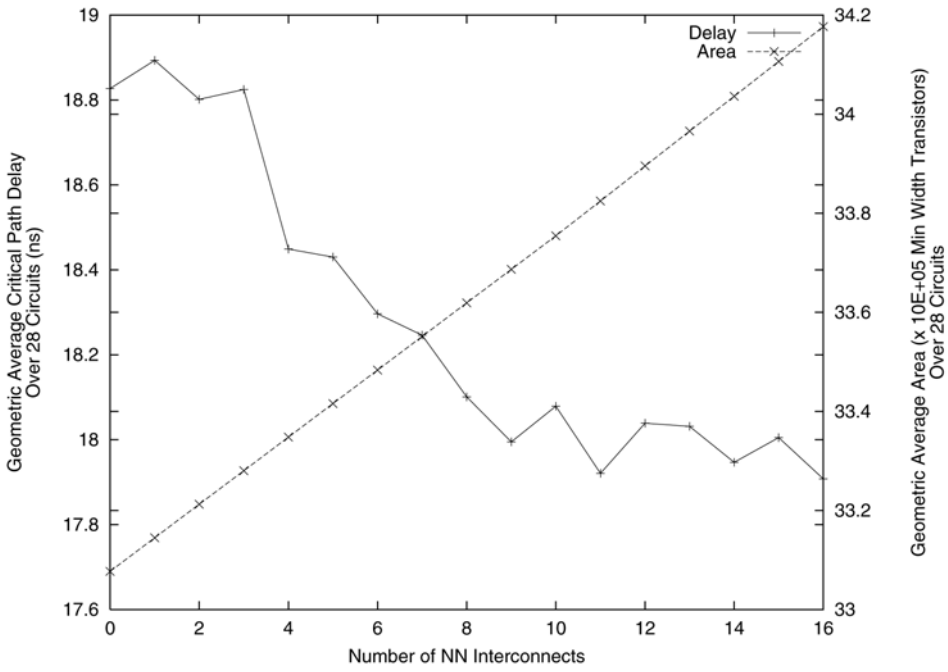


*Figure 4.2 – Delay & Area vs. # of NN interconnects for Cross Radius 1*

The results show that a 4.9% performance gain for a fully populated architecture is achieved. The resulting area increase was 3.3%. Most of the performance increase can be had using 11 NN interconnects. This results in a 4.8% better performance at a cost of 2.3% more area. Tables A.8 and A.9 of Appendix A contains the data for this plot.

### 4.1.2 Manhattan/Cross Radius 1 & 2, Full Radius 1

These architectures are larger and have 32 NN interconnects each for a fully populated scheme. The Manhattan and Cross Radius 1 and 2 schemes have both 16 NN interconnects in Radius 1 and another 16 in Radius 2. In increasing the number of NNs from 0 to 32, Radius 1 is first filled before filling Radius 2. Figure 4.3 shows the geometric average area and delay across 28 circuits for a Manhattan Radius 1 & 2 architecture.

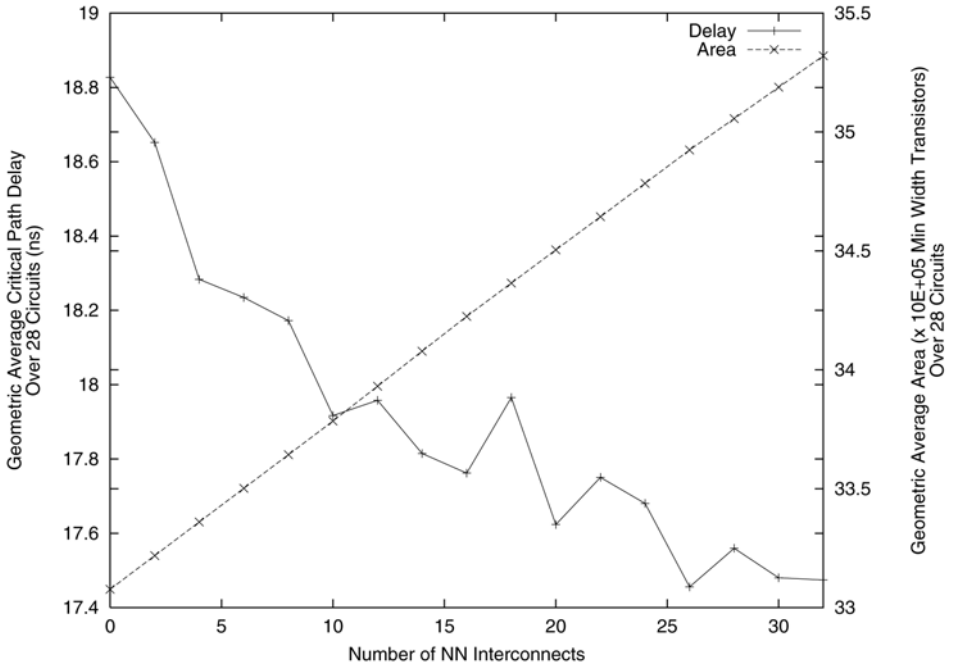


*Figure 4.3 – Delay & Area vs. # of NN interconnects for Manhattan Radius 1 & 2*

It can be seen that for a fully populated architecture, a 7.2% performance improvement can be extracted for a 6.8% area penalty. Observe that this can be minimized by using only 20 NN interconnects. This will give us a 6.4% decrease in critical path delay for a 4.3% cost in area. Tables A.14 and A.15 in Appendix A contains the raw data.

Figure 4.4 shows results for a Cross Radius 1 and 2 architecture.

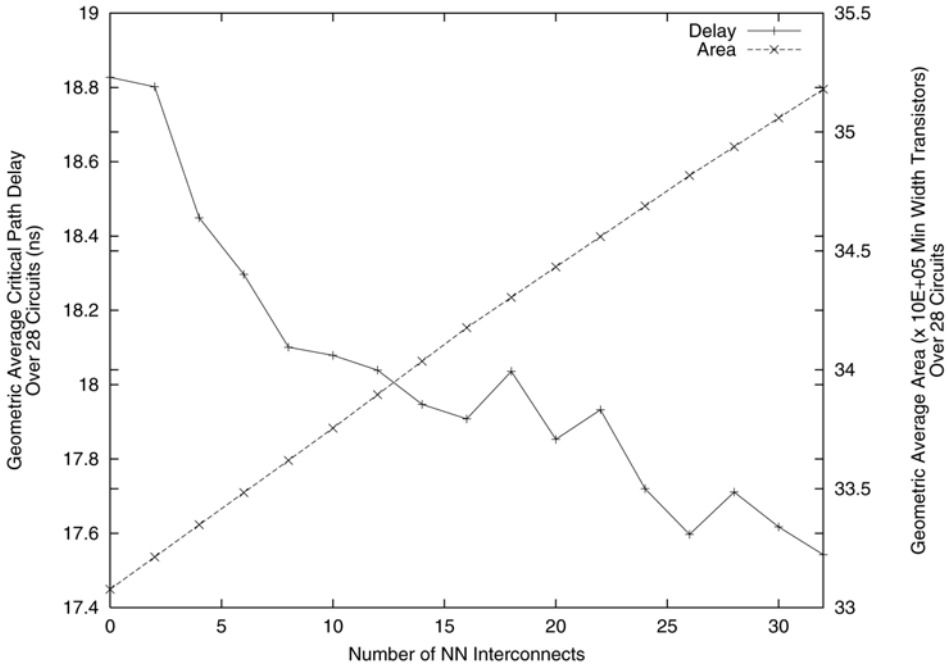


*Figure 4.4 – Delay & Area vs. # of NN interconnects for Cross Radius 1 & 2*

It can be seen that a fully populated architecture reduces the average critical path delay by 6.8% at the cost of a 6.4% increase in area. Using 26 NN interconnects will give us a 6.4% improvement for a 5.3% increase in area. Tables A.19 and A.20 of Appendix A contains the plot data.

Figure 4.5 shows results for a Full Radius 1 architecture.

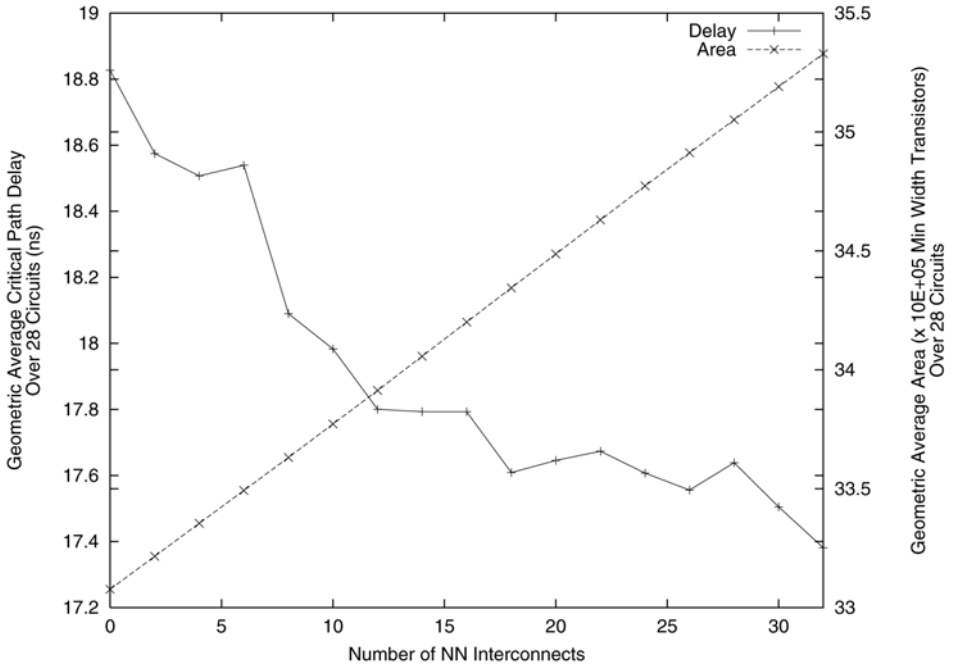


*Figure 4.5 - Delay & Area vs. # of NN interconnects for Full Radius 1*

A fully populated Full Radius 1 architecture reduces the critical path delay by 7.7% for a 6.8% increase in total area. Using only 18 NN interconnects however nets us a 6.4% performance improvement for a 3.8% increase in area. See Tables A.23 and A.24 for raw data.

### 4.1.3 Summary

The performance results of the previous sections are summarized in Tables 4.2 and 4.3. Table 4.2 shows the area and delay results for fully populated architectures while Table 4.3 shows the same results for partially depopulated architectures. The partially depopulated figures were taken by observing each curve and finding the point where adding more NN interconnects produced little or no performance increase.

| Topology (Radius) | # of NNs | Avg. Delay (ns) | Change In Delay | Change In Total Area |
|---|---|---|---|---|
| Manhattan (1) | 16 | 17.8 | - 5.7 % | + 3.5 % |
| Cross (1) | 16 | 17.9 | - 4.9 % | + 3.3 % |
| Manhattan (1 & 2) | 32 | 17.5 | - 7.2 % | + 6.8 % |
| Cross (1 & 2) | 32 | 17.6 | - 6.8 % | + 6.4 % |
| Full (1) | 32 | 17.4 | - 7.7 % | + 6.8 % |

*Table 4.2 – Delay and Area Results for Fully Populated Architectures*

| Topology (Radius) | # of NNs | Avg. Delay (ns) | Change In Delay | Change In Total Area |
|---|---|---|---|---|
| Manhattan (1) | 10 | 17.9 | - 4.8 % | + 2.1 % |
| Cross (1) | 11 | 17.9 | - 4.8 % | + 2.3 % |
| Manhattan (1 & 2) | 20 | 17.6 | - 6.4 % | + 4.3 % |
| Cross (1 & 2) | 26 | 17.6 | - 6.4 % | + 5.3 % |
| Full (1) | 18 | 17.6 | - 6.4 % | + 3.8 % |

*Table 4.3 - Area & Delay Results for Partially Populated Architectures*

It can be seen that in the case of both populated and depopulated architectures, the Full Radius 1 architecture is clearly superior. In the depopulated scheme we are able to achieve a 6.4% reduction in critical path delay at a cost of only 3.8% in total FPGA area.

It is also interesting to note that we can evaluate the performance of several of the commercial NN interconnect architectures by comparing them to the results presented here. While we understand that the architectures of the commercial FPGAs will vary in a number of ways from the architectures used here, we believe that it would still be instructive to attempt to quantify the gains of the commercial architectures by comparing them to the closest possible NN interconnect architectures presented here. Table 4.4 presents the commercial architectures, their closest approximation under our nomenclature, and their

performance results. The performance results are obtained from the raw data of the NN architectures given in Appendix A.

| Commercial FPGA | Approximate NN Architecture | Change in Critical Path Delay |
|---|---|---|
| Algotronix CAL1024 | Manhattan Radius 1, # of NNs = 4 | -2.7 % |
| Xilinx 3000 | Manhattan Radius 1, # of NNs = 4 | -2.7 % |
| Atmel AT6000 | Manhattan Radius 1, # of NNs = 8 | -3.2 % |
| Xilinx Virtex/Virtex-E | N/A | N/A |
| Xilinx Virtex II | Full Radius 1, # of NNs = 16 | -5.3 % |
| Altera Flex 6000 | N/A | N/A |
| Altera Flex 20K | N/A | N/A |
| Atmel AT40K | Full Radius 1, # of NNs = 8 | -3.2 % |

*Table 4.4 – Performance Evaluation of Commercial NN Interconnect Architectures*

We can see that the Xilinx Virtex II architecture has the best NN interconnect performance, resulting in a 5.3 % reduction in critical path delay.

## 4.2 Area, Track Count & NN Interconnects

In the previous section, all architectural parameters, including track count, were held constant as NN interconnects were added to the architecture. It is reasonable to assume that since nets are now routed on NN interconnects, the actual number of tracks required by the FPGA to achieve routability will be reduced. In this section we investigate how area will be affected if the track count is allowed to vary. For this set of experiments, we experimentally determine the minimum number of tracks required to achieve routability as the number of NN interconnects in the architecture is increased.

Figure 4.6 shows how the area varies as the number of NN interconnects is increased from 0 to 32 for our three large architectures – Manhattan and Cross Radius 1 and 2, and Full Radius 1. Observe that the curves are flat for the first 10 to 12 NN interconnects. Here the area required to add NN interconnects is being balanced by the area saved in reducing track count. Figure 4.7 shows how the track count varies as the number of NN interconnects in the various architectures is increased.

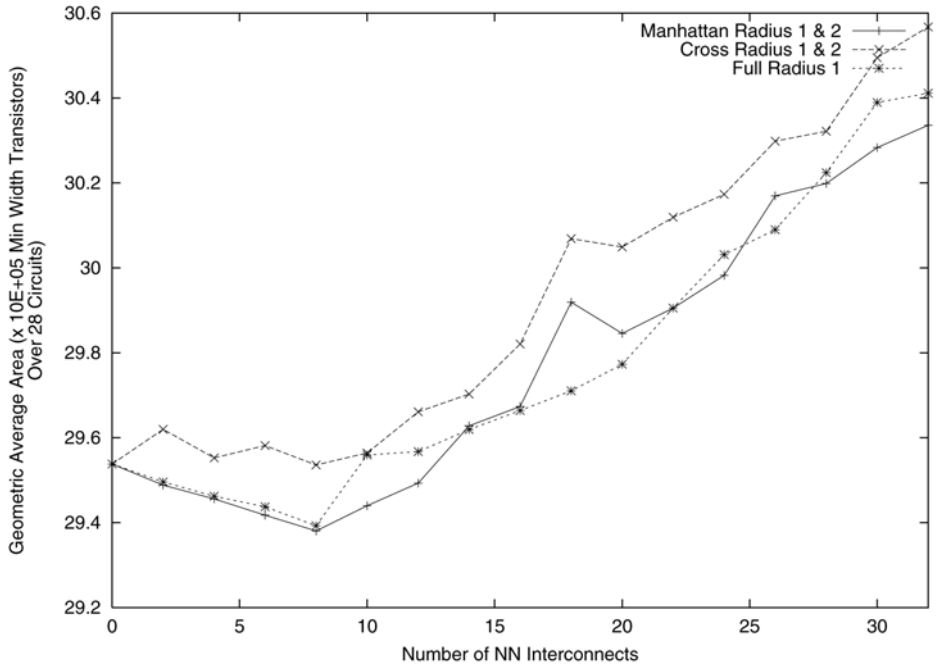


*Figure 4.6 - Average Area vs # of NN Interconnects*

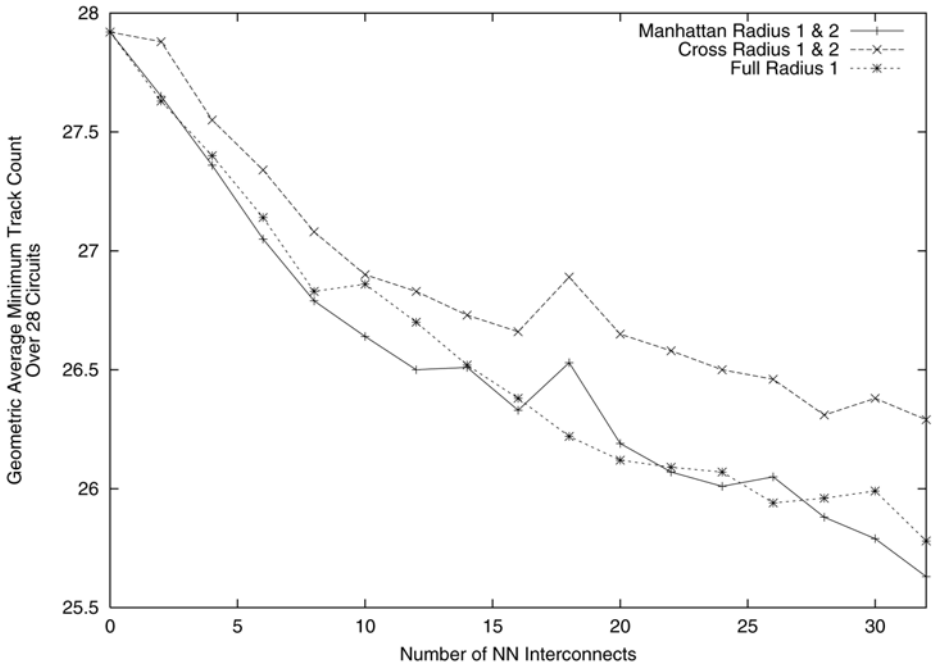


*Figure 4.7 - Track Count vs # of NN Interconnects*

It can be seen from Figure 4.6 that, for each architecture, a particular number of NN interconnects can be added for zero change in total area. The Manhattan topology gives us the best result, allowing 12 NN interconnects to be added to the architecture for zero change in overall area. At this point the FPGA also requires 5% less tracks to achieve routability. Refer to Tables A.17, A.21 and A.26 of Appendix A for the raw data for the area curves of Figure 4.6 and Tables A.18, A.22 and A.27 in Appendix A for the track count data of Figure 4.7.

### 4.2.1 Summary

Table 4.5 summarizes the area results and lists the number of NN interconnects that can be added for no change in total area and also shows the track-count reduction at that point.

| Topology (Radius) | # NNs That Achieve Same Area | Track Count Reduction |
|---|---|---|
| Manhattan (1 & 2) | 12 | 5.0 % |
| Cross (1 & 2) | 9 | 3.3 % |
| Full (1) | 9 | 3.5 % |

*Table 4.5 – Area-Neutral Architectures that Contain NN Interconnects*

It can be seen that a Manhattan topology is best in terms of area, allowing us to add more NN interconnects to the architecture for no change in total FPGA area. It also gives us the most track count reduction.

# *Chapter 5*

# Conclusions & Future Work

## 5.1 Conclusions

This work has presented and examined a broad range of Nearest Neighbour Interconnect architectures for Field-Programmable Gate Arrays. This was performed in an extensive experimental framework which included circuit design and a number of variants of architectural implementation. We have drawn the following conclusions:

1. A Full Radius 1 architecture populated with 18 NN interconnects is best in terms of delay, giving a 6.4% reduction in critical path delay at a cost of a 3.8% increase in total FPGA area.
2. A Manhattan Radius 1 architecture is best in terms of area since we can add up to 12 NN interconnects without any increase in area. At this point we also show that the minimum track count required to achieve routability is reduced by 5%.
3. Architecture-aware placement is essential to achieving proper NN interconnect utilization. It was shown that architecture-aware placement has more critical path nets placed within the NN Radius, thus allowing better NN utilization.
4. The ways in which NN interconnect fan-out is added at the output pins of a logic block is of little importance.
5. Using an input pin connection strategy which evenly distributes NN interconnect to all input pins shows no immediate benefits over the one that goes to the input pins on the nearest side of a neighbouring logic block, however, we believe that

an *Even-Distribution* pattern is a more intelligent choice as it would alleviate uneven pin assignment problems if very large architectures were to be explored.

This research has contributed to the field of FPGA research in the following ways:

1. This is the first published work to empirically explore the architecture of Nearest Neighbour interconnects.
2. We have created a taxonomy of the NN interconnect architectural space.
3. We have classified and evaluated previous NN interconnect architectures within this framework

## 5.2 Future Work

It would be interesting to determine what would happen if NN interconnects were connected directly to local routing multiplexers *inside* of a logic block rather than to the input connection block multiplexer as illustrated in Figure 5.1. This would reduce the flexibility of NN interconnects, however it would further reduce the delay cost.

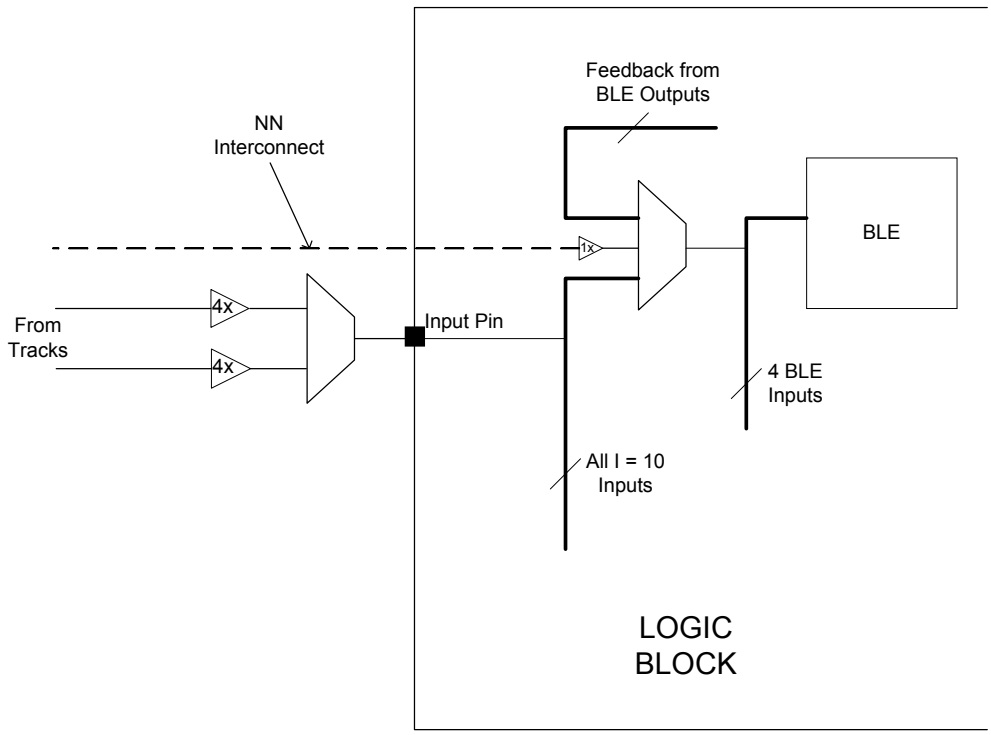


*Figure 5.1 – Alternative NN Interconnect Design*

Compare this to the original NN interconnect setup in Figure 3.1. We see that implementing this new scheme will also save the propagation delay through the input multiplexer.

Currently, VPR is not able to model routing inside of a cluster thus this scheme cannot be implemented with the release of VPR used in this research. A router capable of performing inter-cluster routing is currently under development by Guy Lemieux [33] at the University of Toronto.

Although not explored in this thesis, it would be interesting to see how very large NN interconnect architectures would affect area and delay. However, because very large architectures would have a huge impact on total FPGA area, intelligent depopulation schemes would have to be devised to minimize this penalty.

Also, since architecture-aware placement is key to proper NN utilization, better placement algorithms may be explored. A placer that would more aggressively optimize for NN

interconnect presence would try to fit as many nets as it could into all available radii and thus increase the overall performance of NN interconnect architectures.

Finally, it would be instructive to see the effect of other FPGA parameters on the use of NN interconnects. The parameters to vary would be the length of the routing tracks and the cluster size. Larger clusters may allow the placer to place logic blocks in such a manner that we can fit more critical path nets onto NN interconnects, however smaller clusters may result in an FPGA with more short connections.

# *Appendix A*

# Experimental Data

This Appendix contains the raw circuit data from all experiments conducted in this research. Note that all the data present here is averaged over 5 different placements with the exception of Tables A.2, A.7, A.9, A.15, A.20 and A.24. Table A.7 was used to show how the output performance characteristics is noisy when not averaged across 5 placements while the other tables contain data for area measurements taken under constant track count, thus this measurement is very reliable with only one placement.

All tables presented show the overall change in delay or change in area for each circuit. This change is calculated as:

$$\left( \frac{\text{Area/Delay}_{\text{Fully Populated}} - \text{Area/Delay}_{\text{No NN Interconnects}}}{\text{Area/Delay}_{\text{No NN Interconnects}}} \right) \times 100$$

Table A.29 is a key table that can be used to refer Tables A.1 – A.28 to the appropriate figures and tables in Chapters 3 and 4.

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 15.3 | 15.2 | 15.5 | 15.3 | 15.4 | 15.4 | 15.4 | 15.2 | 15.2 | 15.5 | 15.2 | 15.3 | 14.9 | 15.3 | 15.1 | 15.0 | -4.2 |
| Apex2 | 17.0 | 17.3 | 17.1 | 17.5 | 16.9 | 17.1 | 17.1 | 17.1 | 16.8 | 17.0 | 17.1 | 17.1 | 16.7 | 17.1 | 16.9 | 16.7 | 16.6 | -2.3 |
| Apex4 | 15.8 | 15.8 | 15.3 | 15.6 | 15.4 | 15.0 | 15.3 | 16.3 | 15.8 | 16.2 | 15.1 | 15.1 | 15.2 | 15.4 | 15.9 | 15.2 | 15.2 | -3.4 |
| Bigkey | 8.8 | 9.0 | 8.7 | 8.6 | 8.5 | 8.4 | 8.7 | 8.9 | 8.7 | 8.7 | 8.8 | 8.9 | 8.7 | 8.7 | 8.3 | 8.2 | 8.4 | -4.8 |
| Clma | 34.2 | 32.8 | 34.9 | 34.9 | 33.7 | 32.6 | 33.7 | 33.7 | 36.6 | 35.4 | 34.2 | 34.8 | 34.3 | 32.8 | 32.4 | 33.9 | 33.9 | -1.0 |
| Des | 15.6 | 15.7 | 15.3 | 15.6 | 15.8 | 15.3 | 15.1 | 14.9 | 15.1 | 15.8 | 15.4 | 15.2 | 15.1 | 15.4 | 14.9 | 14.8 | 14.9 | -4.5 |
| Diffeq | 18.2 | 18.5 | 17.5 | 17.3 | 17.1 | 16.6 | 16.8 | 16.5 | 16.9 | 16.9 | 16.6 | 16.5 | 16.2 | 16.0 | 16.4 | 16.2 | 16.0 | -11.9 |
| Display_chip | 16.6 | 16.8 | 16.7 | 16.5 | 16.4 | 16.6 | 16.3 | 16.3 | 16.2 | 15.7 | 16.0 | 15.6 | 15.6 | 16.0 | 15.6 | 15.9 | 15.7 | -5.5 |
| Dsip | 8.0 | 8.2 | 8.1 | 8.2 | 8.1 | 8.1 | 8.3 | 7.8 | 8.2 | 8.2 | 8.2 | 8.0 | 8.4 | 7.6 | 8.1 | 8.5 | 8.2 | 1.8 |
| Elliptic | 24.6 | 26.0 | 25.8 | 24.5 | 24.9 | 25.6 | 24.7 | 24.7 | 24.4 | 24.5 | 25.1 | 24.7 | 25.0 | 24.9 | 23.8 | 24.3 | 24.1 | -2.3 |
| Ex1010 | 26.3 | 25.1 | 26.0 | 24.2 | 24.6 | 24.6 | 25.0 | 24.5 | 24.0 | 24.8 | 25.5 | 24.5 | 23.9 | 24.7 | 24.6 | 24.5 | 24.9 | -5.6 |
| Ex5p | 14.9 | 15.2 | 15.6 | 15.9 | 15.1 | 15.9 | 15.0 | 15.0 | 15.9 | 15.4 | 15.2 | 15.7 | 15.1 | 15.3 | 14.9 | 15.4 | 15.4 | 2.9 |
| Frisc | 30.4 | 30.5 | 30.2 | 29.6 | 30.3 | 29.6 | 29.4 | 29.1 | 29.1 | 28.9 | 29.0 | 29.3 | 29.5 | 29.0 | 29.3 | 28.6 | 29.1 | -4.1 |
| Img_calc | 39.5 | 38.9 | 38.3 | 38.2 | 38.2 | 37.5 | 37.4 | 37.3 | 36.8 | 36.0 | 35.9 | 35.7 | 35.6 | 35.2 | 35.3 | 35.3 | 35.2 | -10.9 |
| Img_interp | 22.4 | 22.1 | 21.3 | 21.9 | 20.6 | 20.7 | 20.5 | 21.4 | 20.7 | 20.5 | 20.5 | 20.8 | 20.3 | 20.8 | 20.1 | 20.7 | 20.7 | -7.6 |
| Input_chip | 15.4 | 15.8 | 15.5 | 14.9 | 14.7 | 14.6 | 14.8 | 14.6 | 14.7 | 14.3 | 14.3 | 14.3 | 14.0 | 14.2 | 14.1 | 14.0 | 14.0 | -9.2 |
| Misex3 | 15.3 | 14.7 | 15.0 | 14.8 | 15.1 | 14.6 | 14.2 | 14.4 | 14.7 | 14.7 | 14.7 | 14.5 | 14.5 | 14.5 | 14.7 | 14.6 | 14.6 | -4.8 |
| Pdc | 27.1 | 26.1 | 27.0 | 26.0 | 27.0 | 25.6 | 27.1 | 26.7 | 26.4 | 25.9 | 24.4 | 28.7 | 27.5 | 24.6 | 25.3 | 26.9 | 26.4 | -2.8 |
| Peak_chip | 18.1 | 17.9 | 17.9 | 17.9 | 17.2 | 17.2 | 17.4 | 16.8 | 16.6 | 16.8 | 16.3 | 16.6 | 16.5 | 16.6 | 16.9 | 16.5 | 16.8 | -7.4 |
| S298 | 32.0 | 32.2 | 32.5 | 30.4 | 29.4 | 30.6 | 31.0 | 30.5 | 29.6 | 30.1 | 29.4 | 30.8 | 30.4 | 30.1 | 30.7 | 30.5 | 30.1 | -5.8 |
| S38417 | 20.2 | 20.5 | 20.5 | 20.0 | 19.3 | 19.3 | 19.8 | 20.1 | 19.3 | 19.4 | 19.0 | 18.7 | 19.1 | 19.3 | 19.0 | 18.6 | 19.0 | -5.9 |
| S38584.1 | 15.2 | 15.5 | 15.4 | 15.3 | 15.0 | 15.1 | 15.1 | 15.0 | 14.9 | 15.0 | 14.6 | 15.0 | 15.3 | 15.3 | 14.8 | 15.1 | 14.9 | -1.8 |
| Scale125_chip | 24.3 | 23.7 | 23.4 | 23.0 | 22.7 | 23.1 | 22.4 | 22.6 | 22.3 | 21.9 | 22.4 | 22.2 | 22.0 | 22.3 | 22.1 | 21.8 | 22.0 | -9.5 |
| Scale2_chip | 18.8 | 18.7 | 18.6 | 17.9 | 17.8 | 17.8 | 17.8 | 17.5 | 17.5 | 17.4 | 17.1 | 17.6 | 17.3 | 17.0 | 17.0 | 17.3 | 17.3 | -8.2 |
| Seq | 15.8 | 16.0 | 15.1 | 15.3 | 15.6 | 15.1 | 15.8 | 15.7 | 15.8 | 15.6 | 15.5 | 15.9 | 15.4 | 15.3 | 15.5 | 15.4 | 14.7 | -7.0 |
| Spla | 22.9 | 22.7 | 23.0 | 22.8 | 23.4 | 24.1 | 22.6 | 22.3 | 23.7 | 22.6 | 21.8 | 23.2 | 22.5 | 23.7 | 22.1 | 23.5 | 20.8 | -9.0 |
| Tseng | 18.2 | 17.8 | 17.5 | 17.3 | 16.9 | 16.6 | 16.5 | 16.4 | 16.0 | 16.1 | 15.7 | 15.7 | 16.0 | 15.9 | 15.7 | 15.6 | 15.6 | -14.1 |
| Warping | 11.7 | 11.9 | 11.4 | 11.4 | 11.2 | 11.1 | 11.1 | 11.0 | 11.0 | 10.9 | 10.6 | 10.8 | 10.9 | 10.9 | 10.9 | 10.7 | 10.8 | -7.8 |
| **Geometric Avg** | 18.8 | 18.8 | 18.7 | 18.5 | 18.3 | 18.2 | 18.2 | 18.2 | 18.2 | 18.1 | 17.9 | 18.1 | 18.0 | 17.9 | 17.8 | 17.9 | 17.8 | -5.7 |

*Table A.1 – Delay vs # of NN Interconnects for Manhattan Radius 1*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 22.4 | 22.5 | 22.5 | 22.5 | 22.6 | 22.6 | 22.7 | 22.7 | 22.8 | 22.8 | 22.8 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 23.1 | 2.9 |
| Apex2 | 32.9 | 33.0 | 33.0 | 33.1 | 33.2 | 33.2 | 33.3 | 33.3 | 33.4 | 33.4 | 33.5 | 33.5 | 33.6 | 33.7 | 33.7 | 33.8 | 33.8 | 2.7 |
| Apex4 | 22.6 | 22.6 | 22.7 | 22.7 | 22.7 | 22.8 | 22.8 | 22.8 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 23.1 | 23.1 | 23.1 | 23.2 | 2.6 |
| Bigkey | 26.6 | 26.6 | 26.7 | 26.8 | 26.9 | 27.0 | 27.0 | 27.1 | 27.2 | 27.3 | 27.3 | 27.4 | 27.5 | 27.6 | 27.6 | 27.7 | 27.8 | 4.6 |
| Clma | 152.1 | 152.5 | 152.8 | 153.2 | 153.6 | 153.9 | 154.3 | 154.7 | 155.0 | 155.4 | 155.8 | 156.0 | 156.2 | 156.5 | 156.7 | 156.9 | 157.2 | 3.3 |
| Des | 35.3 | 35.4 | 35.5 | 35.6 | 35.7 | 35.8 | 35.9 | 36.0 | 36.1 | 36.3 | 36.4 | 36.5 | 36.7 | 36.9 | 37.0 | 37.2 | 37.4 | 5.9 |
| Diffeq | 19.9 | 19.9 | 20.0 | 20.0 | 20.1 | 20.1 | 20.1 | 20.2 | 20.2 | 20.3 | 20.3 | 20.4 | 20.4 | 20.4 | 20.5 | 20.5 | 20.6 | 3.3 |
| Display_chip | 20.5 | 20.5 | 20.6 | 20.6 | 20.7 | 20.7 | 20.7 | 20.8 | 20.8 | 20.9 | 20.9 | 21.0 | 21.0 | 21.1 | 21.1 | 21.2 | 21.2 | 3.9 |
| Dsip | 26.2 | 26.2 | 26.3 | 26.4 | 26.5 | 26.5 | 26.6 | 26.7 | 26.8 | 26.8 | 26.9 | 27.0 | 27.2 | 27.3 | 27.4 | 27.5 | 27.6 | 5.6 |
| Elliptic | 58.9 | 59.0 | 59.1 | 59.2 | 59.3 | 59.4 | 59.5 | 59.6 | 59.7 | 59.8 | 59.9 | 60.0 | 60.1 | 60.2 | 60.3 | 60.4 | 60.5 | 2.7 |
| Ex1010 | 76.6 | 76.7 | 76.8 | 77.0 | 77.1 | 77.2 | 77.4 | 77.5 | 77.6 | 77.7 | 77.9 | 78.0 | 78.1 | 78.3 | 78.4 | 78.5 | 78.6 | 2.7 |
| Ex5p | 18.5 | 18.5 | 18.5 | 18.6 | 18.6 | 18.6 | 18.7 | 18.7 | 18.7 | 18.8 | 18.8 | 18.8 | 18.8 | 18.9 | 18.9 | 18.9 | 19.0 | 2.5 |
| Frisc | 60.4 | 60.5 | 60.5 | 60.6 | 60.7 | 60.8 | 60.9 | 61.0 | 61.1 | 61.2 | 61.3 | 61.4 | 61.5 | 61.6 | 61.7 | 61.8 | 61.9 | 2.5 |
| Img_calc | 152.4 | 152.7 | 153.0 | 153.3 | 153.5 | 153.8 | 154.1 | 154.4 | 154.6 | 154.9 | 155.2 | 155.5 | 155.7 | 156.0 | 156.3 | 156.6 | 156.8 | 2.9 |
| Img_interp | 32.5 | 32.6 | 32.7 | 32.9 | 33.0 | 33.1 | 33.2 | 33.3 | 33.5 | 33.6 | 33.7 | 33.8 | 33.8 | 33.9 | 34.0 | 34.1 | 34.2 | 5.0 |
| Input_chip | 8.8 | 8.8 | 8.9 | 8.9 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 9.1 | 9.1 | 9.2 | 9.2 | 4.1 |
| Misex3 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 23.1 | 23.1 | 23.2 | 23.2 | 23.3 | 23.3 | 23.3 | 23.4 | 23.4 | 23.5 | 23.5 | 23.5 | 2.9 |
| Pdc | 97.8 | 98.0 | 98.1 | 98.2 | 98.4 | 98.5 | 98.6 | 98.7 | 98.9 | 99.0 | 99.1 | 99.3 | 99.4 | 99.5 | 99.6 | 99.8 | 99.9 | 2.1 |
| Peak_chip | 8.4 | 8.4 | 8.5 | 8.5 | 8.5 | 8.5 | 8.6 | 8.6 | 8.6 | 8.6 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.8 | 8.8 | 4.3 |
| S298 | 25.2 | 25.3 | 25.3 | 25.4 | 25.4 | 25.5 | 25.6 | 25.6 | 25.7 | 25.7 | 25.8 | 25.8 | 25.9 | 25.9 | 26.0 | 26.0 | 26.1 | 3.5 |
| S38417 | 93.7 | 93.9 | 94.1 | 94.2 | 94.4 | 94.6 | 94.8 | 95.0 | 95.1 | 95.3 | 95.5 | 95.7 | 95.8 | 96.0 | 96.2 | 96.4 | 96.5 | 3.0 |
| S38584.1 | 89.4 | 89.6 | 89.8 | 90.0 | 90.1 | 90.3 | 90.5 | 90.7 | 90.9 | 91.0 | 91.2 | 91.4 | 91.6 | 91.7 | 91.9 | 92.1 | 92.3 | 3.2 |
| Scale125_chip | 29.5 | 29.5 | 29.6 | 29.7 | 29.7 | 29.8 | 29.9 | 30.0 | 30.0 | 30.1 | 30.2 | 30.3 | 30.4 | 30.5 | 30.6 | 30.7 | 30.8 | 4.6 |
| Scale2_chip | 12.6 | 12.6 | 12.7 | 12.7 | 12.7 | 12.7 | 12.8 | 12.8 | 12.8 | 12.9 | 12.9 | 12.9 | 13.0 | 13.0 | 13.0 | 13.1 | 13.1 | 4.2 |
| Seq | 29.0 | 29.1 | 29.1 | 29.2 | 29.2 | 29.3 | 29.3 | 29.4 | 29.4 | 29.5 | 29.5 | 29.6 | 29.6 | 29.7 | 29.7 | 29.8 | 29.8 | 2.8 |
| Spla | 70.3 | 70.4 | 70.5 | 70.6 | 70.7 | 70.8 | 70.9 | 71.0 | 71.1 | 71.2 | 71.3 | 71.4 | 71.5 | 71.6 | 71.7 | 71.8 | 71.9 | 2.3 |
| Tseng | 13.8 | 13.9 | 13.9 | 13.9 | 14.0 | 14.0 | 14.0 | 14.0 | 14.1 | 14.1 | 14.1 | 14.2 | 14.2 | 14.2 | 14.3 | 14.3 | 14.3 | 3.4 |
| Warping | 15.1 | 15.2 | 15.2 | 15.3 | 15.3 | 15.3 | 15.4 | 15.4 | 15.4 | 15.5 | 15.5 | 15.5 | 15.6 | 15.6 | 15.7 | 15.7 | 15.7 | 3.9 |
| **Geometric Avg** | 33.1 | 33.1 | 33.2 | 33.3 | 33.4 | 33.4 | 33.5 | 33.6 | 33.6 | 33.7 | 33.8 | 33.9 | 33.9 | 34.0 | 34.1 | 34.2 | 34.2 | 3.5 |

*Table A.2 – Area vs # of NN Interconnects for Manhattan Radius 1 (Measured Under Constant Track Count)*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 16.3 | 15.4 | 15.6 | 15.0 | 15.2 | 15.6 | 15.2 | 15.7 | 15.4 | 15.1 | 15.2 | 15.3 | 15.4 | 15.3 | 15.1 | 15.9 | 1.3 |
| Apex2 | 17.0 | 16.8 | 17.0 | 17.9 | 17.1 | 17.0 | 17.1 | 17.2 | 17.4 | 17.4 | 17.1 | 17.2 | 17.2 | 16.7 | 16.8 | 17.0 | 17.0 | 0.1 |
| Apex4 | 15.8 | 15.3 | 16.0 | 15.3 | 16.4 | 15.3 | 15.7 | 15.5 | 15.7 | 15.2 | 16.0 | 15.4 | 15.9 | 15.1 | 15.7 | 15.7 | 16.3 | 3.3 |
| Bigkey | 8.8 | 9.1 | 9.1 | 8.8 | 9.6 | 8.9 | 9.7 | 9.0 | 8.7 | 8.9 | 8.7 | 8.9 | 9.2 | 8.8 | 8.3 | 8.8 | 8.7 | -1.6 |
| Clma | 34.2 | 33.9 | 33.7 | 33.7 | 33.4 | 34.5 | 33.8 | 33.4 | 33.2 | 34.3 | 33.3 | 33.0 | 34.5 | 33.9 | 35.6 | 33.6 | 34.8 | 1.7 |
| Des | 15.6 | 15.5 | 15.5 | 15.1 | 16.0 | 15.5 | 15.3 | 15.4 | 15.5 | 15.2 | 15.5 | 15.4 | 15.6 | 15.5 | 15.4 | 15.2 | 15.6 | 0.0 |
| Diffeq | 18.2 | 17.8 | 17.8 | 17.6 | 17.2 | 17.2 | 17.0 | 17.1 | 16.9 | 16.8 | 17.0 | 16.6 | 16.8 | 16.5 | 16.4 | 16.8 | 16.7 | -8.3 |
| Display_chip | 16.6 | 16.4 | 16.3 | 16.2 | 16.0 | 16.3 | 16.1 | 15.9 | 16.4 | 16.1 | 15.9 | 16.0 | 16.3 | 16.0 | 16.0 | 15.8 | 16.1 | -3.4 |
| Dsip | 8.0 | 7.9 | 8.0 | 7.9 | 7.8 | 8.2 | 8.1 | 8.3 | 8.0 | 7.8 | 8.2 | 7.9 | 7.9 | 8.0 | 7.9 | 7.8 | 7.8 | -2.4 |
| Elliptic | 24.6 | 25.5 | 25.7 | 24.8 | 24.4 | 24.6 | 25.5 | 24.3 | 24.7 | 25.0 | 25.3 | 25.3 | 24.7 | 26.0 | 25.5 | 25.0 | 24.9 | 1.1 |
| Ex1010 | 26.3 | 25.8 | 26.8 | 26.0 | 24.9 | 25.3 | 26.0 | 25.3 | 25.2 | 25.5 | 25.6 | 26.2 | 26.0 | 25.5 | 25.2 | 26.4 | 26.9 | 2.0 |
| Ex5p | 14.9 | 15.7 | 15.4 | 15.5 | 15.2 | 15.7 | 15.3 | 15.3 | 15.4 | 15.4 | 15.3 | 16.0 | 15.1 | 15.0 | 15.3 | 15.3 | 15.3 | 2.2 |
| Frisc | 30.4 | 29.9 | 30.1 | 29.3 | 29.7 | 29.7 | 29.7 | 29.2 | 29.5 | 29.3 | 29.4 | 29.5 | 29.4 | 29.5 | 29.6 | 29.3 | 29.9 | -1.4 |
| Img_calc | 39.5 | 39.0 | 38.8 | 38.7 | 38.7 | 38.0 | 38.0 | 38.0 | 38.3 | 37.4 | 37.4 | 37.3 | 37.3 | 37.0 | 36.6 | 36.5 | 37.0 | -6.4 |
| Img_interp | 22.4 | 22.2 | 21.8 | 21.5 | 21.0 | 21.2 | 21.3 | 21.5 | 21.1 | 21.0 | 20.7 | 21.1 | 21.2 | 21.2 | 21.0 | 21.0 | 21.1 | -6.1 |
| Input_chip | 15.4 | 15.2 | 14.8 | 14.8 | 14.3 | 14.2 | 14.2 | 13.9 | 14.0 | 14.3 | 13.9 | 13.8 | 13.9 | 13.7 | 13.9 | 13.9 | 14.0 | -9.1 |
| Misex3 | 15.3 | 15.1 | 14.7 | 14.4 | 14.5 | 14.7 | 15.0 | 14.4 | 14.9 | 14.6 | 14.6 | 14.6 | 14.6 | 14.5 | 14.5 | 14.6 | 14.5 | -5.1 |
| Pdc | 27.1 | 26.8 | 26.1 | 26.7 | 27.6 | 27.8 | 28.1 | 26.2 | 26.6 | 28.1 | 27.8 | 27.3 | 26.6 | 27.1 | 26.9 | 26.2 | 26.8 | -1.2 |
| Peak_chip | 18.1 | 17.8 | 17.9 | 18.0 | 17.6 | 18.0 | 17.7 | 17.5 | 17.3 | 17.8 | 17.6 | 17.4 | 17.3 | 17.2 | 17.2 | 17.3 | 17.4 | -3.9 |
| S298 | 32.0 | 30.5 | 32.0 | 31.1 | 30.1 | 30.9 | 32.2 | 29.4 | 29.7 | 31.6 | 30.9 | 30.0 | 31.1 | 32.0 | 31.0 | 32.2 | 30.4 | -5.1 |
| S38417 | 20.2 | 19.9 | 20.6 | 20.4 | 20.2 | 20.8 | 20.3 | 20.3 | 20.4 | 20.1 | 20.6 | 19.8 | 19.7 | 19.6 | 20.0 | 19.4 | 20.5 | 1.5 |
| S38584.1 | 15.2 | 15.0 | 15.3 | 15.0 | 14.9 | 15.3 | 14.8 | 14.9 | 14.8 | 14.9 | 14.9 | 15.1 | 14.8 | 14.8 | 14.9 | 15.1 | 14.9 | -1.7 |
| Scale125_chip | 24.3 | 23.9 | 23.4 | 23.3 | 23.4 | 22.7 | 23.2 | 22.9 | 22.9 | 23.1 | 23.2 | 23.0 | 22.9 | 22.7 | 22.6 | 22.9 | 22.9 | -6.0 |
| Scale2_chip | 18.8 | 17.9 | 18.3 | 18.1 | 18.1 | 18.1 | 18.0 | 17.7 | 18.1 | 17.6 | 17.9 | 17.8 | 17.6 | 17.3 | 17.7 | 17.4 | 17.4 | -7.6 |
| Seq | 15.8 | 15.7 | 15.7 | 15.3 | 15.6 | 15.7 | 15.6 | 15.3 | 15.2 | 14.9 | 14.6 | 15.3 | 15.7 | 14.8 | 15.2 | 15.6 | 15.9 | 0.3 |
| Spla | 22.9 | 21.5 | 23.0 | 22.5 | 21.8 | 22.7 | 22.6 | 22.9 | 23.0 | 22.2 | 23.3 | 23.1 | 21.5 | 22.6 | 25.9 | 22.0 | 21.5 | -6.0 |
| Tseng | 18.2 | 18.4 | 18.1 | 17.8 | 17.7 | 17.9 | 17.4 | 17.4 | 17.1 | 17.3 | 17.2 | 17.2 | 17.3 | 17.2 | 17.2 | 16.9 | 16.8 | -7.5 |
| Warping | 11.7 | 11.5 | 11.5 | 11.5 | 11.8 | 11.3 | 11.5 | 11.4 | 11.3 | 11.6 | 11.1 | 11.2 | 11.4 | 11.5 | 11.3 | 11.4 | 11.2 | -4.6 |
| **Geometric Avg** | 18.8 | 18.6 | 18.7 | 18.5 | 18.5 | 18.5 | 18.6 | 18.3 | 18.3 | 18.4 | 18.3 | 18.3 | 18.3 | 18.2 | 18.3 | 18.2 | 18.3 | -2.7 |

*Table A.3 – Delay vs # of NN Interconnects for Manhattan Radius 1 Using Architecture-Oblivious Placement*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 15.3 | 15.2 | 15.5 | 15.3 | 15.2 | 14.7 | 15.2 | 15.5 | 15.3 | 15.2 | 15.2 | 15.2 | 15.2 | 15.1 | 15.5 | 15.0 | -4.4 |
| Apex2 | 17.0 | 17.3 | 17.1 | 17.5 | 16.9 | 17.3 | 17.4 | 17.2 | 16.8 | 16.6 | 16.9 | 17.6 | 17.2 | 17.1 | 17.0 | 17.1 | 17.0 | -0.1 |
| Apex4 | 15.8 | 15.8 | 15.3 | 15.6 | 15.4 | 15.9 | 15.6 | 15.2 | 15.2 | 15.6 | 15.9 | 15.5 | 15.3 | 15.3 | 15.2 | 14.8 | 15.4 | -2.6 |
| Bigkey | 8.8 | 9.0 | 8.7 | 8.6 | 8.5 | 9.0 | 8.8 | 8.6 | 8.7 | 8.8 | 8.5 | 8.5 | 8.6 | 8.5 | 8.6 | 8.4 | 8.2 | -7.3 |
| Clma | 34.2 | 32.8 | 34.9 | 34.9 | 33.7 | 33.9 | 35.3 | 33.4 | 33.3 | 34.1 | 34.0 | 33.3 | 32.4 | 34.2 | 33.5 | 33.8 | 33.5 | -2.3 |
| Des | 15.6 | 15.7 | 15.3 | 15.6 | 15.8 | 15.5 | 15.2 | 14.8 | 15.6 | 15.0 | 14.8 | 15.0 | 15.2 | 15.1 | 14.9 | 15.1 | 15.4 | -1.5 |
| Diffeq | 18.2 | 18.5 | 17.5 | 17.3 | 17.1 | 16.9 | 16.7 | 16.6 | 16.6 | 16.4 | 16.8 | 16.4 | 16.1 | 16.1 | 16.0 | 16.1 | 15.9 | -12.6 |
| Display_chip | 16.6 | 16.8 | 16.7 | 16.5 | 16.4 | 16.4 | 15.9 | 15.7 | 16.2 | 15.9 | 15.9 | 15.7 | 15.7 | 15.6 | 16.1 | 15.7 | 15.5 | -6.8 |
| Dsip | 8.0 | 8.2 | 8.1 | 8.2 | 8.1 | 8.2 | 8.5 | 8.1 | 8.6 | 7.9 | 8.2 | 7.9 | 8.1 | 8.3 | 8.1 | 8.0 | 8.2 | 1.9 |
| Elliptic | 24.6 | 26.0 | 25.8 | 24.5 | 24.9 | 24.8 | 25.0 | 24.4 | 23.5 | 24.4 | 25.1 | 24.3 | 25.2 | 23.9 | 25.4 | 24.8 | 23.6 | -4.3 |
| Ex1010 | 26.3 | 25.1 | 26.0 | 24.2 | 24.6 | 24.6 | 25.9 | 24.5 | 24.4 | 24.1 | 24.7 | 24.9 | 24.4 | 24.0 | 24.4 | 24.6 | 25.3 | -3.9 |
| Ex5p | 14.9 | 15.2 | 15.6 | 15.9 | 15.1 | 15.4 | 15.0 | 15.6 | 15.6 | 15.7 | 15.0 | 15.6 | 15.1 | 15.7 | 15.4 | 15.3 | 15.3 | 2.0 |
| Frisc | 30.4 | 30.5 | 30.2 | 29.6 | 30.3 | 29.7 | 29.2 | 29.8 | 29.2 | 29.1 | 28.6 | 29.0 | 28.2 | 28.2 | 28.7 | 28.6 | 28.3 | -6.7 |
| Img_calc | 39.5 | 38.9 | 38.3 | 38.2 | 38.2 | 38.0 | 36.8 | 36.8 | 35.6 | 35.4 | 35.2 | 35.1 | 35.1 | 35.3 | 34.9 | 35.0 | 34.8 | -11.9 |
| Img_interp | 22.4 | 22.1 | 21.3 | 21.9 | 20.6 | 20.6 | 20.9 | 20.8 | 20.9 | 20.3 | 20.5 | 20.7 | 20.4 | 20.5 | 20.7 | 20.4 | 20.5 | -8.6 |
| Input_chip | 15.4 | 15.8 | 15.5 | 14.9 | 14.7 | 14.8 | 14.8 | 14.5 | 14.6 | 14.3 | 14.1 | 14.1 | 13.9 | 13.9 | 14.0 | 13.9 | 13.7 | -10.5 |
| Misex3 | 15.3 | 14.7 | 15.0 | 14.8 | 15.1 | 14.5 | 14.2 | 15.1 | 14.7 | 14.5 | 14.5 | 14.4 | 14.6 | 14.8 | 14.9 | 15.1 | 14.7 | -4.2 |
| Pdc | 27.1 | 26.1 | 27.0 | 26.0 | 27.0 | 26.8 | 26.6 | 25.0 | 27.4 | 25.9 | 25.3 | 26.4 | 26.7 | 25.6 | 26.5 | 25.7 | 26.3 | -3.0 |
| Peak_chip | 18.1 | 17.9 | 17.9 | 17.9 | 17.2 | 17.2 | 17.1 | 16.8 | 16.9 | 16.4 | 16.8 | 16.4 | 16.3 | 16.6 | 16.8 | 16.4 | 16.4 | -9.6 |
| S298 | 32.0 | 32.2 | 32.5 | 30.4 | 29.4 | 29.7 | 30.6 | 30.3 | 29.8 | 30.4 | 30.2 | 30.5 | 29.5 | 30.0 | 30.9 | 30.5 | 29.5 | -7.7 |
| S38417 | 20.2 | 20.5 | 20.5 | 20.0 | 19.3 | 20.3 | 19.5 | 20.4 | 19.4 | 19.1 | 19.5 | 19.1 | 19.3 | 19.3 | 18.5 | 19.0 | 19.3 | -4.2 |
| S38584.1 | 15.2 | 15.5 | 15.4 | 15.3 | 15.0 | 15.1 | 14.7 | 15.1 | 15.1 | 15.0 | 14.9 | 14.8 | 14.8 | 14.6 | 14.9 | 14.5 | 14.9 | -2.0 |
| Scale125_chip | 24.3 | 23.7 | 23.4 | 23.0 | 22.7 | 22.7 | 22.4 | 22.4 | 22.2 | 22.4 | 22.6 | 22.3 | 21.6 | 21.9 | 22.1 | 22.2 | 22.0 | -9.7 |
| Scale2_chip | 18.8 | 18.7 | 18.6 | 17.9 | 17.8 | 18.0 | 17.8 | 17.9 | 17.5 | 17.4 | 17.1 | 17.4 | 17.2 | 17.2 | 16.9 | 17.1 | 16.9 | -10.0 |
| Seq | 15.8 | 16.0 | 15.1 | 15.3 | 15.6 | 15.0 | 15.7 | 15.4 | 15.2 | 15.0 | 15.0 | 15.3 | 15.4 | 15.1 | 15.3 | 15.3 | 15.4 | -2.7 |
| Spla | 22.9 | 22.7 | 23.0 | 22.8 | 23.4 | 20.9 | 21.2 | 22.5 | 23.3 | 22.2 | 22.5 | 21.7 | 21.9 | 22.1 | 21.6 | 23.3 | 21.5 | -5.9 |
| Tseng | 18.2 | 17.8 | 17.5 | 17.3 | 16.9 | 16.5 | 16.5 | 16.2 | 15.8 | 16.2 | 16.1 | 15.9 | 15.6 | 15.5 | 15.8 | 15.8 | 15.6 | -14.3 |
| Warping | 11.7 | 11.9 | 11.4 | 11.4 | 11.2 | 11.3 | 11.2 | 11.0 | 10.8 | 11.0 | 10.8 | 10.7 | 10.8 | 10.9 | 10.8 | 10.6 | 10.8 | -8.3 |
| **Geometric Avg** | 18.8 | 18.8 | 18.7 | 18.5 | 18.3 | 18.3 | 18.2 | 18.1 | 18.1 | 17.9 | 17.9 | 17.9 | 17.8 | 17.8 | 17.9 | 17.8 | 17.7 | -5.8 |

*Table A.4 – Delay vs # of NN Interconnect for Manhattan Radius 1 Using Alternative 180-Degree Output Fan-out Pattern*

| Circuit | Number of Short Connections On Critical Path That Fall Within NN Architecture | | | | | | | | | | | | | | | | Avg # of Connections Per Circuit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 0.4 | 0.6 | 0.6 | 0.6 | 0.6 | 0.2 | 0.2 | 0.2 | 0.4 | 0.8 | 0.8 | 0.0 | 0.6 | 0.4 | 0.6 | 0.4 | 0.5 |
| Apex2 | 0.8 | 1.0 | 1.2 | 0.8 | 0.8 | 0.6 | 1.0 | 0.4 | 0.4 | 0.4 | 1.2 | 0.6 | 0.4 | 0.6 | 0.4 | 0.4 | 0.7 |
| Apex4 | 0.6 | 1.0 | 0.6 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.0 | 0.4 | 0.0 | 0.0 | 0.0 | 0.3 |
| Bigkey | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Clma | 2.4 | 0.8 | 1.4 | 1.6 | 1.8 | 1.0 | 1.6 | 1.2 | 2.0 | 1.8 | 1.0 | 1.6 | 1.2 | 1.2 | 1.4 | 1.4 | 1.5 |
| Des | 0.8 | 0.8 | 0.6 | 0.4 | 0.8 | 1.0 | 0.8 | 1.0 | 0.8 | 0.6 | 0.4 | 0.8 | 0.6 | 0.8 | 0.6 | 0.4 | 0.7 |
| Diffeq | 6.6 | 5.8 | 6.2 | 6.2 | 6.0 | 6.6 | 6.4 | 6.0 | 6.0 | 6.4 | 5.6 | 4.8 | 6.2 | 5.0 | 4.2 | 5.0 | 5.8 |
| Display_chip | 2.8 | 2.6 | 3.0 | 2.2 | 2.4 | 2.8 | 2.0 | 2.0 | 1.6 | 2.2 | 1.6 | 1.8 | 1.8 | 1.6 | 1.8 | 1.4 | 2.1 |
| Dsip | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.1 |
| Elliptic | 2.0 | 2.0 | 1.6 | 1.6 | 1.0 | 1.6 | 1.6 | 1.4 | 2.2 | 1.8 | 1.8 | 1.2 | 0.8 | 1.4 | 1.4 | 1.0 | 1.5 |
| Ex1010 | 0.2 | 0.0 | 0.4 | 0.2 | 0.4 | 0.0 | 0.2 | 0.6 | 0.4 | 0.4 | 0.4 | 0.6 | 0.4 | 0.0 | 0.4 | 0.4 | 0.3 |
| Ex5p | 0.4 | 0.6 | 1.4 | 0.2 | 0.4 | 0.8 | 0.6 | 0.4 | 0.0 | 0.4 | 0.6 | 0.4 | 1.0 | 0.2 | 0.6 | 0.6 | 0.5 |
| Frisc | 5.0 | 5.6 | 4.6 | 4.4 | 4.4 | 5.6 | 3.0 | 3.2 | 3.4 | 3.0 | 1.6 | 3.2 | 2.4 | 2.2 | 1.6 | 1.2 | 3.4 |
| Img_calc | 11.0 | 11.2 | 10.6 | 10.4 | 9.6 | 9.0 | 10.2 | 9.4 | 9.8 | 9.8 | 10.0 | 6.2 | 8.4 | 9.6 | 8.4 | 8.2 | 9.5 |
| Img_interp | 3.8 | 3.4 | 2.8 | 3.0 | 3.2 | 2.6 | 3.0 | 2.6 | 2.4 | 2.6 | 3.0 | 2.6 | 2.4 | 2.6 | 3.2 | 2.0 | 2.8 |
| Input_chip | 4.0 | 4.0 | 3.4 | 3.2 | 3.2 | 2.6 | 3.6 | 3.2 | 3.0 | 3.6 | 3.4 | 3.8 | 2.8 | 2.6 | 3.0 | 3.2 | 3.3 |
| Misex3 | 0.4 | 0.0 | 0.6 | 0.2 | 0.2 | 0.0 | 0.6 | 0.6 | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.6 | 0.2 | 0.6 | 0.3 |
| Pdc | 0.6 | 0.6 | 0.2 | 0.2 | 0.8 | 0.2 | 0.6 | 0.6 | 0.4 | 0.2 | 0.6 | 0.0 | 1.0 | 0.2 | 0.0 | 0.2 | 0.4 |
| Peak_chip | 4.2 | 4.0 | 3.6 | 3.4 | 3.4 | 2.8 | 3.4 | 3.0 | 3.2 | 3.4 | 3.4 | 3.4 | 3.4 | 3.2 | 2.8 | 3.2 | 3.4 |
| S298 | 3.0 | 1.8 | 1.4 | 1.4 | 1.2 | 1.0 | 0.6 | 1.4 | 1.2 | 0.8 | 1.2 | 1.4 | 0.8 | 1.2 | 0.2 | 0.6 | 1.2 |
| S38417 | 3.8 | 3.2 | 2.6 | 2.2 | 3.2 | 2.4 | 2.0 | 2.6 | 1.8 | 1.8 | 1.6 | 2.2 | 2.4 | 2.4 | 2.0 | 2.0 | 2.4 |
| S38584.1 | 0.8 | 1.6 | 1.2 | 0.4 | 0.6 | 0.8 | 1.4 | 0.8 | 1.0 | 1.0 | 0.8 | 0.6 | 0.4 | 0.4 | 1.0 | 0.2 | 0.8 |
| Scale125_chip | 4.4 | 4.4 | 4.0 | 4.6 | 3.8 | 4.0 | 3.4 | 3.2 | 3.4 | 3.0 | 3.2 | 2.6 | 3.0 | 3.4 | 2.6 | 2.6 | 3.5 |
| Scale2_chip | 3.6 | 3.8 | 3.6 | 4.2 | 3.6 | 3.6 | 3.4 | 3.0 | 3.0 | 2.6 | 2.6 | 2.6 | 3.2 | 2.6 | 3.2 | 3.0 | 3.2 |
| Seq | 0.8 | 0.4 | 0.0 | 0.6 | 0.0 | 0.4 | 0.2 | 0.4 | 0.4 | 0.4 | 0.4 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.3 |
| Spla | 0.2 | 0.6 | 0.6 | 0.4 | 0.6 | 0.6 | 0.4 | 0.6 | 0.6 | 0.2 | 0.6 | 0.4 | 0.0 | 0.2 | 0.0 | 0.0 | 0.4 |
| Tseng | 7.0 | 5.8 | 5.4 | 5.6 | 4.6 | 6.2 | 5.2 | 4.8 | 4.4 | 4.0 | 4.4 | 3.4 | 4.0 | 4.4 | 4.4 | 4.0 | 4.9 |
| Warping | 2.2 | 2.0 | 2.0 | 1.6 | 1.4 | 1.6 | 2.0 | 2.0 | 1.8 | 1.4 | 1.6 | 1.6 | 1.6 | 2.0 | 1.8 | 1.6 | 1.8 |
| **Arithmetic Avg** | 2.6 | 2.4 | 2.3 | 2.1 | 2.1 | 2.1 | 2.1 | 2.0 | 1.9 | 1.9 | 1.9 | 1.6 | 1.8 | 1.8 | 1.7 | 1.6 | 2.0 |

*Table A.5 – Number of Short Connections on Critical Path for Manhattan Radius 1 Using Architecture-Aware Placement*

| Circuit | Number of Short Connections On Critical Path That Fall Within NN Architecture | | | | | | | | | | | | | | | | Avg # of Connections Per Circuit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 | 0.2 | 0.0 | 0.2 | 0.0 | 0.0 | 0.2 | 0.4 | 0.2 |
| Apex2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.4 | 0.0 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.6 | 0.2 | 0.0 | 0.0 | 0.1 |
| Apex4 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.1 |
| Bigkey | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Clma | 0.6 | 0.4 | 0.4 | 0.4 | 0.4 | 0.2 | 0.0 | 0.0 | 0.8 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 |
| Des | 0.2 | 0.4 | 0.0 | 0.4 | 0.6 | 0.2 | 0.4 | 0.0 | 0.4 | 0.0 | 0.8 | 0.4 | 0.0 | 0.0 | 0.2 | 0.0 | 0.3 |
| Diffeq | 6.0 | 5.4 | 4.8 | 4.8 | 5.0 | 5.0 | 4.4 | 3.6 | 4.4 | 4.6 | 3.8 | 4.4 | 3.0 | 4.2 | 2.4 | 2.8 | 4.3 |
| Display_chip | 2.2 | 2.0 | 1.2 | 0.8 | 1.2 | 0.8 | 1.4 | 2.2 | 1.0 | 1.6 | 1.0 | 1.4 | 1.4 | 1.0 | 1.2 | 0.4 | 1.3 |
| Dsip | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 |
| Elliptic | 0.6 | 0.2 | 0.4 | 0.2 | 0.2 | 0.0 | 0.4 | 0.2 | 0.6 | 0.0 | 0.4 | 0.4 | 0.0 | 0.2 | 0.6 | 0.2 | 0.3 |
| Ex1010 | 0.2 | 0.0 | 0.2 | 0.0 | 0.2 | 0.4 | 0.0 | 0.2 | 0.0 | 0.0 | 0.4 | 0.2 | 0.0 | 0.0 | 0.2 | 0.0 | 0.1 |
| Ex5p | 0.4 | 0.2 | 0.6 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.6 | 0.0 | 0.4 | 0.4 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 |
| Frisc | 1.8 | 2.0 | 1.2 | 1.4 | 1.6 | 1.6 | 2.2 | 1.4 | 1.2 | 1.2 | 1.4 | 1.4 | 0.6 | 0.6 | 0.8 | 0.6 | 1.3 |
| Img_calc | 7.8 | 6.2 | 8.6 | 7.0 | 6.6 | 4.6 | 7.6 | 6.2 | 6.2 | 7.6 | 5.6 | 5.8 | 5.6 | 6.2 | 6.0 | 6.4 | 6.5 |
| Img_interp | 2.0 | 1.6 | 1.4 | 2.0 | 1.8 | 1.4 | 1.6 | 1.0 | 1.4 | 1.4 | 1.8 | 1.4 | 1.8 | 1.0 | 2.0 | 1.2 | 1.6 |
| Input_chip | 4.4 | 3.6 | 2.4 | 2.2 | 2.4 | 2.6 | 2.0 | 2.0 | 2.4 | 2.6 | 2.6 | 2.2 | 1.6 | 3.0 | 3.2 | 2.6 | 2.6 |
| Misex3 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.0 | 0.4 | 0.0 | 0.4 | 0.2 | 0.2 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.1 |
| Pdc | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.4 | 0.0 | 0.1 |
| Peak_chip | 2.2 | 1.6 | 2.0 | 1.6 | 1.0 | 1.0 | 1.4 | 1.4 | 1.2 | 1.2 | 1.4 | 1.6 | 1.0 | 1.6 | 1.0 | 1.2 | 1.4 |
| S298 | 0.8 | 0.6 | 0.8 | 0.6 | 0.2 | 0.0 | 1.0 | 0.2 | 0.2 | 0.4 | 0.4 | 0.0 | 0.6 | 0.2 | 0.2 | 0.4 | 0.4 |
| S38417 | 1.6 | 1.4 | 1.0 | 0.6 | 0.6 | 0.4 | 1.2 | 1.2 | 0.8 | 0.4 | 0.6 | 0.6 | 0.6 | 0.6 | 0.6 | 0.2 | 0.8 |
| S38584.1 | 0.6 | 0.0 | 0.4 | 0.4 | 0.2 | 0.0 | 0.4 | 0.4 | 0.4 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 |
| Scale125_chip | 3.2 | 2.6 | 2.6 | 3.0 | 2.4 | 3.2 | 2.0 | 2.8 | 1.8 | 2.0 | 1.8 | 1.8 | 1.6 | 1.8 | 1.2 | 1.4 | 2.2 |
| Scale2_chip | 2.2 | 2.6 | 2.2 | 2.4 | 2.0 | 2.0 | 2.6 | 1.4 | 1.0 | 2.0 | 1.4 | 2.2 | 1.2 | 1.8 | 1.2 | 1.4 | 1.9 |
| Seq | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.2 | 0.4 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.1 |
| Spla | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.6 | 0.0 | 0.2 | 0.4 | 0.1 |
| Tseng | 2.8 | 3.2 | 2.2 | 2.6 | 1.8 | 1.8 | 1.8 | 1.6 | 2.0 | 1.8 | 1.6 | 2.0 | 1.6 | 1.8 | 2.0 | 1.6 | 2.0 |
| Warping | 1.0 | 0.6 | 0.4 | 0.4 | 0.8 | 0.6 | 0.4 | 0.6 | 0.4 | 0.2 | 0.2 | 0.4 | 0.4 | 0.4 | 0.2 | 0.2 | 0.5 |
| **Arithmetic Avg** | 1.5 | 1.3 | 1.2 | 1.1 | 1.1 | 1.0 | 1.2 | 1.0 | 1.0 | 1.0 | 0.9 | 1.0 | 0.8 | 0.9 | 0.9 | 0.8 | 1.0 |

*Table A.6 – Number of Short Connections on Critical Path for Manhattan Radius 1 Using Architecture-Oblivious Placement*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 16.4 | 16.0 | 15.2 | 15.8 | 15.6 | 15.2 | 15.5 | 15.9 | 14.8 | 15.2 | 15.3 | 15.2 | 15.3 | 14.2 | 15.5 | 14.6 | 15.0 | -8.5 |
| Apex2 | 16.5 | 17.3 | 17.8 | 18.3 | 17.1 | 18.0 | 17.0 | 17.6 | 17.3 | 18.3 | 17.0 | 16.7 | 16.8 | 18.0 | 16.6 | 17.2 | 16.9 | 2.6 |
| Apex4 | 17.1 | 16.4 | 14.8 | 15.7 | 15.7 | 14.5 | 13.4 | 15.4 | 16.3 | 17.7 | 14.6 | 14.2 | 15.5 | 15.6 | 16.8 | 14.7 | 14.6 | -14.5 |
| Bigkey | 9.1 | 9.2 | 10.2 | 9.2 | 8.4 | 8.3 | 8.8 | 8.6 | 9.1 | 8.1 | 8.8 | 9.0 | 8.5 | 8.1 | 8.6 | 7.8 | 8.4 | -8.3 |
| Clma | 35.9 | 34.3 | 36.8 | 37.0 | 34.4 | 35.7 | 33.7 | 35.3 | 39.4 | 35.9 | 34.1 | 37.1 | 37.4 | 37.1 | 33.5 | 36.4 | 34.6 | -3.6 |
| Des | 15.3 | 17.0 | 15.0 | 14.8 | 16.3 | 15.0 | 15.9 | 15.3 | 15.3 | 14.8 | 15.3 | 15.1 | 15.0 | 14.5 | 15.2 | 14.7 | 14.4 | -6.1 |
| Diffeq | 17.9 | 19.0 | 16.9 | 17.2 | 18.0 | 16.7 | 16.9 | 16.4 | 16.7 | 16.9 | 16.3 | 16.7 | 16.1 | 16.6 | 16.2 | 16.5 | 15.6 | -12.9 |
| Display_chip | 16.4 | 16.1 | 16.1 | 16.5 | 16.6 | 16.5 | 16.8 | 15.9 | 16.2 | 15.3 | 16.5 | 15.6 | 15.2 | 15.0 | 15.8 | 15.4 | 16.0 | -2.0 |
| Dsip | 8.4 | 8.5 | 9.4 | 8.2 | 7.6 | 8.3 | 7.6 | 8.4 | 8.6 | 8.2 | 8.0 | 8.1 | 7.9 | 7.4 | 8.3 | 8.6 | 8.6 | 3.2 |
| Elliptic | 24.1 | 24.3 | 26.6 | 23.5 | 25.2 | 28.9 | 25.8 | 26.1 | 26.4 | 25.6 | 24.9 | 25.6 | 26.0 | 25.2 | 24.2 | 23.8 | 24.3 | 0.7 |
| Ex1010 | 24.6 | 26.1 | 25.4 | 25.8 | 25.5 | 24.0 | 26.0 | 26.9 | 24.4 | 25.6 | 24.6 | 23.6 | 23.7 | 26.7 | 24.8 | 25.8 | 26.0 | 5.9 |
| Ex5p | 14.7 | 14.6 | 15.6 | 16.1 | 15.4 | 16.0 | 15.0 | 14.6 | 16.3 | 15.2 | 15.4 | 16.0 | 15.7 | 15.0 | 14.8 | 16.2 | 16.1 | 9.0 |
| Frisc | 29.9 | 29.1 | 31.5 | 28.9 | 31.4 | 29.3 | 30.4 | 29.4 | 29.2 | 28.3 | 29.7 | 30.1 | 29.8 | 28.8 | 28.4 | 28.6 | 28.5 | -4.6 |
| Img_calc | 38.2 | 38.0 | 37.9 | 36.9 | 38.6 | 37.8 | 36.8 | 38.0 | 37.6 | 35.6 | 35.4 | 35.1 | 35.5 | 34.9 | 34.5 | 34.8 | 34.6 | -9.3 |
| Img_interp | 22.8 | 24.0 | 21.7 | 27.4 | 21.9 | 23.1 | 21.8 | 23.2 | 21.3 | 20.9 | 21.1 | 21.9 | 20.3 | 21.6 | 20.6 | 22.3 | 21.7 | -4.9 |
| Input_chip | 15.1 | 15.2 | 15.4 | 15.2 | 14.4 | 14.3 | 14.9 | 14.2 | 14.8 | 13.8 | 14.5 | 14.7 | 13.8 | 14.5 | 14.5 | 13.4 | 13.6 | -10.4 |
| Misex3 | 16.4 | 15.3 | 15.6 | 14.6 | 14.7 | 14.0 | 13.8 | 14.1 | 15.1 | 14.3 | 13.9 | 14.7 | 15.1 | 14.3 | 14.1 | 14.8 | 14.9 | -9.1 |
| Pdc | 27.4 | 24.3 | 28.2 | 27.3 | 27.8 | 26.7 | 26.5 | 28.4 | 27.8 | 25.6 | 24.1 | 30.7 | 25.2 | 24.0 | 27.3 | 25.5 | 26.0 | -5.3 |
| Peak_chip | 17.4 | 18.3 | 17.8 | 17.2 | 16.7 | 17.3 | 17.0 | 16.2 | 16.8 | 17.1 | 16.6 | 16.6 | 16.4 | 15.7 | 16.6 | 16.0 | 16.1 | -7.1 |
| S298 | 31.1 | 28.7 | 33.2 | 28.7 | 30.6 | 27.7 | 30.6 | 29.8 | 29.5 | 28.3 | 28.7 | 38.3 | 31.4 | 30.0 | 31.4 | 32.1 | 30.1 | -3.2 |
| S38417 | 19.9 | 21.2 | 20.3 | 19.6 | 18.7 | 19.0 | 19.1 | 19.3 | 19.7 | 18.5 | 18.8 | 18.6 | 18.2 | 19.8 | 19.3 | 18.4 | 19.2 | -3.9 |
| S38584.1 | 15.2 | 15.2 | 15.3 | 14.7 | 14.7 | 14.7 | 15.1 | 14.8 | 15.1 | 14.9 | 14.3 | 14.6 | 15.0 | 15.2 | 15.1 | 15.2 | 14.5 | -4.6 |
| Scale125_chip | 23.5 | 23.7 | 23.3 | 23.4 | 23.1 | 23.2 | 22.0 | 22.8 | 22.8 | 21.1 | 22.7 | 22.7 | 21.8 | 21.8 | 22.3 | 21.8 | 22.6 | -3.9 |
| Scale2_chip | 18.3 | 18.7 | 18.1 | 17.1 | 17.7 | 17.2 | 18.1 | 18.3 | 17.0 | 18.2 | 17.1 | 17.6 | 17.3 | 17.4 | 17.1 | 17.3 | 16.9 | -7.9 |
| Seq | 15.8 | 16.7 | 15.6 | 15.2 | 15.8 | 16.3 | 15.8 | 15.1 | 16.6 | 15.5 | 16.6 | 16.1 | 15.7 | 15.3 | 16.1 | 15.1 | 13.8 | -13.1 |
| Spla | 25.9 | 21.8 | 23.8 | 19.8 | 23.6 | 22.9 | 20.2 | 25.0 | 24.6 | 25.9 | 23.7 | 26.1 | 24.0 | 22.2 | 20.1 | 23.1 | 21.0 | -18.7 |
| Tseng | 18.2 | 18.0 | 17.4 | 17.7 | 17.1 | 16.6 | 17.1 | 16.9 | 16.2 | 16.6 | 15.8 | 15.7 | 16.3 | 16.4 | 15.7 | 15.6 | 15.5 | -15.1 |
| Warping | 11.7 | 12.5 | 12.4 | 12.5 | 11.9 | 11.3 | 11.4 | 11.4 | 11.7 | 11.4 | 11.2 | 11.5 | 11.8 | 11.5 | 11.1 | 11.2 | 11.2 | -4.7 |
| **Geometric Avg** | 18.9 | 18.9 | 19.0 | 18.6 | 18.5 | 18.3 | 18.2 | 18.4 | 18.6 | 18.2 | 18.0 | 18.5 | 18.1 | 17.9 | 18.0 | 17.9 | 17.8 | -5.9 |

*Table A.7 – Delay vs # of NN Interconnects for Manhattan Radius 1 Using Only 1 Placement*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 15.3 | 15.8 | 15.8 | 15.4 | 16.0 | 15.5 | 15.2 | 15.5 | 15.3 | 15.4 | 15.0 | 15.1 | 15.4 | 15.0 | 15.3 | 15.5 | -1.3 |
| Apex2 | 17.0 | 16.9 | 17.6 | 17.5 | 17.3 | 16.9 | 17.4 | 17.2 | 16.9 | 17.4 | 17.2 | 16.9 | 17.3 | 17.2 | 16.8 | 17.0 | 17.2 | 1.2 |
| Apex4 | 15.8 | 15.5 | 15.5 | 15.6 | 15.8 | 15.4 | 15.7 | 16.0 | 15.6 | 15.0 | 15.3 | 15.2 | 15.3 | 15.2 | 15.1 | 15.5 | 14.5 | -7.8 |
| Bigkey | 8.8 | 9.0 | 8.9 | 8.3 | 8.4 | 8.2 | 8.6 | 8.5 | 8.2 | 8.7 | 8.4 | 8.3 | 8.8 | 8.3 | 8.4 | 8.7 | 8.6 | -2.9 |
| Clma | 34.2 | 35.2 | 33.6 | 36.4 | 32.5 | 33.1 | 33.0 | 34.6 | 33.7 | 32.9 | 34.4 | 34.8 | 32.5 | 33.1 | 34.9 | 33.2 | 34.6 | 1.0 |
| Des | 15.6 | 16.4 | 15.3 | 16.2 | 15.9 | 15.2 | 15.5 | 15.7 | 15.8 | 15.8 | 15.5 | 15.2 | 15.1 | 15.4 | 15.2 | 14.6 | 15.1 | -3.7 |
| Diffeq | 18.2 | 18.7 | 18.1 | 17.6 | 17.4 | 17.1 | 17.2 | 16.6 | 16.5 | 16.5 | 16.4 | 16.2 | 16.6 | 16.4 | 16.2 | 16.2 | 16.0 | -11.9 |
| Display_chip | 16.6 | 17.0 | 16.5 | 17.0 | 16.2 | 16.1 | 16.1 | 16.1 | 16.0 | 16.0 | 15.9 | 16.0 | 15.8 | 15.7 | 15.5 | 15.8 | 15.7 | -5.8 |
| Dsip | 8.0 | 8.3 | 8.2 | 8.3 | 8.6 | 8.5 | 8.1 | 8.1 | 8.7 | 8.1 | 8.5 | 8.3 | 8.1 | 8.2 | 8.0 | 8.3 | 8.1 | 0.9 |
| Elliptic | 24.6 | 26.7 | 25.2 | 24.6 | 25.1 | 24.7 | 24.8 | 25.3 | 25.2 | 24.7 | 23.9 | 24.3 | 23.6 | 24.9 | 25.0 | 24.5 | 24.2 | -1.6 |
| Ex1010 | 26.3 | 25.9 | 25.3 | 25.1 | 24.8 | 24.7 | 25.1 | 24.6 | 24.7 | 25.0 | 25.3 | 24.6 | 25.3 | 25.5 | 24.6 | 24.5 | 24.4 | -7.4 |
| Ex5p | 14.9 | 15.5 | 15.4 | 15.7 | 15.3 | 15.9 | 15.5 | 15.6 | 15.2 | 15.8 | 15.3 | 15.1 | 15.5 | 15.4 | 14.9 | 15.5 | 15.3 | 2.4 |
| Frisc | 30.4 | 30.5 | 30.4 | 30.6 | 29.8 | 29.6 | 29.8 | 29.7 | 29.6 | 29.2 | 29.3 | 29.6 | 28.8 | 29.3 | 28.9 | 29.6 | 29.0 | -4.5 |
| Img_calc | 39.5 | 40.1 | 39.7 | 39.2 | 39.5 | 38.1 | 37.7 | 37.5 | 37.0 | 36.4 | 36.1 | 36.4 | 35.8 | 35.8 | 36.4 | 36.2 | 35.6 | -9.9 |
| Img_interp | 22.4 | 22.8 | 22.8 | 21.7 | 21.3 | 21.2 | 21.3 | 21.4 | 20.8 | 20.7 | 21.2 | 21.0 | 20.9 | 21.2 | 21.2 | 21.2 | 20.8 | -7.1 |
| Input_chip | 15.4 | 15.4 | 15.4 | 14.9 | 14.5 | 14.5 | 14.2 | 14.0 | 13.8 | 13.7 | 13.9 | 13.8 | 13.5 | 13.9 | 13.9 | 13.6 | 13.8 | -10.4 |
| Misex3 | 15.3 | 15.2 | 15.4 | 15.2 | 15.0 | 15.3 | 14.9 | 15.1 | 14.3 | 14.3 | 14.5 | 14.4 | 14.5 | 15.0 | 14.3 | 14.4 | 14.7 | -3.8 |
| Pdc | 27.1 | 26.0 | 26.9 | 27.5 | 26.3 | 28.4 | 26.5 | 25.7 | 24.8 | 25.2 | 25.7 | 26.3 | 29.4 | 26.3 | 27.3 | 26.6 | 26.7 | -1.7 |
| Peak_chip | 18.1 | 18.5 | 18.6 | 17.5 | 17.6 | 17.6 | 17.4 | 17.6 | 17.4 | 17.2 | 17.3 | 17.0 | 17.0 | 17.1 | 17.0 | 16.7 | 16.8 | -7.3 |
| S298 | 32.0 | 30.9 | 31.7 | 32.1 | 31.8 | 33.1 | 31.8 | 31.7 | 31.4 | 31.9 | 31.2 | 30.4 | 30.1 | 29.8 | 30.3 | 32.0 | 30.5 | -4.6 |
| S38417 | 20.2 | 20.3 | 20.8 | 21.0 | 20.4 | 20.4 | 20.1 | 19.8 | 19.8 | 19.9 | 19.7 | 19.2 | 19.2 | 19.6 | 19.5 | 19.9 | 19.5 | -3.5 |
| S38584.1 | 15.2 | 15.4 | 15.1 | 15.3 | 15.0 | 15.1 | 15.2 | 15.3 | 15.1 | 14.9 | 15.2 | 15.1 | 15.0 | 14.9 | 14.9 | 15.1 | 15.0 | -1.1 |
| Scale125_chip | 24.3 | 23.6 | 23.7 | 23.5 | 22.7 | 22.5 | 22.4 | 22.4 | 22.4 | 22.0 | 22.1 | 22.0 | 22.3 | 21.7 | 22.1 | 21.7 | 21.5 | -11.8 |
| Scale2_chip | 18.8 | 18.4 | 18.7 | 18.9 | 18.6 | 18.5 | 18.0 | 17.7 | 17.5 | 17.5 | 17.6 | 17.4 | 17.5 | 17.6 | 17.1 | 17.5 | 17.7 | -6.0 |
| Seq | 15.8 | 15.4 | 15.5 | 16.1 | 15.4 | 15.2 | 15.0 | 14.9 | 15.2 | 15.2 | 15.2 | 15.2 | 15.5 | 15.3 | 15.9 | 15.8 | 15.8 | -0.4 |
| Spla | 22.9 | 22.1 | 22.6 | 23.2 | 21.4 | 22.3 | 21.2 | 21.6 | 21.5 | 21.8 | 22.9 | 22.2 | 23.0 | 23.9 | 22.8 | 22.3 | 22.0 | -3.8 |
| Tseng | 18.2 | 18.3 | 18.2 | 17.9 | 17.6 | 17.0 | 16.9 | 16.6 | 16.7 | 15.8 | 16.0 | 16.0 | 16.2 | 15.9 | 15.9 | 15.8 | 16.0 | -12.3 |
| Warping | 11.7 | 11.7 | 11.2 | 11.4 | 11.2 | 11.0 | 11.3 | 11.0 | 10.9 | 10.7 | 10.7 | 10.7 | 10.8 | 10.8 | 10.8 | 10.6 | 10.6 | -9.5 |
| **Geometric Avg** | 18.8 | 18.9 | 18.8 | 18.8 | 18.5 | 18.4 | 18.3 | 18.3 | 18.1 | 18.0 | 18.1 | 17.9 | 18.1 | 18.0 | 18.0 | 18.0 | 17.9 | -4.9 |

*Table A.8 - Delay vs # of NN Interconnects for Cross Radius 1*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 22.4 | 22.5 | 22.5 | 22.5 | 22.6 | 22.6 | 22.7 | 22.7 | 22.7 | 22.8 | 22.8 | 22.9 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 2.8 |
| Apex2 | 32.9 | 33.0 | 33.0 | 33.1 | 33.1 | 33.2 | 33.3 | 33.3 | 33.4 | 33.4 | 33.5 | 33.5 | 33.6 | 33.6 | 33.7 | 33.7 | 33.8 | 2.5 |
| Apex4 | 22.6 | 22.6 | 22.7 | 22.7 | 22.7 | 22.8 | 22.8 | 22.8 | 22.9 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 23.1 | 23.1 | 23.1 | 2.5 |
| Bigkey | 26.6 | 26.6 | 26.7 | 26.8 | 26.9 | 26.9 | 27.0 | 27.1 | 27.2 | 27.2 | 27.3 | 27.4 | 27.4 | 27.5 | 27.6 | 27.7 | 27.7 | 4.4 |
| Clma | 152.1 | 152.5 | 152.8 | 153.2 | 153.5 | 153.9 | 154.3 | 154.6 | 155.0 | 155.3 | 155.7 | 155.9 | 156.1 | 156.4 | 156.6 | 156.8 | 157.1 | 3.2 |
| Des | 35.3 | 35.4 | 35.5 | 35.6 | 35.7 | 35.8 | 35.9 | 36.0 | 36.1 | 36.2 | 36.3 | 36.5 | 36.7 | 36.8 | 37.0 | 37.1 | 37.3 | 5.7 |
| Diffeq | 19.9 | 19.9 | 20.0 | 20.0 | 20.1 | 20.1 | 20.1 | 20.2 | 20.2 | 20.3 | 20.3 | 20.3 | 20.4 | 20.4 | 20.4 | 20.5 | 20.5 | 3.1 |
| Display_chip | 20.5 | 20.5 | 20.5 | 20.6 | 20.6 | 20.7 | 20.7 | 20.8 | 20.8 | 20.9 | 20.9 | 21.0 | 21.0 | 21.1 | 21.1 | 21.2 | 21.2 | 3.7 |
| Dsip | 26.2 | 26.2 | 26.3 | 26.4 | 26.4 | 26.5 | 26.6 | 26.7 | 26.7 | 26.8 | 26.9 | 27.0 | 27.1 | 27.2 | 27.3 | 27.5 | 27.6 | 5.4 |
| Elliptic | 58.9 | 59.0 | 59.1 | 59.2 | 59.3 | 59.4 | 59.5 | 59.6 | 59.7 | 59.7 | 59.8 | 59.9 | 60.0 | 60.1 | 60.2 | 60.3 | 60.4 | 2.6 |
| Ex1010 | 76.6 | 76.7 | 76.8 | 77.0 | 77.1 | 77.2 | 77.3 | 77.5 | 77.6 | 77.7 | 77.8 | 78.0 | 78.1 | 78.2 | 78.3 | 78.5 | 78.6 | 2.6 |
| Ex5p | 18.5 | 18.5 | 18.5 | 18.6 | 18.6 | 18.6 | 18.7 | 18.7 | 18.7 | 18.7 | 18.8 | 18.8 | 18.8 | 18.8 | 18.9 | 18.9 | 18.9 | 2.4 |
| Frisc | 60.4 | 60.4 | 60.5 | 60.6 | 60.7 | 60.8 | 60.9 | 61.0 | 61.1 | 61.2 | 61.3 | 61.4 | 61.4 | 61.5 | 61.6 | 61.7 | 61.8 | 2.4 |
| Img_calc | 152.4 | 152.7 | 153.0 | 153.3 | 153.5 | 153.8 | 154.1 | 154.3 | 154.6 | 154.9 | 155.1 | 155.4 | 155.7 | 156.0 | 156.2 | 156.5 | 156.8 | 2.8 |
| Img_interp | 32.5 | 32.6 | 32.7 | 32.9 | 33.0 | 33.1 | 33.2 | 33.3 | 33.4 | 33.5 | 33.6 | 33.7 | 33.8 | 33.9 | 33.9 | 34.0 | 34.1 | 4.9 |
| Input_chip | 8.8 | 8.8 | 8.9 | 8.9 | 8.9 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 9.1 | 9.1 | 9.1 | 9.2 | 3.8 |
| Misex3 | 22.9 | 22.9 | 23.0 | 23.0 | 23.0 | 23.1 | 23.1 | 23.2 | 23.2 | 23.2 | 23.3 | 23.3 | 23.4 | 23.4 | 23.4 | 23.5 | 23.5 | 2.7 |
| Pdc | 97.8 | 98.0 | 98.1 | 98.2 | 98.3 | 98.5 | 98.6 | 98.7 | 98.8 | 99.0 | 99.1 | 99.2 | 99.3 | 99.5 | 99.6 | 99.7 | 99.8 | 2.0 |
| Peak_chip | 8.4 | 8.4 | 8.5 | 8.5 | 8.5 | 8.5 | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 | 8.7 | 8.7 | 8.7 | 8.7 | 8.7 | 8.8 | 4.0 |
| S298 | 25.2 | 25.3 | 25.3 | 25.4 | 25.4 | 25.5 | 25.5 | 25.6 | 25.6 | 25.7 | 25.7 | 25.8 | 25.9 | 25.9 | 26.0 | 26.0 | 26.1 | 3.3 |
| S38417 | 93.7 | 93.9 | 94.1 | 94.2 | 94.4 | 94.6 | 94.7 | 94.9 | 95.1 | 95.3 | 95.4 | 95.6 | 95.8 | 96.0 | 96.1 | 96.3 | 96.5 | 3.0 |
| S38584.1 | 89.4 | 89.6 | 89.8 | 90.0 | 90.1 | 90.3 | 90.5 | 90.7 | 90.8 | 91.0 | 91.2 | 91.3 | 91.5 | 91.7 | 91.9 | 92.0 | 92.2 | 3.1 |
| Scale125_chip | 29.5 | 29.5 | 29.6 | 29.7 | 29.7 | 29.8 | 29.9 | 29.9 | 30.0 | 30.1 | 30.1 | 30.2 | 30.3 | 30.5 | 30.6 | 30.7 | 30.8 | 4.4 |
| Scale2_chip | 12.6 | 12.6 | 12.6 | 12.7 | 12.7 | 12.7 | 12.8 | 12.8 | 12.8 | 12.9 | 12.9 | 12.9 | 13.0 | 13.0 | 13.0 | 13.1 | 13.1 | 4.0 |
| Seq | 29.0 | 29.1 | 29.1 | 29.2 | 29.2 | 29.3 | 29.3 | 29.4 | 29.4 | 29.4 | 29.5 | 29.5 | 29.6 | 29.6 | 29.7 | 29.7 | 29.8 | 2.6 |
| Spla | 70.3 | 70.4 | 70.5 | 70.6 | 70.7 | 70.8 | 70.9 | 71.0 | 71.1 | 71.2 | 71.3 | 71.4 | 71.5 | 71.6 | 71.7 | 71.8 | 71.9 | 2.2 |
| Tseng | 13.8 | 13.9 | 13.9 | 13.9 | 14.0 | 14.0 | 14.0 | 14.0 | 14.1 | 14.1 | 14.1 | 14.1 | 14.2 | 14.2 | 14.2 | 14.3 | 14.3 | 3.2 |
| Warping | 15.1 | 15.2 | 15.2 | 15.2 | 15.3 | 15.3 | 15.4 | 15.4 | 15.4 | 15.5 | 15.5 | 15.5 | 15.6 | 15.6 | 15.6 | 15.7 | 15.7 | 3.7 |
| **Geometric Avg** | 33.1 | 33.1 | 33.2 | 33.3 | 33.3 | 33.4 | 33.5 | 33.6 | 33.6 | 33.7 | 33.8 | 33.8 | 33.9 | 34.0 | 34.0 | 34.1 | 34.2 | 3.3 |

*Table A.9 – Area vs # of NN Interconnects for Cross Radius 1 (Measured Under Constant Track Count)*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 15.1 | 15.6 | 15.6 | 15.5 | 15.7 | 15.6 | 16.0 | 15.4 | 15.0 | 15.6 | 15.1 | 15.8 | 15.5 | 15.2 | 15.1 | 15.5 | -1.3 |
| Apex2 | 17.0 | 17.8 | 16.7 | 17.3 | 16.9 | 17.4 | 16.5 | 16.8 | 17.6 | 17.0 | 17.0 | 17.1 | 17.2 | 17.3 | 16.9 | 16.9 | 17.2 | 1.5 |
| Apex4 | 15.8 | 15.7 | 15.5 | 15.9 | 15.1 | 15.4 | 15.3 | 15.1 | 15.4 | 15.5 | 15.9 | 15.9 | 15.1 | 15.5 | 15.2 | 15.3 | 15.6 | -1.0 |
| Bigkey | 8.8 | 8.8 | 9.1 | 8.6 | 8.5 | 8.3 | 8.8 | 8.9 | 9.3 | 9.0 | 9.0 | 8.6 | 9.0 | 9.1 | 9.1 | 8.9 | 8.9 | 0.9 |
| Clma | 34.2 | 33.8 | 33.6 | 33.0 | 33.9 | 34.4 | 35.7 | 34.4 | 33.7 | 34.1 | 36.0 | 34.8 | 33.8 | 33.1 | 35.7 | 35.5 | 33.5 | -2.1 |
| Des | 15.6 | 15.5 | 15.3 | 15.5 | 15.2 | 15.2 | 15.5 | 16.0 | 15.4 | 15.2 | 15.1 | 15.2 | 15.4 | 15.3 | 14.9 | 15.3 | 15.7 | 0.7 |
| Diffeq | 18.2 | 18.2 | 18.1 | 18.5 | 18.0 | 17.9 | 17.7 | 17.7 | 17.7 | 17.8 | 17.6 | 17.5 | 18.0 | 17.6 | 17.6 | 17.8 | 17.7 | -2.4 |
| Display_chip | 16.6 | 16.4 | 16.6 | 16.8 | 16.5 | 16.7 | 16.6 | 16.7 | 16.4 | 16.4 | 16.5 | 16.3 | 16.2 | 16.2 | 16.6 | 16.4 | 16.4 | -1.7 |
| Dsip | 8.0 | 8.0 | 7.9 | 7.9 | 8.1 | 7.9 | 8.1 | 7.9 | 7.8 | 7.9 | 7.9 | 7.9 | 7.9 | 8.1 | 8.0 | 7.8 | 7.8 | -2.7 |
| Elliptic | 24.6 | 25.0 | 25.2 | 25.8 | 24.6 | 26.5 | 25.7 | 24.8 | 25.6 | 25.7 | 25.3 | 25.6 | 25.2 | 24.9 | 25.1 | 24.8 | 25.3 | 2.7 |
| Ex1010 | 26.3 | 26.4 | 25.1 | 24.9 | 25.8 | 25.8 | 26.1 | 25.9 | 26.0 | 25.9 | 25.0 | 26.2 | 25.6 | 26.5 | 26.4 | 24.8 | 25.1 | -4.6 |
| Ex5p | 14.9 | 15.3 | 15.8 | 15.2 | 15.8 | 15.4 | 15.5 | 15.2 | 15.3 | 15.5 | 15.1 | 15.2 | 15.6 | 15.2 | 15.3 | 15.5 | 15.4 | 3.3 |
| Frisc | 30.4 | 29.7 | 29.9 | 30.0 | 29.7 | 29.4 | 30.1 | 29.6 | 29.6 | 29.3 | 29.5 | 29.1 | 29.6 | 29.3 | 28.9 | 29.1 | 29.0 | -4.3 |
| Img_calc | 39.5 | 39.3 | 39.6 | 38.8 | 38.7 | 39.0 | 39.0 | 39.0 | 38.7 | 38.8 | 38.6 | 38.5 | 38.1 | 38.3 | 38.4 | 38.1 | 38.4 | -2.7 |
| Img_interp | 22.4 | 21.8 | 22.1 | 22.0 | 21.8 | 22.1 | 22.2 | 21.6 | 22.6 | 22.4 | 21.8 | 22.0 | 21.6 | 22.1 | 22.3 | 22.0 | 22.3 | -0.4 |
| Input_chip | 15.4 | 15.4 | 15.5 | 15.1 | 15.2 | 15.6 | 15.3 | 15.6 | 15.1 | 15.4 | 15.1 | 15.0 | 15.1 | 14.9 | 15.0 | 15.2 | 14.8 | -3.6 |
| Misex3 | 15.3 | 15.0 | 15.2 | 15.2 | 15.2 | 15.0 | 15.0 | 14.7 | 14.6 | 14.8 | 14.9 | 14.4 | 14.8 | 14.7 | 14.7 | 14.7 | 14.4 | -6.0 |
| Pdc | 27.1 | 25.2 | 26.2 | 25.6 | 26.5 | 26.5 | 26.6 | 26.3 | 27.5 | 26.1 | 26.0 | 25.7 | 25.1 | 27.2 | 27.5 | 27.3 | 27.5 | 1.3 |
| Peak_chip | 18.1 | 18.3 | 18.0 | 18.5 | 18.0 | 18.4 | 18.2 | 18.2 | 18.0 | 18.0 | 17.9 | 18.0 | 18.2 | 18.4 | 18.4 | 18.0 | 18.1 | -0.3 |
| S298 | 32.0 | 30.7 | 30.0 | 30.7 | 30.5 | 29.9 | 31.0 | 31.3 | 31.2 | 30.9 | 32.1 | 31.1 | 30.3 | 30.3 | 30.0 | 30.2 | 30.1 | -5.8 |
| S38417 | 20.2 | 20.0 | 20.4 | 20.6 | 19.9 | 20.3 | 20.1 | 19.8 | 19.9 | 20.2 | 19.9 | 19.8 | 19.6 | 20.4 | 19.7 | 20.5 | 19.6 | -3.0 |
| S38584.1 | 15.2 | 14.9 | 14.6 | 15.1 | 14.7 | 14.9 | 15.4 | 14.6 | 15.0 | 15.1 | 15.2 | 15.1 | 14.6 | 14.8 | 14.8 | 14.8 | 14.6 | -3.9 |
| Scale125_chip | 24.3 | 23.8 | 24.1 | 23.8 | 23.6 | 24.0 | 24.0 | 23.7 | 23.7 | 23.7 | 23.4 | 23.6 | 23.4 | 23.5 | 23.7 | 23.4 | 23.3 | -4.5 |
| Scale2_chip | 18.8 | 17.9 | 18.3 | 18.3 | 18.2 | 18.4 | 18.3 | 18.2 | 18.0 | 18.1 | 18.0 | 17.8 | 17.8 | 18.1 | 18.0 | 17.9 | 17.8 | -5.1 |
| Seq | 15.8 | 15.3 | 15.1 | 15.2 | 15.2 | 15.6 | 15.0 | 15.8 | 15.1 | 15.3 | 15.3 | 15.4 | 15.1 | 15.4 | 14.9 | 15.0 | 15.6 | -1.3 |
| Spla | 22.9 | 25.1 | 21.8 | 23.4 | 21.6 | 22.9 | 22.7 | 22.0 | 23.2 | 21.7 | 24.4 | 22.8 | 22.2 | 22.1 | 23.0 | 22.9 | 22.8 | -0.5 |
| Tseng | 18.2 | 18.2 | 18.3 | 18.0 | 17.8 | 17.6 | 17.7 | 18.0 | 17.8 | 17.9 | 17.5 | 17.8 | 17.7 | 17.5 | 17.4 | 17.6 | 18.0 | -1.3 |
| Warping | 11.7 | 11.5 | 11.4 | 11.4 | 11.4 | 11.5 | 11.4 | 11.6 | 11.5 | 11.3 | 11.6 | 11.4 | 11.3 | 11.4 | 11.3 | 11.3 | 11.6 | -1.3 |
| **Geometric Avg** | 18.8 | 18.7 | 18.6 | 18.7 | 18.5 | 18.7 | 18.7 | 18.6 | 18.7 | 18.5 | 18.6 | 18.5 | 18.4 | 18.5 | 18.5 | 18.5 | 18.5 | -1.8 |

*Table A.10 – Delay vs # of NN Interconnects for Cross Radius 1 Using Architecture-Oblivious Placement*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 15.7 | 15.3 | 15.8 | 15.8 | 15.4 | 15.6 | 15.3 | 15.7 | 15.3 | 15.4 | 15.5 | 15.3 | 15.3 | 15.2 | 15.1 | 15.2 | 15.3 | -2.4 |
| Apex2 | 17.0 | 16.9 | 17.6 | 17.5 | 17.3 | 17.1 | 17.2 | 16.8 | 17.3 | 17.1 | 17.0 | 16.5 | 17.4 | 17.3 | 16.8 | 16.8 | 17.3 | 2.0 |
| Apex4 | 15.8 | 15.5 | 15.5 | 15.6 | 15.8 | 15.9 | 15.7 | 15.8 | 15.5 | 15.2 | 15.2 | 15.2 | 15.3 | 15.3 | 15.7 | 15.2 | 15.0 | -5.2 |
| Bigkey | 8.8 | 9.0 | 8.9 | 8.3 | 8.4 | 8.4 | 8.3 | 8.6 | 8.5 | 8.7 | 8.3 | 8.5 | 8.7 | 8.6 | 8.5 | 8.8 | 8.4 | -4.5 |
| Clma | 34.2 | 35.2 | 33.6 | 36.4 | 32.5 | 33.3 | 34.4 | 33.0 | 33.3 | 33.6 | 33.9 | 35.2 | 34.4 | 33.0 | 33.6 | 34.8 | 33.7 | -1.5 |
| Des | 15.6 | 16.4 | 15.3 | 16.2 | 15.9 | 15.4 | 15.3 | 16.2 | 15.7 | 15.1 | 15.8 | 15.2 | 15.1 | 15.5 | 15.1 | 15.3 | 15.2 | -2.7 |
| Diffeq | 18.2 | 18.7 | 18.1 | 17.6 | 17.4 | 17.2 | 17.3 | 17.1 | 16.9 | 16.6 | 16.9 | 16.6 | 16.7 | 16.4 | 16.5 | 16.7 | 16.4 | -9.6 |
| Display_chip | 16.6 | 17.0 | 16.5 | 17.0 | 16.2 | 16.0 | 16.0 | 16.0 | 16.2 | 16.0 | 15.8 | 15.7 | 15.7 | 15.8 | 15.7 | 15.7 | 16.0 | -3.9 |
| Dsip | 8.0 | 8.3 | 8.2 | 8.3 | 8.6 | 8.2 | 8.2 | 8.3 | 7.9 | 8.3 | 8.2 | 8.3 | 8.1 | 8.2 | 7.9 | 8.0 | 8.4 | 5.0 |
| Elliptic | 24.6 | 26.7 | 25.2 | 24.6 | 25.1 | 24.6 | 23.9 | 24.1 | 24.1 | 24.8 | 25.2 | 24.2 | 24.8 | 24.5 | 24.2 | 25.3 | 24.2 | -1.8 |
| Ex1010 | 26.3 | 25.9 | 25.3 | 25.1 | 24.8 | 24.4 | 24.0 | 23.8 | 25.3 | 25.0 | 24.4 | 24.2 | 25.1 | 24.6 | 24.4 | 25.2 | 24.5 | -6.9 |
| Ex5p | 14.9 | 15.5 | 15.4 | 15.7 | 15.3 | 15.6 | 15.5 | 15.4 | 15.8 | 15.8 | 15.7 | 15.2 | 15.2 | 15.5 | 15.6 | 14.9 | 15.2 | 1.7 |
| Frisc | 30.4 | 30.5 | 30.4 | 30.6 | 29.8 | 29.2 | 29.6 | 29.8 | 29.8 | 29.8 | 29.2 | 29.1 | 28.5 | 29.4 | 28.6 | 29.1 | 28.8 | -5.0 |
| Img_calc | 39.5 | 40.1 | 39.7 | 39.2 | 39.5 | 38.4 | 38.3 | 37.4 | 36.8 | 36.6 | 36.7 | 37.0 | 36.6 | 36.2 | 36.6 | 36.0 | 36.9 | -6.6 |
| Img_interp | 22.4 | 22.8 | 22.8 | 21.7 | 21.3 | 21.4 | 21.2 | 21.2 | 21.2 | 20.9 | 20.9 | 21.1 | 20.9 | 20.7 | 21.2 | 20.5 | 20.8 | -7.2 |
| Input_chip | 15.4 | 15.4 | 15.4 | 14.9 | 14.5 | 14.5 | 14.3 | 14.0 | 13.8 | 14.0 | 13.9 | 13.8 | 13.9 | 13.6 | 13.8 | 13.8 | 13.6 | -11.5 |
| Misex3 | 15.3 | 15.2 | 15.4 | 15.2 | 15.0 | 14.9 | 14.5 | 14.6 | 14.1 | 14.4 | 15.3 | 14.9 | 14.8 | 14.4 | 14.6 | 15.1 | 14.6 | -4.6 |
| Pdc | 27.1 | 26.0 | 26.9 | 27.5 | 26.3 | 24.9 | 25.3 | 26.3 | 26.6 | 26.2 | 26.5 | 26.4 | 27.0 | 25.8 | 25.7 | 24.7 | 26.0 | -4.1 |
| Peak_chip | 18.1 | 18.5 | 18.6 | 17.5 | 17.6 | 17.5 | 17.4 | 17.4 | 17.3 | 17.2 | 16.9 | 17.4 | 17.0 | 17.2 | 16.9 | 17.2 | 16.8 | -7.3 |
| S298 | 32.0 | 30.9 | 31.7 | 32.1 | 31.8 | 31.6 | 29.4 | 31.3 | 32.6 | 30.3 | 30.0 | 32.4 | 29.5 | 31.2 | 29.9 | 30.6 | 30.9 | -3.3 |
| S38417 | 20.2 | 20.3 | 20.8 | 21.0 | 20.4 | 20.0 | 20.0 | 19.8 | 19.1 | 20.5 | 19.5 | 19.6 | 19.5 | 19.6 | 19.4 | 19.3 | 19.7 | -2.3 |
| S38584.1 | 15.2 | 15.4 | 15.1 | 15.3 | 15.0 | 15.0 | 15.6 | 15.1 | 15.2 | 14.6 | 15.4 | 15.1 | 15.1 | 15.2 | 14.9 | 15.2 | 15.0 | -0.8 |
| Scale125_chip | 24.3 | 23.6 | 23.7 | 23.5 | 22.7 | 22.6 | 22.4 | 22.3 | 22.3 | 22.4 | 22.0 | 22.1 | 21.9 | 21.7 | 21.9 | 22.2 | 21.8 | -10.4 |
| Scale2_chip | 18.8 | 18.4 | 18.7 | 18.9 | 18.6 | 18.4 | 17.9 | 17.6 | 17.6 | 17.7 | 17.7 | 17.4 | 17.8 | 17.9 | 17.3 | 17.1 | 17.3 | -7.9 |
| Seq | 15.8 | 15.4 | 15.5 | 16.1 | 15.4 | 15.4 | 15.6 | 15.1 | 15.8 | 15.6 | 15.4 | 15.2 | 15.4 | 15.8 | 14.7 | 15.1 | 15.4 | -2.4 |
| Spla | 22.9 | 22.1 | 22.6 | 23.2 | 21.4 | 22.7 | 23.5 | 21.4 | 23.2 | 21.5 | 22.2 | 21.8 | 24.1 | 22.2 | 21.2 | 22.3 | 21.7 | -5.3 |
| Tseng | 18.2 | 18.3 | 18.2 | 17.9 | 17.6 | 17.1 | 16.6 | 16.5 | 16.4 | 16.6 | 16.1 | 16.2 | 15.8 | 16.1 | 16.0 | 15.9 | 15.9 | -12.9 |
| Warping | 11.7 | 11.7 | 11.2 | 11.4 | 11.2 | 11.3 | 11.1 | 10.9 | 11.1 | 11.0 | 10.7 | 10.9 | 11.0 | 10.9 | 11.0 | 10.7 | 10.6 | -9.7 |
| **Geometric Avg** | 18.8 | 18.9 | 18.8 | 18.8 | 18.5 | 18.3 | 18.2 | 18.2 | 18.2 | 18.1 | 18.1 | 18.1 | 18.1 | 18.0 | 17.9 | 18.0 | 17.9 | -4.8 |

*Table A.11 – Delay vs # of NN Interconnects for Cross Radius 1 Using Nearest-Side Input Pin Connection Strategy*

| Circuit | Number of Short Connections On Critical Path That Fall Within NN Architecture | | | | | | | | | | | | | | | | Avg # of Connections Per Circuit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 0.8 | 0.8 | 0.0 | 0.2 | 0.4 | 0.4 | 0.6 | 0.4 | 0.4 | 0.2 | 0.4 | 0.6 | 0.2 | 0.4 | 0.0 | 0.4 | 0.4 |
| Apex2 | 0.8 | 0.8 | 0.6 | 0.2 | 0.4 | 0.2 | 0.4 | 0.8 | 0.4 | 1.2 | 0.6 | 0.4 | 0.6 | 0.6 | 0.4 | 0.2 | 0.5 |
| Apex4 | 0.4 | 0.6 | 0.2 | 0.0 | 0.6 | 0.0 | 0.4 | 0.4 | 0.4 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.2 |
| Bigkey | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Clma | 1.6 | 1.8 | 1.4 | 2.2 | 1.2 | 1.6 | 0.2 | 1.6 | 0.8 | 0.8 | 1.6 | 1.6 | 1.0 | 0.8 | 2.0 | 0.2 | 1.3 |
| Des | 0.8 | 1.4 | 0.8 | 0.8 | 1.0 | 0.6 | 1.2 | 0.6 | 0.8 | 0.4 | 0.2 | 1.0 | 1.4 | 0.8 | 1.0 | 0.4 | 0.8 |
| Diffeq | 6.8 | 5.2 | 6.6 | 6.6 | 6.0 | 5.6 | 5.0 | 5.4 | 5.6 | 5.6 | 5.2 | 3.6 | 4.6 | 5.0 | 5.2 | 5.0 | 5.4 |
| Display_chip | 2.8 | 4.0 | 2.4 | 2.4 | 1.6 | 2.0 | 1.8 | 2.2 | 2.6 | 2.2 | 2.6 | 1.8 | 2.0 | 1.6 | 1.8 | 1.6 | 2.2 |
| Dsip | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Elliptic | 1.6 | 3.2 | 2.6 | 2.4 | 1.8 | 1.6 | 1.6 | 2.0 | 1.8 | 1.6 | 2.6 | 1.6 | 1.8 | 1.8 | 1.8 | 2.0 | 2.0 |
| Ex1010 | 0.2 | 0.4 | 0.4 | 0.2 | 0.4 | 0.8 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.4 | 0.2 | 0.3 |
| Ex5p | 0.6 | 0.4 | 0.0 | 0.6 | 0.2 | 0.6 | 0.0 | 0.2 | 0.4 | 0.4 | 0.6 | 0.4 | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 |
| Frisc | 2.4 | 2.8 | 4.8 | 4.0 | 3.4 | 3.6 | 3.4 | 1.6 | 1.6 | 2.0 | 2.2 | 2.2 | 1.6 | 1.2 | 1.8 | 1.8 | 2.5 |
| Img_calc | 11.4 | 11.2 | 9.6 | 10.2 | 10.4 | 9.8 | 9.8 | 8.6 | 8.0 | 7.2 | 7.0 | 6.8 | 7.2 | 6.6 | 7.2 | 8.2 | 8.7 |
| Img_interp | 3.2 | 3.6 | 3.8 | 3.6 | 2.8 | 2.6 | 2.4 | 2.8 | 2.6 | 3.0 | 2.8 | 2.4 | 3.4 | 2.2 | 3.2 | 2.4 | 2.9 |
| Input_chip | 5.0 | 4.8 | 4.2 | 3.0 | 2.6 | 4.2 | 3.8 | 2.2 | 3.0 | 3.6 | 3.2 | 2.8 | 3.0 | 2.0 | 3.0 | 2.8 | 3.3 |
| Misex3 | 0.6 | 0.2 | 0.2 | 0.6 | 0.2 | 0.0 | 0.0 | 0.4 | 0.0 | 0.2 | 0.2 | 0.6 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 |
| Pdc | 0.2 | 0.2 | 0.8 | 0.4 | 0.6 | 0.4 | 0.2 | 0.4 | 0.6 | 0.4 | 0.4 | 0.4 | 0.4 | 1.0 | 0.2 | 0.2 | 0.4 |
| Peak_chip | 3.6 | 3.2 | 3.0 | 3.0 | 3.4 | 3.6 | 2.6 | 2.8 | 2.8 | 2.6 | 2.8 | 2.4 | 2.2 | 1.8 | 2.6 | 3.0 | 2.8 |
| S298 | 2.0 | 1.4 | 1.6 | 0.4 | 1.4 | 1.0 | 1.8 | 1.2 | 0.2 | 0.4 | 0.6 | 1.2 | 0.4 | 0.4 | 0.2 | 0.2 | 0.9 |
| S38417 | 2.8 | 3.4 | 2.8 | 2.2 | 1.8 | 1.4 | 2.2 | 1.6 | 1.8 | 2.4 | 2.0 | 2.0 | 2.8 | 1.6 | 2.4 | 2.2 | 2.2 |
| S38584.1 | 1.8 | 0.0 | 0.6 | 0.6 | 0.8 | 1.4 | 0.2 | 0.6 | 0.2 | 1.4 | 0.2 | 0.6 | 1.0 | 0.2 | 0.4 | 0.2 | 0.6 |
| Scale125_chip | 4.6 | 5.4 | 4.4 | 4.2 | 4.4 | 3.8 | 3.2 | 3.4 | 3.6 | 4.2 | 3.6 | 3.6 | 3.0 | 2.6 | 3.8 | 2.2 | 3.8 |
| Scale2_chip | 3.8 | 3.8 | 3.4 | 3.4 | 2.6 | 3.0 | 2.8 | 2.4 | 3.0 | 1.6 | 3.0 | 2.6 | 2.2 | 2.0 | 1.2 | 1.6 | 2.7 |
| Seq | 0.2 | 0.4 | 0.4 | 0.6 | 0.0 | 0.2 | 0.0 | 0.4 | 0.2 | 0.2 | 1.0 | 0.6 | 0.6 | 0.2 | 0.4 | 0.0 | 0.3 |
| Spla | 0.6 | 0.4 | 0.4 | 0.2 | 0.6 | 0.0 | 0.2 | 0.6 | 0.4 | 0.4 | 0.2 | 0.0 | 0.2 | 0.0 | 0.4 | 0.0 | 0.3 |
| Tseng | 6.0 | 7.2 | 5.6 | 6.2 | 4.0 | 4.4 | 5.0 | 5.0 | 4.8 | 4.2 | 4.6 | 4.2 | 4.4 | 3.2 | 4.0 | 4.4 | 4.8 |
| Warping | 2.0 | 2.0 | 1.6 | 1.8 | 1.8 | 1.8 | 2.0 | 1.8 | 2.2 | 1.8 | 1.8 | 1.8 | 1.8 | 1.6 | 2.0 | 1.6 | 1.8 |
| **Arithmetic Avg** | 2.4 | 2.5 | 2.2 | 2.1 | 2.0 | 2.0 | 1.8 | 1.8 | 1.7 | 1.7 | 1.8 | 1.6 | 1.7 | 1.4 | 1.7 | 1.5 | 1.9 |

*Table A.12 – Number of Short Connections on Critical Path for Cross Radius 1 Using Architecture-Aware Placement*

| Circuit | Number of Short Connections On Critical Path That Fall Within NN Architecture | | | | | | | | | | | | | | | | Avg # of Connections Per Circuit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
| Alu4 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.4 | 0.0 | 0.0 | 0.2 | 0.2 | 0.6 | 0.2 | 0.2 | 0.2 | 0.4 | 0.2 |
| Apex2 | 0.4 | 0.0 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.4 | 0.0 | 0.0 | 0.0 | 0.4 | 0.0 | 0.0 | 0.0 | 0.0 | 0.1 |
| Apex4 | 0.4 | 0.0 | 0.2 | 0.0 | 0.0 | 0.4 | 0.2 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 |
| Bigkey | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Clma | 0.6 | 0.0 | 0.4 | 0.2 | 0.0 | 0.4 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.4 | 0.2 | 0.0 | 0.2 |
| Des | 0.6 | 0.2 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.1 |
| Diffeq | 1.4 | 1.6 | 2.0 | 2.0 | 1.6 | 1.8 | 1.2 | 1.6 | 1.0 | 0.6 | 1.4 | 0.8 | 1.0 | 1.4 | 1.2 | 1.2 | 1.4 |
| Display_chip | 0.4 | 0.8 | 0.8 | 0.4 | 0.4 | 0.4 | 0.6 | 0.4 | 0.6 | 0.8 | 0.0 | 0.2 | 0.0 | 0.6 | 0.4 | 0.0 | 0.4 |
| Dsip | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Elliptic | 0.4 | 0.4 | 0.2 | 0.6 | 0.2 | 0.8 | 0.4 | 0.4 | 0.2 | 0.4 | 0.2 | 0.4 | 0.2 | 0.2 | 0.4 | 0.0 | 0.3 |
| Ex1010 | 0.2 | 0.0 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.1 |
| Ex5p | 0.4 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.1 |
| Frisc | 1.6 | 1.2 | 0.8 | 0.8 | 0.8 | 0.6 | 0.4 | 1.0 | 0.8 | 0.6 | 1.2 | 0.4 | 0.6 | 0.2 | 0.2 | 0.4 | 0.7 |
| Img_calc | 1.4 | 2.8 | 1.6 | 1.4 | 1.4 | 2.0 | 1.6 | 1.4 | 1.8 | 1.0 | 1.2 | 1.0 | 0.8 | 1.0 | 2.2 | 0.8 | 1.5 |
| Img_interp | 0.6 | 1.0 | 0.4 | 0.4 | 0.6 | 0.6 | 0.6 | 0.6 | 1.0 | 0.6 | 0.6 | 0.8 | 0.6 | 0.8 | 0.6 | 0.6 | 0.7 |
| Input_chip | 0.4 | 0.6 | 0.6 | 0.2 | 0.4 | 0.2 | 0.4 | 0.4 | 0.4 | 0.0 | 0.0 | 0.2 | 0.0 | 0.2 | 0.2 | 0.4 | 0.3 |
| Misex3 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Pdc | 0.4 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 | 0.0 | 0.2 | 0.2 | 0.4 | 0.0 | 0.0 | 0.2 | 0.4 | 0.2 | 0.0 | 0.2 |
| Peak_chip | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.4 | 0.4 | 0.2 | 0.4 | 0.4 | 0.0 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 |
| S298 | 1.2 | 0.6 | 0.2 | 0.0 | 0.4 | 0.4 | 0.2 | 0.8 | 0.2 | 0.6 | 0.6 | 0.2 | 0.4 | 0.2 | 0.2 | 0.4 | 0.4 |
| S38417 | 0.2 | 1.0 | 0.6 | 0.6 | 0.2 | 0.4 | 0.2 | 0.8 | 0.4 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.6 | 0.8 | 0.4 |
| S38584.1 | 0.4 | 0.6 | 0.8 | 0.8 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.2 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 |
| Scale125_chip | 1.0 | 1.0 | 0.8 | 1.0 | 0.6 | 0.6 | 0.6 | 0.8 | 1.0 | 0.6 | 0.4 | 0.4 | 0.6 | 0.6 | 0.4 | 0.6 | 0.7 |
| Scale2_chip | 1.6 | 0.6 | 0.6 | 1.0 | 0.6 | 0.2 | 0.6 | 0.2 | 0.2 | 0.2 | 0.0 | 0.2 | 0.4 | 0.2 | 0.6 | 0.4 | 0.5 |
| Seq | 0.2 | 0.4 | 0.0 | 0.4 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.1 |
| Spla | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.4 | 0.0 | 0.0 | 0.0 |
| Tseng | 2.2 | 1.4 | 1.0 | 1.8 | 1.2 | 0.8 | 1.2 | 1.0 | 1.2 | 0.8 | 1.0 | 0.6 | 0.2 | 0.8 | 0.6 | 1.2 | 1.1 |
| Warping | 0.4 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.6 | 0.2 | 0.0 | 0.2 | 0.2 | 0.2 | 0.2 | 0.0 | 0.0 | 0.2 | 0.2 |
| **Arithmetic Avg** | 0.6 | 0.5 | 0.4 | 0.4 | 0.3 | 0.4 | 0.4 | 0.4 | 0.4 | 0.3 | 0.3 | 0.3 | 0.2 | 0.3 | 0.3 | 0.3 | 0.4 |

*Table A.13 - Number of Short Connections on Critical Path for Cross Radius 1 Using Architecture-Oblivious Placement*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 15.7 | 15.2 | 15.3 | 15.4 | 15.2 | 15.5 | 15.3 | 15.3 | 15.0 | 14.9 | 15.1 | 14.8 | 14.8 | 14.9 | 15.4 | 15.1 | 15.1 | -3.6 |
| Apex2 | 17.0 | 17.1 | 16.9 | 17.1 | 16.8 | 17.1 | 16.7 | 16.9 | 16.6 | 17.0 | 16.7 | 17.1 | 16.7 | 17.2 | 16.4 | 17.0 | 16.8 | -1.3 |
| Apex4 | 15.8 | 15.3 | 15.4 | 15.3 | 15.8 | 15.1 | 15.2 | 15.9 | 15.2 | 15.0 | 15.6 | 15.3 | 14.8 | 15.4 | 15.5 | 14.9 | 15.7 | -0.3 |
| Bigkey | 8.8 | 8.7 | 8.5 | 8.7 | 8.7 | 8.8 | 8.7 | 8.3 | 8.4 | 8.9 | 8.4 | 8.6 | 8.7 | 8.9 | 8.5 | 8.6 | 8.6 | -2.9 |
| Clma | 34.2 | 34.9 | 33.7 | 33.7 | 36.6 | 34.2 | 34.3 | 32.4 | 33.9 | 33.6 | 33.5 | 33.6 | 31.7 | 32.1 | 32.6 | 33.7 | 32.7 | -4.5 |
| Des | 15.6 | 15.3 | 15.8 | 15.1 | 15.1 | 15.4 | 15.1 | 14.9 | 14.9 | 15.4 | 14.9 | 15.3 | 15.5 | 14.5 | 14.8 | 14.8 | 15.0 | -4.0 |
| Diffeq | 18.2 | 17.5 | 17.1 | 16.8 | 16.9 | 16.6 | 16.2 | 16.4 | 16.0 | 16.0 | 15.6 | 15.4 | 15.8 | 15.7 | 15.6 | 15.2 | 15.6 | -14.4 |
| Display_chip | 16.6 | 16.7 | 16.4 | 16.3 | 16.2 | 16.0 | 15.6 | 15.6 | 15.7 | 15.6 | 15.7 | 15.4 | 15.4 | 15.2 | 15.2 | 15.3 | 15.4 | -7.5 |
| Dsip | 8.0 | 8.1 | 8.1 | 8.3 | 8.2 | 8.2 | 8.4 | 8.1 | 8.2 | 7.9 | 8.0 | 8.3 | 7.8 | 7.8 | 8.3 | 7.8 | 7.9 | -1.5 |
| Elliptic | 24.6 | 25.8 | 24.9 | 24.7 | 24.4 | 25.1 | 25.0 | 23.8 | 24.1 | 25.4 | 24.3 | 25.2 | 24.2 | 23.5 | 24.5 | 24.1 | 24.1 | -1.9 |
| Ex1010 | 26.3 | 26.0 | 24.6 | 25.0 | 24.0 | 25.5 | 23.9 | 24.6 | 24.9 | 24.8 | 24.9 | 24.5 | 24.9 | 23.4 | 24.8 | 24.5 | 24.5 | -6.9 |
| Ex5p | 14.9 | 15.6 | 15.1 | 15.0 | 15.9 | 15.2 | 15.1 | 14.9 | 15.4 | 15.5 | 15.5 | 15.4 | 15.3 | 15.0 | 15.2 | 15.0 | 15.1 | 1.1 |
| Frisc | 30.4 | 30.2 | 30.3 | 29.4 | 29.1 | 29.0 | 29.5 | 29.3 | 29.1 | 29.0 | 28.0 | 28.6 | 28.3 | 28.1 | 28.7 | 28.1 | 27.6 | -9.0 |
| Img_calc | 39.5 | 38.3 | 38.2 | 37.4 | 36.8 | 35.9 | 35.6 | 35.3 | 35.2 | 36.2 | 35.5 | 35.1 | 34.9 | 35.0 | 34.8 | 34.3 | 34.5 | -12.8 |
| Img_interp | 22.4 | 21.3 | 20.6 | 20.5 | 20.7 | 20.5 | 20.3 | 20.1 | 20.7 | 20.8 | 20.5 | 19.7 | 20.2 | 20.4 | 20.1 | 19.9 | 19.8 | -11.8 |
| Input_chip | 15.4 | 15.5 | 14.7 | 14.8 | 14.7 | 14.3 | 14.0 | 14.1 | 14.0 | 13.9 | 13.6 | 13.5 | 13.4 | 13.2 | 13.4 | 13.2 | 13.3 | -13.6 |
| Misex3 | 15.3 | 15.0 | 15.1 | 14.2 | 14.7 | 14.7 | 14.5 | 14.7 | 14.6 | 15.1 | 14.2 | 14.6 | 14.7 | 14.2 | 14.0 | 14.4 | 13.9 | -9.3 |
| Pdc | 27.1 | 27.0 | 27.0 | 27.1 | 26.4 | 24.4 | 27.5 | 25.3 | 26.4 | 25.9 | 25.3 | 25.7 | 28.2 | 25.5 | 26.3 | 27.8 | 26.6 | -2.1 |
| Peak_chip | 18.1 | 17.9 | 17.2 | 17.4 | 16.6 | 16.3 | 16.5 | 16.9 | 16.8 | 16.7 | 16.5 | 16.1 | 16.5 | 16.4 | 16.3 | 15.8 | 16.0 | -11.8 |
| S298 | 32.0 | 32.5 | 29.4 | 31.0 | 29.6 | 29.4 | 30.4 | 30.7 | 30.1 | 29.3 | 29.0 | 29.6 | 29.9 | 29.1 | 29.5 | 28.5 | 28.8 | -10.0 |
| S38417 | 20.2 | 20.5 | 19.3 | 19.8 | 19.3 | 19.0 | 19.1 | 19.0 | 19.0 | 19.4 | 19.3 | 19.1 | 19.0 | 18.8 | 18.8 | 19.8 | 19.4 | -4.0 |
| S38584.1 | 15.2 | 15.4 | 15.0 | 15.1 | 14.9 | 14.6 | 15.3 | 14.8 | 14.9 | 15.0 | 14.6 | 14.7 | 14.5 | 14.4 | 14.4 | 14.5 | 14.5 | -4.5 |
| Scale125_chip | 24.3 | 23.4 | 22.7 | 22.4 | 22.3 | 22.4 | 22.0 | 22.1 | 22.0 | 21.6 | 21.2 | 21.3 | 20.8 | 21.0 | 21.2 | 20.7 | 21.1 | -13.2 |
| Scale2_chip | 18.8 | 18.6 | 17.8 | 17.8 | 17.5 | 17.1 | 17.3 | 17.0 | 17.3 | 17.5 | 16.9 | 17.1 | 16.9 | 17.0 | 16.6 | 16.6 | 16.6 | -11.9 |
| Seq | 15.8 | 15.1 | 15.6 | 15.8 | 15.8 | 15.5 | 15.4 | 15.5 | 14.7 | 15.7 | 14.9 | 15.4 | 15.0 | 14.8 | 14.9 | 14.9 | 14.7 | -7.4 |
| Spla | 22.9 | 23.0 | 23.4 | 22.6 | 23.7 | 21.8 | 22.5 | 22.1 | 20.8 | 21.8 | 21.8 | 24.3 | 24.2 | 23.0 | 22.1 | 22.1 | 22.0 | -4.0 |
| Tseng | 18.2 | 17.5 | 16.9 | 16.5 | 16.0 | 15.7 | 16.0 | 15.7 | 15.6 | 16.1 | 15.5 | 15.4 | 15.4 | 15.0 | 15.3 | 15.0 | 15.2 | -16.5 |
| Warping | 11.7 | 11.4 | 11.2 | 11.1 | 11.0 | 10.6 | 10.9 | 10.9 | 10.8 | 11.4 | 10.7 | 10.8 | 10.7 | 10.8 | 10.8 | 10.6 | 10.7 | -9.1 |
| **Geometric Avg** | 18.8 | 18.7 | 18.3 | 18.2 | 18.2 | 17.9 | 18.0 | 17.8 | 17.8 | 18.0 | 17.6 | 17.8 | 17.7 | 17.5 | 17.6 | 17.5 | 17.5 | -7.2 |

*Table A.14 – Delay vs # of NN Interconnects for Manhattan Radius 1 & 2*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 22.4 | 22.5 | 22.6 | 22.7 | 22.8 | 22.8 | 22.9 | 23.0 | 23.1 | 23.2 | 23.2 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 23.7 | 5.7 |
| Apex2 | 32.9 | 33.0 | 33.2 | 33.3 | 33.4 | 33.5 | 33.6 | 33.7 | 33.8 | 33.9 | 34.0 | 34.1 | 34.2 | 34.3 | 34.4 | 34.5 | 34.6 | 5.2 |
| Apex4 | 22.6 | 22.7 | 22.7 | 22.8 | 22.9 | 23.0 | 23.0 | 23.1 | 23.2 | 23.2 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 23.7 | 23.7 | 5.1 |
| Bigkey | 26.6 | 26.7 | 26.9 | 27.0 | 27.2 | 27.3 | 27.5 | 27.6 | 27.8 | 28.0 | 28.2 | 28.5 | 28.6 | 28.8 | 28.9 | 29.0 | 29.2 | 9.9 |
| Clma | 152.1 | 152.8 | 153.6 | 154.3 | 155.0 | 155.8 | 156.2 | 156.7 | 157.2 | 157.6 | 158.1 | 158.5 | 159.0 | 159.4 | 159.9 | 160.4 | 160.8 | 5.7 |
| Des | 35.3 | 35.5 | 35.7 | 35.9 | 36.1 | 36.4 | 36.7 | 37.0 | 37.4 | 37.6 | 37.8 | 38.0 | 38.3 | 38.6 | 38.8 | 39.0 | 39.3 | 11.2 |
| Diffeq | 19.9 | 20.0 | 20.1 | 20.1 | 20.2 | 20.3 | 20.4 | 20.5 | 20.6 | 20.6 | 20.7 | 20.8 | 20.9 | 20.9 | 21.0 | 21.1 | 21.2 | 6.4 |
| Display_chip | 20.5 | 20.6 | 20.7 | 20.7 | 20.8 | 20.9 | 21.0 | 21.1 | 21.2 | 21.4 | 21.5 | 21.7 | 21.8 | 21.9 | 22.0 | 22.1 | 22.2 | 8.4 |
| Dsip | 26.2 | 26.3 | 26.5 | 26.6 | 26.8 | 26.9 | 27.2 | 27.4 | 27.6 | 27.8 | 27.9 | 28.1 | 28.3 | 28.5 | 28.7 | 28.8 | 29.0 | 10.7 |
| Elliptic | 58.9 | 59.1 | 59.3 | 59.5 | 59.7 | 59.9 | 60.1 | 60.3 | 60.5 | 60.7 | 60.9 | 61.1 | 61.3 | 61.5 | 61.6 | 61.8 | 62.0 | 5.4 |
| Ex1010 | 76.6 | 76.8 | 77.1 | 77.4 | 77.6 | 77.9 | 78.1 | 78.4 | 78.6 | 78.9 | 79.1 | 79.4 | 79.6 | 79.9 | 80.1 | 80.4 | 80.6 | 5.3 |
| Ex5p | 18.5 | 18.5 | 18.6 | 18.7 | 18.7 | 18.8 | 18.8 | 18.9 | 19.0 | 19.0 | 19.1 | 19.1 | 19.2 | 19.2 | 19.3 | 19.3 | 19.4 | 4.9 |
| Frisc | 60.4 | 60.5 | 60.7 | 60.9 | 61.1 | 61.3 | 61.5 | 61.7 | 61.9 | 62.0 | 62.2 | 62.4 | 62.6 | 62.8 | 63.0 | 63.3 | 63.6 | 5.4 |
| Img_calc | 152.4 | 153.0 | 153.5 | 154.1 | 154.6 | 155.2 | 155.7 | 156.3 | 156.8 | 157.4 | 157.9 | 158.5 | 159.0 | 159.5 | 160.1 | 160.6 | 161.2 | 5.7 |
| Img_interp | 32.5 | 32.7 | 33.0 | 33.2 | 33.5 | 33.7 | 33.8 | 34.0 | 34.2 | 34.3 | 34.4 | 34.6 | 34.7 | 34.9 | 35.0 | 35.2 | 35.3 | 8.6 |
| Input_chip | 8.8 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 9.2 | 9.2 | 9.3 | 9.3 | 9.3 | 9.4 | 9.4 | 9.5 | 9.5 | 7.9 |
| Misex3 | 22.9 | 23.0 | 23.0 | 23.1 | 23.2 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 23.7 | 23.8 | 23.9 | 23.9 | 24.0 | 24.1 | 24.2 | 5.6 |
| Pdc | 97.8 | 98.1 | 98.4 | 98.6 | 98.9 | 99.1 | 99.4 | 99.6 | 99.9 | 100.1 | 100.4 | 100.6 | 100.9 | 101.1 | 101.4 | 101.6 | 101.9 | 4.1 |
| Peak_chip | 8.4 | 8.5 | 8.5 | 8.6 | 8.6 | 8.7 | 8.7 | 8.7 | 8.8 | 8.8 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 8.3 |
| S298 | 25.2 | 25.3 | 25.4 | 25.6 | 25.7 | 25.8 | 25.9 | 26.0 | 26.1 | 26.2 | 26.3 | 26.4 | 26.5 | 26.6 | 26.7 | 26.8 | 26.9 | 6.8 |
| S38417 | 93.7 | 94.1 | 94.4 | 94.8 | 95.1 | 95.5 | 95.8 | 96.2 | 96.5 | 96.9 | 97.2 | 97.6 | 97.9 | 98.3 | 98.6 | 99.0 | 99.3 | 6.0 |
| S38584.1 | 89.4 | 89.8 | 90.1 | 90.5 | 90.9 | 91.2 | 91.6 | 91.9 | 92.3 | 92.6 | 93.0 | 93.3 | 93.7 | 94.0 | 94.3 | 94.7 | 95.0 | 6.3 |
| Scale125_chip | 29.5 | 29.6 | 29.7 | 29.9 | 30.0 | 30.2 | 30.4 | 30.6 | 30.8 | 31.0 | 31.1 | 31.2 | 31.4 | 31.6 | 31.8 | 31.9 | 32.1 | 8.8 |
| Scale2_chip | 12.6 | 12.7 | 12.7 | 12.8 | 12.8 | 12.9 | 13.0 | 13.0 | 13.1 | 13.2 | 13.2 | 13.3 | 13.4 | 13.4 | 13.5 | 13.5 | 13.6 | 8.2 |
| Seq | 29.0 | 29.1 | 29.2 | 29.3 | 29.4 | 29.5 | 29.6 | 29.7 | 29.8 | 29.9 | 30.0 | 30.1 | 30.2 | 30.3 | 30.4 | 30.5 | 30.6 | 5.4 |
| Spla | 70.3 | 70.5 | 70.7 | 70.9 | 71.1 | 71.3 | 71.5 | 71.7 | 71.9 | 72.1 | 72.3 | 72.5 | 72.7 | 72.9 | 73.1 | 73.3 | 73.5 | 4.5 |
| Tseng | 13.8 | 13.9 | 14.0 | 14.0 | 14.1 | 14.1 | 14.2 | 14.3 | 14.3 | 14.4 | 14.4 | 14.5 | 14.5 | 14.6 | 14.6 | 14.7 | 14.8 | 6.6 |
| Warping | 15.1 | 15.2 | 15.3 | 15.4 | 15.4 | 15.5 | 15.6 | 15.7 | 15.7 | 15.8 | 15.9 | 16.1 | 16.1 | 16.2 | 16.3 | 16.3 | 16.4 | 8.4 |
| **Geometric Avg** | 33.1 | 33.2 | 33.4 | 33.5 | 33.6 | 33.8 | 33.9 | 34.1 | 34.2 | 34.4 | 34.5 | 34.6 | 34.8 | 34.9 | 35.1 | 35.2 | 35.3 | 6.8 |

*Table A.15 – Area vs # of NN Interconnects for Manhattan Radius 1 & 2 (Measured Under Constant Track Count)*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 15.7 | 15.2 | 15.3 | 14.7 | 15.5 | 15.2 | 15.2 | 15.1 | 15.0 | 15.0 | 15.4 | 14.9 | 15.2 | 14.9 | 15.3 | 15.0 | 14.7 | -6.6 |
| Apex2 | 17.0 | 17.1 | 16.9 | 17.4 | 16.8 | 16.9 | 17.2 | 17.0 | 17.0 | 17.1 | 17.1 | 17.1 | 16.6 | 16.8 | 16.7 | 16.8 | 16.9 | -0.7 |
| Apex4 | 15.8 | 15.3 | 15.4 | 15.6 | 15.2 | 15.9 | 15.3 | 15.2 | 15.4 | 15.7 | 15.4 | 15.5 | 15.4 | 15.3 | 15.4 | 15.5 | 15.1 | -4.5 |
| Bigkey | 8.8 | 8.7 | 8.5 | 8.8 | 8.7 | 8.5 | 8.6 | 8.6 | 8.2 | 8.7 | 8.4 | 8.6 | 8.1 | 8.9 | 8.5 | 8.6 | 8.1 | -7.9 |
| Clma | 34.2 | 34.9 | 33.7 | 35.3 | 33.3 | 34.0 | 32.4 | 33.5 | 33.5 | 32.7 | 32.6 | 32.1 | 31.2 | 33.4 | 32.6 | 33.7 | 31.4 | -8.3 |
| Des | 15.6 | 15.3 | 15.8 | 15.2 | 15.6 | 14.8 | 15.2 | 14.9 | 15.4 | 15.2 | 15.1 | 15.5 | 15.1 | 14.7 | 14.9 | 15.6 | 14.8 | -5.1 |
| Diffeq | 18.2 | 17.5 | 17.1 | 16.7 | 16.6 | 16.8 | 16.1 | 16.0 | 15.9 | 16.3 | 15.6 | 15.6 | 15.3 | 15.4 | 15.6 | 15.5 | 15.3 | -15.9 |
| Display_chip | 16.6 | 16.7 | 16.4 | 15.9 | 16.2 | 15.9 | 15.7 | 16.1 | 15.5 | 15.5 | 15.4 | 15.4 | 15.2 | 15.1 | 15.2 | 15.1 | 15.1 | -9.5 |
| Dsip | 8.0 | 8.1 | 8.1 | 8.5 | 8.6 | 8.2 | 8.1 | 8.1 | 8.2 | 8.0 | 8.0 | 8.1 | 8.1 | 8.2 | 8.1 | 8.4 | 8.2 | 1.9 |
| Elliptic | 24.6 | 25.8 | 24.9 | 25.0 | 23.5 | 25.1 | 25.2 | 25.4 | 23.6 | 24.8 | 24.1 | 24.9 | 24.0 | 24.2 | 23.6 | 24.5 | 24.1 | -2.2 |
| Ex1010 | 26.3 | 26.0 | 24.6 | 25.9 | 24.4 | 24.7 | 24.4 | 24.4 | 25.3 | 24.3 | 25.2 | 24.7 | 24.4 | 24.3 | 24.6 | 25.2 | 25.0 | -5.0 |
| Ex5p | 14.9 | 15.6 | 15.1 | 15.0 | 15.6 | 15.0 | 15.1 | 15.4 | 15.3 | 15.3 | 15.8 | 15.3 | 15.4 | 15.0 | 15.1 | 15.5 | 15.0 | 0.1 |
| Frisc | 30.4 | 30.2 | 30.3 | 29.2 | 29.2 | 28.6 | 28.2 | 28.7 | 28.3 | 29.0 | 27.9 | 28.6 | 28.5 | 28.8 | 27.6 | 27.9 | 28.1 | -7.4 |
| Img_calc | 39.5 | 38.3 | 38.2 | 36.8 | 35.6 | 35.2 | 35.1 | 34.9 | 34.8 | 35.5 | 35.1 | 34.6 | 35.2 | 34.2 | 34.0 | 34.1 | 33.9 | -14.4 |
| Img_interp | 22.4 | 21.3 | 20.6 | 20.9 | 20.9 | 20.5 | 20.4 | 20.7 | 20.5 | 20.6 | 19.9 | 20.3 | 20.1 | 19.8 | 20.4 | 19.9 | 19.7 | -12.1 |
| Input_chip | 15.4 | 15.5 | 14.7 | 14.8 | 14.6 | 14.1 | 13.9 | 14.0 | 13.7 | 14.1 | 13.5 | 13.4 | 13.4 | 13.2 | 13.1 | 13.2 | 13.3 | -13.7 |
| Misex3 | 15.3 | 15.0 | 15.1 | 14.2 | 14.7 | 14.5 | 14.6 | 14.9 | 14.7 | 14.5 | 14.1 | 14.3 | 14.0 | 14.9 | 14.3 | 14.2 | 13.9 | -9.2 |
| Pdc | 27.1 | 27.0 | 27.0 | 26.6 | 27.4 | 25.3 | 26.7 | 26.5 | 26.3 | 26.1 | 26.5 | 25.6 | 27.6 | 24.7 | 25.6 | 25.7 | 27.8 | 2.3 |
| Peak_chip | 18.1 | 17.9 | 17.2 | 17.1 | 16.9 | 16.8 | 16.3 | 16.8 | 16.4 | 16.9 | 16.3 | 16.3 | 15.8 | 16.2 | 16.0 | 16.0 | 16.0 | -11.6 |
| S298 | 32.0 | 32.5 | 29.4 | 30.6 | 29.8 | 30.2 | 29.5 | 30.9 | 29.5 | 30.8 | 29.7 | 29.2 | 29.9 | 30.8 | 29.2 | 29.0 | 29.7 | -7.3 |
| S38417 | 20.2 | 20.5 | 19.3 | 19.5 | 19.4 | 19.5 | 19.3 | 18.5 | 19.3 | 19.8 | 19.5 | 19.4 | 19.3 | 18.7 | 18.9 | 18.8 | 18.8 | -6.5 |
| S38584.1 | 15.2 | 15.4 | 15.0 | 14.7 | 15.1 | 14.9 | 14.8 | 14.9 | 14.9 | 15.1 | 14.7 | 14.7 | 14.7 | 14.6 | 14.8 | 14.6 | 14.6 | -3.9 |
| Scale125_chip | 24.3 | 23.4 | 22.7 | 22.4 | 22.2 | 22.6 | 21.6 | 22.1 | 22.0 | 21.4 | 21.6 | 21.3 | 21.5 | 21.5 | 21.1 | 21.5 | 21.0 | -13.8 |
| Scale2_chip | 18.8 | 18.6 | 17.8 | 17.8 | 17.5 | 17.1 | 17.2 | 16.9 | 16.9 | 17.1 | 16.9 | 16.9 | 17.0 | 16.3 | 16.7 | 16.5 | 16.5 | -12.4 |
| Seq | 15.8 | 15.1 | 15.6 | 15.7 | 15.2 | 15.0 | 15.4 | 15.3 | 15.4 | 15.4 | 15.5 | 14.8 | 15.3 | 15.5 | 14.9 | 14.8 | 15.0 | -5.2 |
| Spla | 22.9 | 23.0 | 23.4 | 21.2 | 23.3 | 22.5 | 21.9 | 21.6 | 21.5 | 21.9 | 22.5 | 23.1 | 23.4 | 22.7 | 22.4 | 23.2 | 22.5 | -1.7 |
| Tseng | 18.2 | 17.5 | 16.9 | 16.5 | 15.8 | 16.1 | 15.6 | 15.8 | 15.6 | 16.0 | 15.2 | 15.2 | 15.5 | 15.4 | 15.2 | 15.2 | 15.1 | -16.8 |
| Warping | 11.7 | 11.4 | 11.2 | 11.2 | 10.8 | 10.8 | 10.8 | 10.8 | 10.8 | 11.5 | 10.7 | 10.9 | 10.7 | 10.9 | 10.9 | 10.8 | 10.7 | -9.1 |
| **Geometric Avg** | 18.8 | 18.7 | 18.3 | 18.2 | 18.1 | 17.9 | 17.8 | 17.9 | 17.7 | 17.9 | 17.7 | 17.7 | 17.6 | 17.6 | 17.5 | 17.6 | 17.4 | -7.5 |

*Table A.16 – Delay vs # of NN Interconnects for Manhattan Radius 1 & 2 Using 180-Degree Output Fan-out Pattern*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 19.9 | 19.9 | 19.9 | 19.7 | 19.8 | 19.8 | 19.8 | 20.0 | 19.6 | 20.0 | 19.9 | 19.8 | 20.1 | 20.1 | 20.3 | 20.1 | 20.3 | 1.9 |
| Apex2 | 29.1 | 28.6 | 29.0 | 29.0 | 28.6 | 29.3 | 28.9 | 28.9 | 29.2 | 29.2 | 29.1 | 29.1 | 29.4 | 29.3 | 29.4 | 29.7 | 29.6 | 1.9 |
| Apex4 | 20.0 | 19.9 | 19.9 | 19.7 | 19.9 | 19.9 | 19.8 | 20.0 | 20.2 | 20.2 | 20.2 | 20.3 | 20.2 | 20.2 | 20.4 | 20.2 | 20.6 | 2.9 |
| Bigkey | 23.8 | 23.6 | 23.8 | 24.1 | 23.9 | 24.0 | 24.2 | 24.5 | 24.7 | 24.3 | 24.5 | 24.9 | 24.9 | 25.2 | 24.9 | 25.7 | 25.1 | 5.5 |
| Clma | 133.4 | 134.1 | 135.2 | 134.7 | 135.4 | 136.1 | 134.8 | 134.5 | 135.4 | 136.1 | 134.9 | 137.3 | 136.4 | 138.9 | 138.5 | 137.8 | 138.2 | 3.6 |
| Des | 31.5 | 31.2 | 30.9 | 30.9 | 30.9 | 31.4 | 31.0 | 31.6 | 31.5 | 32.2 | 32.2 | 32.6 | 32.4 | 32.8 | 32.2 | 32.8 | 32.8 | 3.9 |
| Diffeq | 17.7 | 17.5 | 17.6 | 17.7 | 17.6 | 17.6 | 17.4 | 17.6 | 17.7 | 17.8 | 17.6 | 17.6 | 18.0 | 17.7 | 17.8 | 17.9 | 17.9 | 1.1 |
| Display_chip | 18.7 | 18.7 | 18.4 | 18.6 | 18.4 | 18.5 | 18.4 | 18.5 | 18.5 | 18.7 | 18.8 | 18.7 | 18.9 | 19.1 | 19.2 | 19.2 | 19.2 | 2.7 |
| Dsip | 23.2 | 23.4 | 23.5 | 23.5 | 23.0 | 23.5 | 23.8 | 23.8 | 24.2 | 23.9 | 24.4 | 24.4 | 24.0 | 24.2 | 24.6 | 25.0 | 24.4 | 5.2 |
| Elliptic | 52.2 | 52.1 | 52.4 | 51.9 | 52.0 | 51.5 | 53.1 | 53.0 | 52.4 | 53.7 | 53.2 | 53.2 | 53.2 | 53.8 | 53.9 | 53.8 | 53.8 | 2.9 |
| Ex1010 | 67.8 | 67.8 | 67.6 | 68.6 | 68.1 | 67.6 | 68.4 | 67.9 | 68.3 | 68.6 | 68.9 | 68.4 | 69.1 | 69.6 | 69.1 | 69.4 | 69.8 | 3.0 |
| Ex5p | 16.6 | 16.4 | 16.5 | 16.7 | 16.5 | 16.6 | 16.7 | 16.8 | 16.9 | 17.0 | 16.8 | 16.9 | 16.7 | 17.1 | 17.0 | 17.1 | 16.9 | 1.9 |
| Frisc | 53.1 | 53.5 | 52.5 | 52.9 | 53.5 | 53.7 | 53.5 | 53.3 | 53.1 | 54.2 | 54.0 | 54.4 | 53.9 | 54.8 | 54.9 | 55.3 | 55.2 | 3.9 |
| Img_calc | 135.1 | 136.4 | 135.3 | 135.5 | 134.1 | 134.7 | 135.3 | 135.7 | 135.4 | 137.5 | 136.6 | 136.7 | 136.1 | 138.2 | 138.5 | 137.8 | 138.3 | 2.3 |
| Img_interp | 29.4 | 29.8 | 29.4 | 28.9 | 29.0 | 28.9 | 29.1 | 29.1 | 29.4 | 29.8 | 29.5 | 29.7 | 29.6 | 29.9 | 29.8 | 29.8 | 29.7 | 0.9 |
| Input_chip | 8.2 | 8.2 | 8.2 | 8.2 | 8.1 | 8.1 | 8.1 | 8.2 | 8.0 | 8.2 | 8.2 | 8.1 | 8.1 | 8.1 | 8.2 | 8.2 | 8.2 | 0.5 |
| Misex3 | 20.3 | 19.9 | 20.2 | 20.0 | 20.2 | 20.3 | 20.1 | 20.3 | 20.3 | 20.6 | 20.6 | 20.5 | 20.6 | 20.7 | 20.8 | 20.6 | 20.8 | 2.2 |
| Pdc | 85.2 | 83.8 | 84.4 | 83.9 | 85.1 | 85.0 | 84.7 | 85.1 | 87.1 | 85.4 | 85.2 | 85.3 | 85.3 | 86.8 | 86.7 | 87.3 | 87.0 | 2.0 |
| Peak_chip | 7.7 | 8.0 | 8.0 | 7.8 | 7.8 | 7.8 | 7.7 | 7.9 | 7.8 | 8.0 | 7.8 | 7.9 | 7.9 | 7.9 | 7.9 | 7.9 | 7.9 | 2.0 |
| S298 | 22.1 | 21.9 | 21.5 | 21.6 | 21.7 | 21.8 | 22.0 | 22.3 | 22.0 | 22.2 | 22.4 | 22.1 | 22.5 | 22.6 | 22.6 | 22.5 | 22.8 | 3.3 |
| S38417 | 83.3 | 83.7 | 84.0 | 83.0 | 83.1 | 82.9 | 83.2 | 82.8 | 83.4 | 84.0 | 84.3 | 85.0 | 83.7 | 84.7 | 84.6 | 85.3 | 85.2 | 2.3 |
| S38584.1 | 80.7 | 80.2 | 80.4 | 80.9 | 79.8 | 80.5 | 80.8 | 81.2 | 80.6 | 81.6 | 80.2 | 80.9 | 81.5 | 80.9 | 81.7 | 82.3 | 82.6 | 2.4 |
| Scale125_chip | 26.6 | 27.0 | 26.5 | 26.4 | 26.5 | 26.3 | 26.3 | 26.3 | 26.5 | 26.5 | 26.7 | 26.6 | 27.0 | 27.1 | 26.7 | 26.9 | 27.2 | 2.2 |
| Scale2_chip | 11.7 | 11.6 | 11.5 | 11.3 | 11.5 | 11.4 | 11.4 | 11.4 | 11.6 | 11.6 | 11.5 | 11.6 | 11.7 | 11.7 | 11.8 | 11.7 | 11.9 | 1.9 |
| Seq | 25.8 | 26.1 | 26.0 | 25.9 | 25.8 | 26.1 | 26.2 | 26.4 | 26.2 | 26.5 | 26.6 | 26.5 | 26.6 | 26.8 | 27.0 | 26.7 | 26.8 | 3.9 |
| Spla | 61.4 | 60.7 | 61.1 | 62.2 | 61.5 | 60.9 | 61.7 | 61.4 | 62.1 | 62.1 | 62.5 | 61.9 | 62.9 | 63.3 | 62.1 | 62.8 | 64.1 | 4.4 |
| Tseng | 12.2 | 12.2 | 12.1 | 12.1 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.3 | 12.4 | 12.3 | 12.5 | 12.4 | 12.5 | 12.5 | 12.5 | 1.8 |
| Warping | 13.7 | 13.6 | 13.7 | 13.7 | 13.6 | 13.6 | 13.7 | 13.9 | 13.7 | 13.9 | 13.7 | 13.9 | 13.9 | 13.9 | 14.1 | 14.0 | 14.1 | 3.4 |
| **Geometric Avg** | 29.5 | 29.5 | 29.5 | 29.4 | 29.4 | 29.4 | 29.5 | 29.6 | 29.7 | 29.9 | 29.8 | 29.9 | 30.0 | 30.2 | 30.2 | 30.3 | 30.3 | 2.7 |

*Table A.17 – Area vs # of NN Interconnects for Manhattan Radius 1 & 2 (Measured Under Varying Track Count)*

| Circuit | Wmin For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Wmin (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 30 | 29 | 29 | 29 | 29 | 28 | 28 | 29 | 27 | 28 | 28 | 27 | 28 | 28 | 28 | 27 | 28 | -8.0 |
| Apex2 | 36 | 35 | 36 | 36 | 35 | 36 | 35 | 35 | 35 | 35 | 34 | 34 | 35 | 34 | 34 | 35 | 34 | -5.0 |
| Apex4 | 36 | 35 | 35 | 34 | 35 | 34 | 34 | 34 | 35 | 35 | 34 | 34 | 34 | 34 | 34 | 33 | 34 | -5.0 |
| Bigkey | 20 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 20 | 19 | 19 | 19 | 19 | 19 | 18 | 20 | 18 | -8.0 |
| Clma | 44 | 44 | 44 | 44 | 44 | 44 | 43 | 43 | 43 | 43 | 42 | 43 | 43 | 44 | 43 | 43 | 43 | -2.7 |
| Des | 21 | 21 | 20 | 20 | 20 | 20 | 19 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | 19 | 19 | -9.5 |
| Diffeq | 25 | 25 | 25 | 25 | 24 | 24 | 23 | 24 | 24 | 24 | 23 | 23 | 23 | 23 | 22 | 22 | 22 | -11.2 |
| Display_chip | 20 | 20 | 19 | 20 | 19 | 19 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | -11.0 |
| Dsip | 21 | 21 | 21 | 21 | 20 | 20 | 20 | 20 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | -8.6 |
| Elliptic | 37 | 36 | 36 | 36 | 36 | 35 | 36 | 36 | 35 | 36 | 36 | 35 | 35 | 36 | 35 | 35 | 35 | -5.4 |
| Ex1010 | 37 | 37 | 37 | 37 | 37 | 36 | 37 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | -3.2 |
| Ex5p | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 35 | 36 | 35 | 36 | 35 | 35 | 34 | -4.4 |
| Frisc | 41 | 41 | 40 | 40 | 40 | 40 | 40 | 39 | 39 | 40 | 40 | 40 | 39 | 40 | 40 | 40 | 40 | -3.4 |
| Img_calc | 35 | 35 | 35 | 34 | 34 | 34 | 34 | 34 | 33 | 34 | 33 | 33 | 33 | 33 | 33 | 33 | 33 | -6.9 |
| Img_interp | 22 | 23 | 22 | 21 | 21 | 21 | 21 | 20 | 21 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | -11.8 |
| Input_chip | 17 | 17 | 17 | 17 | 16 | 16 | 16 | 16 | 15 | 16 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | -14.1 |
| Misex3 | 32 | 30 | 31 | 30 | 31 | 31 | 30 | 30 | 30 | 31 | 30 | 30 | 30 | 30 | 30 | 29 | 30 | -6.9 |
| Pdc | 53 | 51 | 51 | 51 | 52 | 51 | 51 | 51 | 52 | 51 | 50 | 50 | 50 | 51 | 50 | 51 | 50 | -5.3 |
| Peak_chip | 15 | 16 | 16 | 15 | 15 | 15 | 14 | 15 | 14 | 15 | 14 | 14 | 14 | 13 | 14 | 13 | 13 | -13.3 |
| S298 | 24 | 23 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 21 | 22 | 22 | 21 | 21 | 21 | -11.7 |
| S38417 | 32 | 32 | 32 | 31 | 31 | 31 | 31 | 30 | 30 | 31 | 31 | 31 | 30 | 30 | 30 | 30 | 30 | -6.9 |
| S38584.1 | 30 | 30 | 30 | 30 | 29 | 29 | 29 | 29 | 29 | 29 | 28 | 28 | 28 | 28 | 28 | 28 | 28 | -6.0 |
| Scale125_chip | 21 | 21 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 19 | 19 | 18 | 19 | 19 | 18 | 18 | 18 | -14.3 |
| Scale2_chip | 17 | 17 | 16 | 16 | 16 | 15 | 15 | 15 | 16 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | -11.8 |
| Seq | 34 | 35 | 34 | 34 | 33 | 34 | 34 | 34 | 33 | 34 | 34 | 34 | 34 | 34 | 34 | 33 | 33 | -2.4 |
| Spla | 46 | 45 | 45 | 46 | 45 | 44 | 45 | 44 | 45 | 45 | 45 | 44 | 45 | 45 | 44 | 44 | 45 | -1.7 |
| Tseng | 23 | 23 | 22 | 22 | 22 | 22 | 22 | 22 | 21 | 22 | 22 | 21 | 22 | 21 | 21 | 21 | 21 | -10.4 |
| Warping | 19 | 19 | 18 | 18 | 18 | 18 | 18 | 18 | 17 | 18 | 17 | 17 | 17 | 17 | 17 | 17 | 17 | -10.5 |
| **Geometric Avg** | 27.9 | 27.7 | 27.4 | 27.1 | 26.8 | 26.7 | 26.5 | 26.5 | 26.3 | 26.5 | 26.2 | 26.1 | 26.0 | 26.1 | 25.9 | 25.8 | 25.6 | -7.9 |

*Table A.18 - $W_{min}$ vs # of NN Interconnects for Manhattan Radius 1 & 2*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 15.7 | 15.8 | 15.4 | 15.5 | 15.5 | 15.4 | 15.1 | 15.0 | 15.5 | 15.4 | 15.6 | 15.1 | 15.3 | 15.2 | 15.4 | 14.7 | 15.1 | -3.6 |
| Apex2 | 17.0 | 17.6 | 17.3 | 17.4 | 16.9 | 17.2 | 17.3 | 16.8 | 17.2 | 17.0 | 16.8 | 17.0 | 16.7 | 16.7 | 16.7 | 16.7 | 16.8 | -1.4 |
| Apex4 | 15.8 | 15.5 | 15.8 | 15.7 | 15.6 | 15.3 | 15.3 | 15.1 | 14.5 | 15.0 | 15.0 | 15.1 | 15.2 | 15.5 | 14.7 | 15.2 | 15.3 | -3.0 |
| Bigkey | 8.8 | 8.9 | 8.4 | 8.6 | 8.2 | 8.4 | 8.8 | 8.4 | 8.6 | 8.6 | 8.4 | 8.4 | 8.3 | 8.4 | 8.7 | 8.3 | 8.5 | -3.6 |
| Clma | 34.2 | 33.6 | 32.5 | 33.0 | 33.7 | 34.4 | 32.5 | 34.9 | 34.6 | 33.8 | 33.3 | 33.3 | 33.8 | 32.4 | 35.0 | 33.1 | 32.4 | -5.5 |
| Des | 15.6 | 15.3 | 15.9 | 15.5 | 15.8 | 15.5 | 15.1 | 15.2 | 15.1 | 15.3 | 14.9 | 14.9 | 15.1 | 15.1 | 14.8 | 14.9 | 15.0 | -4.3 |
| Diffeq | 18.2 | 18.1 | 17.4 | 17.2 | 16.5 | 16.4 | 16.6 | 16.2 | 16.0 | 16.6 | 16.1 | 15.8 | 16.1 | 15.9 | 15.5 | 15.7 | 15.8 | -13.2 |
| Display_chip | 16.6 | 16.5 | 16.2 | 16.1 | 16.0 | 15.9 | 15.8 | 15.5 | 15.7 | 15.9 | 15.7 | 15.6 | 15.6 | 15.7 | 15.5 | 15.7 | 15.3 | -8.3 |
| Dsip | 8.0 | 8.2 | 8.6 | 8.1 | 8.7 | 8.5 | 8.1 | 8.0 | 8.1 | 8.0 | 8.1 | 8.3 | 8.0 | 7.7 | 7.7 | 7.9 | 7.6 | -5.3 |
| Elliptic | 24.6 | 25.2 | 25.1 | 24.8 | 25.2 | 23.9 | 23.6 | 25.0 | 24.2 | 25.1 | 25.0 | 24.8 | 24.2 | 23.8 | 24.0 | 24.4 | 24.1 | -2.1 |
| Ex1010 | 26.3 | 25.3 | 24.8 | 25.1 | 24.7 | 25.3 | 25.3 | 24.6 | 24.4 | 24.2 | 24.4 | 24.1 | 24.9 | 24.6 | 25.3 | 24.5 | 24.2 | -8.2 |
| Ex5p | 14.9 | 15.4 | 15.3 | 15.5 | 15.2 | 15.3 | 15.5 | 14.9 | 15.3 | 15.7 | 15.5 | 15.1 | 15.4 | 15.3 | 15.3 | 15.0 | 15.2 | 1.7 |
| Frisc | 30.4 | 30.4 | 29.8 | 29.8 | 29.6 | 29.3 | 28.8 | 28.9 | 29.0 | 29.7 | 29.1 | 28.6 | 28.8 | 28.7 | 28.4 | 27.9 | 28.0 | -7.6 |
| Img_calc | 39.5 | 39.7 | 39.5 | 37.7 | 37.0 | 36.1 | 35.8 | 36.4 | 35.6 | 36.5 | 36.0 | 35.8 | 35.1 | 35.1 | 35.3 | 35.0 | 35.0 | -11.4 |
| Img_interp | 22.4 | 22.8 | 21.3 | 21.3 | 20.8 | 21.2 | 20.9 | 21.2 | 20.8 | 21.2 | 20.7 | 20.5 | 20.6 | 20.3 | 20.5 | 20.4 | 20.3 | -9.3 |
| Input_chip | 15.4 | 15.4 | 14.5 | 14.2 | 13.8 | 13.9 | 13.5 | 13.9 | 13.8 | 14.3 | 14.0 | 13.9 | 13.9 | 13.7 | 14.0 | 13.4 | 13.4 | -12.8 |
| Misex3 | 15.3 | 15.4 | 15.0 | 14.9 | 14.3 | 14.5 | 14.5 | 14.3 | 14.7 | 14.8 | 14.7 | 14.1 | 14.5 | 14.3 | 14.4 | 14.2 | 14.2 | -7.1 |
| Pdc | 27.1 | 26.9 | 26.3 | 26.5 | 24.8 | 25.7 | 29.4 | 27.3 | 26.7 | 25.4 | 24.4 | 28.4 | 26.4 | 26.5 | 27.1 | 25.4 | 27.0 | -0.5 |
| Peak_chip | 18.1 | 18.6 | 17.6 | 17.4 | 17.4 | 17.3 | 17.0 | 17.0 | 16.8 | 16.8 | 16.7 | 16.4 | 16.4 | 16.5 | 16.3 | 16.7 | 16.5 | -9.0 |
| S298 | 32.0 | 31.7 | 31.8 | 31.8 | 31.4 | 31.2 | 30.1 | 30.3 | 30.5 | 29.3 | 30.2 | 32.0 | 29.0 | 30.0 | 29.0 | 29.8 | 29.9 | -6.6 |
| S38417 | 20.2 | 20.8 | 20.4 | 20.1 | 19.8 | 19.7 | 19.2 | 19.5 | 19.5 | 19.6 | 19.2 | 19.8 | 18.6 | 19.0 | 19.2 | 18.9 | 18.7 | -7.0 |
| S38584.1 | 15.2 | 15.1 | 15.0 | 15.2 | 15.1 | 15.2 | 15.0 | 14.9 | 15.0 | 14.8 | 14.9 | 15.0 | 14.8 | 14.6 | 14.6 | 14.8 | 14.9 | -1.5 |
| Scale125_chip | 24.3 | 23.7 | 22.7 | 22.4 | 22.4 | 22.1 | 22.3 | 22.1 | 21.5 | 22.6 | 21.9 | 21.8 | 21.6 | 21.7 | 22.1 | 21.5 | 21.3 | -12.7 |
| Scale2_chip | 18.8 | 18.7 | 18.6 | 18.0 | 17.5 | 17.6 | 17.5 | 17.1 | 17.7 | 17.4 | 17.2 | 17.3 | 17.1 | 17.1 | 16.9 | 17.2 | 17.2 | -8.6 |
| Seq | 15.8 | 15.5 | 15.4 | 15.0 | 15.2 | 15.2 | 15.5 | 15.9 | 15.8 | 15.2 | 15.7 | 14.9 | 15.2 | 15.2 | 14.9 | 15.0 | 15.1 | -4.6 |
| Spla | 22.9 | 22.6 | 21.4 | 21.2 | 21.5 | 22.9 | 23.0 | 22.8 | 22.0 | 21.6 | 21.9 | 24.5 | 21.7 | 20.8 | 22.3 | 23.5 | 21.1 | -7.7 |
| Tseng | 18.2 | 18.2 | 17.6 | 16.9 | 16.7 | 16.0 | 16.2 | 15.9 | 16.0 | 16.8 | 16.0 | 16.0 | 15.9 | 15.6 | 15.8 | 15.8 | 15.4 | -15.5 |
| Warping | 11.7 | 11.2 | 11.2 | 11.3 | 10.9 | 10.7 | 10.8 | 10.8 | 10.6 | 11.4 | 10.9 | 10.7 | 10.7 | 10.5 | 10.5 | 10.7 | 10.6 | -9.9 |
| **Geometric Avg** | 18.8 | 18.8 | 18.5 | 18.3 | 18.1 | 18.1 | 18.1 | 18.0 | 17.9 | 18.1 | 17.9 | 17.9 | 17.7 | 17.6 | 17.7 | 17.6 | 17.6 | -6.8 |

*Table A.19 – Delay vs # of NN Interconnects for Cross Radius 1 & 2*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 22.4 | 22.5 | 22.6 | 22.7 | 22.7 | 22.8 | 22.9 | 23.0 | 23.0 | 23.1 | 23.2 | 23.3 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 5.3 |
| Apex2 | 32.9 | 33.0 | 33.1 | 33.3 | 33.4 | 33.5 | 33.6 | 33.7 | 33.8 | 33.9 | 34.0 | 34.1 | 34.2 | 34.3 | 34.3 | 34.4 | 34.5 | 4.9 |
| Apex4 | 22.6 | 22.7 | 22.7 | 22.8 | 22.9 | 22.9 | 23.0 | 23.1 | 23.1 | 23.2 | 23.3 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 23.6 | 4.7 |
| Bigkey | 26.6 | 26.7 | 26.9 | 27.0 | 27.2 | 27.3 | 27.4 | 27.6 | 27.7 | 28.0 | 28.2 | 28.4 | 28.5 | 28.6 | 28.8 | 28.9 | 29.0 | 9.3 |
| Clma | 152.1 | 152.8 | 153.5 | 154.3 | 155.0 | 155.7 | 156.1 | 156.6 | 157.1 | 157.5 | 157.9 | 158.4 | 158.8 | 159.2 | 159.7 | 160.1 | 160.6 | 5.5 |
| Des | 35.3 | 35.5 | 35.7 | 35.9 | 36.1 | 36.3 | 36.7 | 37.0 | 37.3 | 37.5 | 37.7 | 37.9 | 38.2 | 38.5 | 38.7 | 38.9 | 39.1 | 10.7 |
| Diffeq | 19.9 | 20.0 | 20.1 | 20.1 | 20.2 | 20.3 | 20.4 | 20.4 | 20.5 | 20.6 | 20.7 | 20.7 | 20.8 | 20.9 | 20.9 | 21.0 | 21.1 | 5.9 |
| Display_chip | 20.5 | 20.5 | 20.6 | 20.7 | 20.8 | 20.9 | 21.0 | 21.1 | 21.2 | 21.3 | 21.5 | 21.6 | 21.7 | 21.8 | 21.9 | 22.0 | 22.0 | 7.8 |
| Dsip | 26.2 | 26.3 | 26.4 | 26.6 | 26.7 | 26.9 | 27.1 | 27.3 | 27.6 | 27.7 | 27.8 | 28.0 | 28.2 | 28.4 | 28.5 | 28.7 | 28.8 | 10.1 |
| Elliptic | 58.9 | 59.1 | 59.3 | 59.5 | 59.7 | 59.8 | 60.0 | 60.2 | 60.4 | 60.6 | 60.8 | 61.0 | 61.2 | 61.3 | 61.5 | 61.7 | 61.9 | 5.1 |
| Ex1010 | 76.6 | 76.8 | 77.1 | 77.3 | 77.6 | 77.8 | 78.1 | 78.3 | 78.6 | 78.8 | 79.1 | 79.3 | 79.5 | 79.8 | 80.0 | 80.2 | 80.5 | 5.1 |
| Ex5p | 18.5 | 18.5 | 18.6 | 18.7 | 18.7 | 18.8 | 18.8 | 18.9 | 18.9 | 19.0 | 19.0 | 19.1 | 19.1 | 19.2 | 19.2 | 19.3 | 19.3 | 4.5 |
| Frisc | 60.4 | 60.5 | 60.7 | 60.9 | 61.1 | 61.3 | 61.4 | 61.6 | 61.8 | 62.0 | 62.1 | 62.3 | 62.5 | 62.7 | 62.9 | 63.2 | 63.4 | 5.1 |
| Img_calc | 152.4 | 153.0 | 153.5 | 154.1 | 154.6 | 155.1 | 155.7 | 156.2 | 156.8 | 157.3 | 157.8 | 158.3 | 158.8 | 159.4 | 159.9 | 160.4 | 160.9 | 5.6 |
| Img_interp | 32.5 | 32.7 | 33.0 | 33.2 | 33.4 | 33.6 | 33.8 | 33.9 | 34.1 | 34.2 | 34.4 | 34.5 | 34.6 | 34.8 | 34.9 | 35.0 | 35.2 | 8.2 |
| Input_chip | 8.8 | 8.9 | 8.9 | 8.9 | 9.0 | 9.0 | 9.1 | 9.1 | 9.2 | 9.2 | 9.2 | 9.3 | 9.3 | 9.3 | 9.4 | 9.4 | 9.4 | 7.2 |
| Misex3 | 22.9 | 23.0 | 23.0 | 23.1 | 23.2 | 23.3 | 23.4 | 23.4 | 23.5 | 23.6 | 23.6 | 23.7 | 23.8 | 23.9 | 23.9 | 24.0 | 24.1 | 5.2 |
| Pdc | 97.8 | 98.1 | 98.3 | 98.6 | 98.8 | 99.1 | 99.3 | 99.6 | 99.8 | 100.1 | 100.3 | 100.5 | 100.8 | 101.0 | 101.2 | 101.5 | 101.7 | 4.0 |
| Peak_chip | 8.4 | 8.5 | 8.5 | 8.6 | 8.6 | 8.6 | 8.7 | 8.7 | 8.8 | 8.8 | 8.8 | 8.9 | 8.9 | 8.9 | 9.0 | 9.0 | 9.1 | 7.5 |
| S298 | 25.2 | 25.3 | 25.4 | 25.5 | 25.6 | 25.7 | 25.9 | 26.0 | 26.1 | 26.2 | 26.2 | 26.3 | 26.4 | 26.5 | 26.6 | 26.7 | 26.8 | 6.3 |
| S38417 | 93.7 | 94.1 | 94.4 | 94.7 | 95.1 | 95.4 | 95.8 | 96.1 | 96.5 | 96.8 | 97.1 | 97.5 | 97.8 | 98.1 | 98.4 | 98.8 | 99.1 | 5.8 |
| S38584.1 | 89.4 | 89.8 | 90.1 | 90.5 | 90.8 | 91.2 | 91.5 | 91.9 | 92.2 | 92.5 | 92.9 | 93.2 | 93.5 | 93.8 | 94.2 | 94.5 | 94.8 | 6.0 |
| Scale125_chip | 29.5 | 29.6 | 29.7 | 29.9 | 30.0 | 30.1 | 30.3 | 30.6 | 30.8 | 30.9 | 31.0 | 31.1 | 31.3 | 31.5 | 31.7 | 31.8 | 31.9 | 8.3 |
| Scale2_chip | 12.6 | 12.6 | 12.7 | 12.8 | 12.8 | 12.9 | 13.0 | 13.0 | 13.1 | 13.1 | 13.2 | 13.2 | 13.3 | 13.4 | 13.4 | 13.5 | 13.5 | 7.5 |
| Seq | 29.0 | 29.1 | 29.2 | 29.3 | 29.4 | 29.5 | 29.6 | 29.7 | 29.8 | 29.9 | 30.0 | 30.0 | 30.1 | 30.2 | 30.3 | 30.4 | 30.5 | 5.0 |
| Spla | 70.3 | 70.5 | 70.7 | 70.9 | 71.1 | 71.3 | 71.5 | 71.7 | 71.9 | 72.0 | 72.2 | 72.4 | 72.6 | 72.8 | 72.9 | 73.1 | 73.3 | 4.3 |
| Tseng | 13.8 | 13.9 | 14.0 | 14.0 | 14.1 | 14.1 | 14.2 | 14.2 | 14.3 | 14.3 | 14.4 | 14.4 | 14.5 | 14.5 | 14.6 | 14.6 | 14.7 | 6.0 |
| Warping | 15.1 | 15.2 | 15.3 | 15.4 | 15.4 | 15.5 | 15.6 | 15.6 | 15.7 | 15.8 | 15.9 | 16.0 | 16.1 | 16.1 | 16.2 | 16.2 | 16.3 | 7.7 |
| **Geometric Avg** | 33.1 | 33.2 | 33.3 | 33.5 | 33.6 | 33.8 | 33.9 | 34.0 | 34.2 | 34.3 | 34.4 | 34.6 | 34.7 | 34.8 | 34.9 | 35.1 | 35.2 | 6.4 |

*Table A.20 – Area vs # of NN Interconnects for Cross Radius 1 & 2 (Measured Under Constant Track Count)*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 19.9 | 19.8 | 19.8 | 19.8 | 19.7 | 19.7 | 20.3 | 20.2 | 20.0 | 20.3 | 20.2 | 20.5 | 20.2 | 20.3 | 20.3 | 20.6 | 20.5 | 3.0 |
| Apex2 | 29.1 | 28.5 | 28.9 | 28.7 | 28.5 | 29.0 | 28.8 | 28.9 | 29.4 | 29.2 | 29.3 | 29.2 | 29.2 | 29.5 | 29.2 | 29.3 | 29.3 | 1.0 |
| Apex4 | 20.0 | 19.9 | 19.7 | 19.7 | 19.6 | 19.9 | 19.8 | 19.9 | 19.9 | 20.0 | 20.0 | 20.0 | 20.0 | 20.0 | 20.0 | 20.1 | 20.4 | 2.2 |
| Bigkey | 23.8 | 24.0 | 23.8 | 24.2 | 24.4 | 24.0 | 23.9 | 24.1 | 24.2 | 24.2 | 24.4 | 24.8 | 24.7 | 25.2 | 25.1 | 25.1 | 25.2 | 5.7 |
| Clma | 133.4 | 135.2 | 135.0 | 136.5 | 135.5 | 134.3 | 136.3 | 134.4 | 137.0 | 135.7 | 135.8 | 136.1 | 137.8 | 137.7 | 137.1 | 139.6 | 139.9 | 4.8 |
| Des | 31.5 | 31.8 | 31.7 | 31.1 | 30.8 | 31.6 | 31.8 | 31.6 | 31.9 | 31.8 | 31.4 | 32.0 | 31.9 | 32.4 | 32.0 | 32.4 | 33.0 | 4.7 |
| Diffeq | 17.7 | 17.8 | 17.8 | 17.6 | 17.6 | 17.6 | 17.7 | 17.8 | 17.6 | 17.9 | 18.3 | 18.3 | 18.1 | 18.2 | 18.1 | 18.3 | 18.4 | 3.9 |
| Display_chip | 18.7 | 18.7 | 18.9 | 18.7 | 18.7 | 18.7 | 18.5 | 18.8 | 18.7 | 19.0 | 18.9 | 19.0 | 19.1 | 19.2 | 19.2 | 19.3 | 19.4 | 3.6 |
| Dsip | 23.2 | 23.4 | 23.2 | 23.7 | 23.3 | 23.3 | 23.9 | 23.9 | 23.9 | 24.0 | 24.2 | 24.3 | 24.1 | 24.7 | 24.6 | 24.9 | 24.8 | 6.7 |
| Elliptic | 52.2 | 52.1 | 52.0 | 52.8 | 52.5 | 52.2 | 52.4 | 52.6 | 52.8 | 54.0 | 53.2 | 53.7 | 54.4 | 53.9 | 53.3 | 55.1 | 54.2 | 3.8 |
| Ex1010 | 67.8 | 67.3 | 67.9 | 67.8 | 67.6 | 68.4 | 67.3 | 67.8 | 68.6 | 68.5 | 68.5 | 69.0 | 68.7 | 68.7 | 68.4 | 70.0 | 69.9 | 3.1 |
| Ex5p | 16.6 | 16.8 | 16.7 | 16.7 | 16.9 | 16.8 | 16.6 | 16.8 | 16.8 | 16.7 | 16.7 | 16.8 | 16.7 | 16.8 | 16.9 | 16.7 | 17.1 | 3.1 |
| Frisc | 53.1 | 53.1 | 52.5 | 53.7 | 53.3 | 53.3 | 53.8 | 53.4 | 53.4 | 54.6 | 55.3 | 54.5 | 54.9 | 55.0 | 55.2 | 55.2 | 55.8 | 5.0 |
| Img_calc | 135.1 | 135.7 | 134.4 | 134.5 | 133.7 | 133.8 | 134.3 | 134.3 | 134.0 | 137.0 | 136.0 | 136.9 | 136.8 | 136.3 | 138.5 | 138.6 | 138.5 | 2.5 |
| Img_interp | 29.4 | 30.1 | 29.5 | 29.6 | 29.1 | 29.4 | 29.4 | 29.5 | 29.5 | 30.1 | 29.6 | 29.9 | 29.8 | 29.8 | 30.0 | 30.0 | 29.9 | 1.7 |
| Input_chip | 8.2 | 8.3 | 8.3 | 8.3 | 8.2 | 8.3 | 8.2 | 8.2 | 8.3 | 8.3 | 8.3 | 8.2 | 8.4 | 8.4 | 8.4 | 8.4 | 8.4 | 2.6 |
| Misex3 | 20.3 | 20.2 | 20.1 | 20.1 | 20.2 | 20.2 | 20.8 | 20.4 | 20.4 | 20.4 | 20.5 | 20.4 | 20.4 | 20.9 | 20.6 | 20.6 | 20.6 | 1.4 |
| Pdc | 85.2 | 83.5 | 84.3 | 84.8 | 85.3 | 85.4 | 84.9 | 84.3 | 86.7 | 87.4 | 87.9 | 86.5 | 87.0 | 87.3 | 87.9 | 88.1 | 88.0 | 3.3 |
| Peak_chip | 7.7 | 8.1 | 8.0 | 7.9 | 8.0 | 7.8 | 7.9 | 7.9 | 8.0 | 8.1 | 8.0 | 8.0 | 8.0 | 8.0 | 8.1 | 8.1 | 8.1 | 4.5 |
| S298 | 22.1 | 22.0 | 21.8 | 21.7 | 22.0 | 21.7 | 21.7 | 22.2 | 22.2 | 22.3 | 22.4 | 22.0 | 22.1 | 22.2 | 22.6 | 22.9 | 22.7 | 2.8 |
| S38417 | 83.3 | 83.0 | 83.0 | 83.0 | 82.8 | 83.1 | 83.9 | 83.6 | 83.9 | 84.5 | 84.0 | 84.6 | 85.2 | 85.0 | 84.7 | 85.9 | 85.4 | 2.5 |
| S38584.1 | 80.7 | 80.4 | 81.0 | 80.1 | 80.8 | 81.5 | 80.8 | 80.7 | 82.2 | 82.2 | 81.8 | 82.7 | 82.8 | 83.2 | 83.8 | 83.1 | 84.1 | 4.2 |
| Scale125_chip | 26.6 | 27.0 | 26.7 | 26.8 | 26.8 | 26.6 | 26.6 | 26.9 | 26.6 | 27.1 | 27.0 | 27.2 | 27.0 | 27.3 | 27.7 | 27.9 | 27.6 | 3.7 |
| Scale2_chip | 11.7 | 11.8 | 11.7 | 11.7 | 11.7 | 11.7 | 11.6 | 11.7 | 11.6 | 11.8 | 11.7 | 11.9 | 11.9 | 11.8 | 11.8 | 11.9 | 12.0 | 2.5 |
| Seq | 25.8 | 25.5 | 25.9 | 26.1 | 26.2 | 26.0 | 26.1 | 25.9 | 26.3 | 26.6 | 26.7 | 26.5 | 26.6 | 26.5 | 26.6 | 26.6 | 26.7 | 3.5 |
| Spla | 61.4 | 61.1 | 61.6 | 61.8 | 60.7 | 62.1 | 61.2 | 61.2 | 62.3 | 62.3 | 62.4 | 62.6 | 63.0 | 63.2 | 63.5 | 62.5 | 63.6 | 3.6 |
| Tseng | 12.2 | 12.3 | 12.2 | 12.1 | 12.3 | 12.1 | 12.4 | 12.5 | 12.5 | 12.7 | 12.5 | 12.5 | 12.8 | 12.7 | 12.7 | 12.8 | 12.8 | 4.8 |
| Warping | 13.7 | 13.9 | 13.7 | 13.6 | 13.7 | 13.7 | 13.8 | 13.8 | 13.8 | 14.1 | 14.0 | 14.0 | 14.1 | 14.1 | 14.1 | 14.3 | 14.2 | 4.0 |
| **Geometric Avg** | 29.5 | 29.6 | 29.6 | 29.6 | 29.5 | 29.6 | 29.7 | 29.7 | 29.8 | 30.1 | 30.1 | 30.1 | 30.2 | 30.3 | 30.3 | 30.5 | 30.6 | 3.5 |

*Table A.21 – Area vs # of NN Interconnects for Cross Radius 1 & 2 (Measured Under Varying Track Count)*

| Circuit | Wmin For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Wmin (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 30 | 29 | 29 | 29 | 29 | 28 | 30 | 29 | 29 | 29 | 29 | 29 | 28 | 28 | 28 | 29 | 28 | -5.3 |
| Apex2 | 36 | 35 | 36 | 35 | 35 | 35 | 35 | 35 | 36 | 35 | 35 | 35 | 34 | 35 | 34 | 34 | 34 | -6.1 |
| Apex4 | 36 | 35 | 35 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 33 | 33 | 33 | 34 | -5.6 |
| Bigkey | 20 | 20 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | -6.0 |
| Clma | 44 | 45 | 44 | 45 | 44 | 43 | 44 | 43 | 44 | 43 | 43 | 43 | 44 | 43 | 43 | 44 | 44 | -0.5 |
| Des | 21 | 21 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | -7.6 |
| Diffeq | 25 | 25 | 25 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 25 | 24 | 24 | 24 | 23 | 24 | 24 | -4.8 |
| Display_chip | 20 | 20 | 20 | 20 | 19 | 19 | 18 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | -7.0 |
| Dsip | 21 | 21 | 20 | 21 | 20 | 20 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | -4.8 |
| Elliptic | 37 | 36 | 36 | 37 | 36 | 36 | 36 | 36 | 36 | 37 | 36 | 36 | 36 | 36 | 35 | 37 | 36 | -3.8 |
| Ex1010 | 37 | 37 | 37 | 37 | 36 | 37 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 35 | 36 | 36 | -2.7 |
| Ex5p | 36 | 37 | 37 | 36 | 37 | 36 | 35 | 36 | 36 | 35 | 35 | 35 | 35 | 35 | 35 | 34 | 35 | -1.7 |
| Frisc | 41 | 40 | 40 | 41 | 40 | 40 | 40 | 40 | 39 | 40 | 41 | 40 | 40 | 40 | 40 | 40 | 40 | -1.5 |
| Img_calc | 35 | 35 | 34 | 34 | 33 | 33 | 33 | 33 | 33 | 34 | 33 | 33 | 33 | 33 | 33 | 33 | 33 | -6.3 |
| Img_interp | 22 | 23 | 22 | 22 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 20 | 20 | 20 | 20 | -9.1 |
| Input_chip | 17 | 17 | 17 | 17 | 17 | 17 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | -8.2 |
| Misex3 | 32 | 31 | 31 | 31 | 31 | 30 | 32 | 31 | 30 | 30 | 30 | 30 | 30 | 31 | 30 | 30 | 30 | -7.5 |
| Pdc | 53 | 51 | 51 | 52 | 52 | 52 | 51 | 50 | 52 | 52 | 52 | 51 | 51 | 51 | 51 | 51 | 51 | -3.4 |
| Peak_chip | 15 | 17 | 16 | 15 | 16 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 14 | 14 | 14 | 14 | -5.3 |
| S298 | 24 | 23 | 23 | 22 | 23 | 22 | 22 | 22 | 22 | 22 | 22 | 21 | 21 | 21 | 22 | 22 | 21 | -11.7 |
| S38417 | 32 | 32 | 32 | 31 | 31 | 31 | 31 | 31 | 31 | 31 | 30 | 31 | 31 | 30 | 30 | 31 | 30 | -6.3 |
| S38584.1 | 30 | 30 | 30 | 29 | 30 | 30 | 29 | 29 | 30 | 29 | 29 | 29 | 29 | 29 | 29 | 29 | 29 | -2.7 |
| Scale125_chip | 21 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | 20 | 19 | 19 | 19 | 19 | 20 | 20 | 19 | -9.5 |
| Scale2_chip | 17 | 17 | 17 | 17 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 15 | 15 | 15 | 15 | -9.4 |
| Seq | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 33 | 34 | 34 | 34 | 34 | 34 | 33 | 33 | 33 | 33 | -2.4 |
| Spla | 46 | 45 | 46 | 46 | 44 | 45 | 44 | 44 | 45 | 45 | 45 | 45 | 45 | 45 | 45 | 44 | 45 | -2.6 |
| Tseng | 23 | 23 | 23 | 22 | 23 | 22 | 23 | 23 | 22 | 23 | 22 | 22 | 23 | 22 | 22 | 22 | 22 | -4.3 |
| Warping | 19 | 19 | 19 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 17 | 18 | 17 | -8.4 |
| **Geometric Avg** | 27.9 | 27.9 | 27.6 | 27.4 | 27.1 | 26.9 | 26.8 | 26.7 | 26.7 | 26.9 | 26.7 | 26.6 | 26.5 | 26.5 | 26.3 | 26.4 | 26.3 | -5.6 |

*Table A.22 – $W_{min}$ vs # of NN Interconnects for Cross Radius 1 & 2*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 15.7 | 15.2 | 15.3 | 15.4 | 15.2 | 15.5 | 15.3 | 15.3 | 15.0 | 15.0 | 14.6 | 14.9 | 14.8 | 14.9 | 14.8 | 15.0 | 14.9 | -5.1 |
| Apex2 | 17.0 | 17.1 | 16.9 | 17.1 | 16.8 | 17.1 | 16.7 | 16.9 | 16.6 | 16.8 | 17.1 | 17.0 | 16.7 | 16.4 | 16.6 | 16.8 | 16.8 | -1.1 |
| Apex4 | 15.8 | 15.3 | 15.4 | 15.3 | 15.8 | 15.1 | 15.2 | 15.9 | 15.2 | 15.3 | 15.4 | 15.6 | 14.7 | 15.4 | 15.3 | 15.1 | 15.4 | -2.5 |
| Bigkey | 8.8 | 8.7 | 8.5 | 8.7 | 8.7 | 8.8 | 8.7 | 8.3 | 8.4 | 7.9 | 8.4 | 8.3 | 8.3 | 8.5 | 8.4 | 8.4 | 8.4 | -5.0 |
| Clma | 34.2 | 34.9 | 33.7 | 33.7 | 36.6 | 34.2 | 34.3 | 32.4 | 33.9 | 33.6 | 32.9 | 32.0 | 33.1 | 33.7 | 33.1 | 33.2 | 32.6 | -4.9 |
| Des | 15.6 | 15.3 | 15.8 | 15.1 | 15.1 | 15.4 | 15.1 | 14.9 | 14.9 | 15.2 | 14.9 | 14.6 | 15.2 | 14.8 | 15.3 | 14.9 | 14.8 | -5.1 |
| Diffeq | 18.2 | 17.5 | 17.1 | 16.8 | 16.9 | 16.6 | 16.2 | 16.4 | 16.0 | 16.0 | 15.7 | 15.7 | 15.2 | 15.3 | 15.4 | 15.4 | 15.1 | -16.6 |
| Display_chip | 16.6 | 16.7 | 16.4 | 16.3 | 16.2 | 16.0 | 15.6 | 15.6 | 15.7 | 15.2 | 15.2 | 15.2 | 15.2 | 15.0 | 15.3 | 14.7 | 15.0 | -10.1 |
| Dsip | 8.0 | 8.1 | 8.1 | 8.3 | 8.2 | 8.2 | 8.4 | 8.1 | 8.2 | 8.2 | 8.2 | 8.4 | 8.2 | 8.4 | 8.6 | 7.8 | 8.0 | -1.1 |
| Elliptic | 24.6 | 25.8 | 24.9 | 24.7 | 24.4 | 25.1 | 25.0 | 23.8 | 24.1 | 23.6 | 23.2 | 23.4 | 23.9 | 24.4 | 23.8 | 24.3 | 23.5 | -4.6 |
| Ex1010 | 26.3 | 26.0 | 24.6 | 25.0 | 24.0 | 25.5 | 23.9 | 24.6 | 24.9 | 24.4 | 24.5 | 25.4 | 24.4 | 25.0 | 24.7 | 24.9 | 24.1 | -8.7 |
| Ex5p | 14.9 | 15.6 | 15.1 | 15.0 | 15.9 | 15.2 | 15.1 | 14.9 | 15.4 | 15.3 | 15.9 | 15.1 | 15.2 | 15.2 | 15.5 | 15.8 | 15.6 | 4.3 |
| Frisc | 30.4 | 30.2 | 30.3 | 29.4 | 29.1 | 29.0 | 29.5 | 29.3 | 29.1 | 28.4 | 28.4 | 27.7 | 28.2 | 27.7 | 27.8 | 27.3 | 27.5 | -9.4 |
| Img_calc | 39.5 | 38.3 | 38.2 | 37.4 | 36.8 | 35.9 | 35.6 | 35.3 | 35.2 | 35.3 | 35.1 | 35.0 | 34.9 | 35.1 | 35.0 | 35.2 | 35.0 | -11.5 |
| Img_interp | 22.4 | 21.3 | 20.6 | 20.5 | 20.7 | 20.5 | 20.3 | 20.1 | 20.7 | 20.5 | 20.6 | 20.7 | 20.4 | 20.3 | 19.9 | 20.6 | 20.3 | -9.5 |
| Input_chip | 15.4 | 15.5 | 14.7 | 14.8 | 14.7 | 14.3 | 14.0 | 14.1 | 14.0 | 13.7 | 13.7 | 13.5 | 13.6 | 13.6 | 13.3 | 13.4 | 13.4 | -12.8 |
| Misex3 | 15.3 | 15.0 | 15.1 | 14.2 | 14.7 | 14.7 | 14.5 | 14.7 | 14.6 | 14.5 | 14.7 | 14.5 | 14.5 | 14.3 | 14.7 | 14.2 | 14.7 | -4.3 |
| Pdc | 27.1 | 27.0 | 27.0 | 27.1 | 26.4 | 24.4 | 27.5 | 25.3 | 26.4 | 24.7 | 25.9 | 27.8 | 26.5 | 25.8 | 26.2 | 27.7 | 25.5 | -5.9 |
| Peak_chip | 18.1 | 17.9 | 17.2 | 17.4 | 16.6 | 16.3 | 16.5 | 16.9 | 16.8 | 16.6 | 16.2 | 16.2 | 16.2 | 16.2 | 16.0 | 16.2 | 16.1 | -11.0 |
| S298 | 32.0 | 32.5 | 29.4 | 31.0 | 29.6 | 29.4 | 30.4 | 30.7 | 30.1 | 29.3 | 30.6 | 30.4 | 30.1 | 30.3 | 31.7 | 29.2 | 30.9 | -3.4 |
| S38417 | 20.2 | 20.5 | 19.3 | 19.8 | 19.3 | 19.0 | 19.1 | 19.0 | 19.0 | 19.6 | 18.9 | 18.7 | 19.4 | 19.4 | 18.9 | 18.6 | 18.4 | -8.9 |
| S38584.1 | 15.2 | 15.4 | 15.0 | 15.1 | 14.9 | 14.6 | 15.3 | 14.8 | 14.9 | 14.4 | 14.3 | 14.7 | 14.8 | 14.5 | 14.9 | 14.5 | 14.6 | -3.7 |
| Scale125_chip | 24.3 | 23.4 | 22.7 | 22.4 | 22.3 | 22.4 | 22.0 | 22.1 | 22.0 | 21.4 | 20.7 | 20.7 | 21.0 | 20.6 | 20.7 | 20.5 | 20.3 | -16.8 |
| Scale2_chip | 18.8 | 18.6 | 17.8 | 17.8 | 17.5 | 17.1 | 17.3 | 17.0 | 17.3 | 16.8 | 16.6 | 16.8 | 16.7 | 16.6 | 16.5 | 16.5 | 16.5 | -12.4 |
| Seq | 15.8 | 15.1 | 15.6 | 15.8 | 15.8 | 15.5 | 15.4 | 15.5 | 14.7 | 15.2 | 15.7 | 15.4 | 16.0 | 15.1 | 15.3 | 15.0 | 14.6 | -7.7 |
| Spla | 22.9 | 23.0 | 23.4 | 22.6 | 23.7 | 21.8 | 22.5 | 22.1 | 20.8 | 22.0 | 22.5 | 23.3 | 22.9 | 21.2 | 22.9 | 22.2 | 20.8 | -9.0 |
| Tseng | 18.2 | 17.5 | 16.9 | 16.5 | 16.0 | 15.7 | 16.0 | 15.7 | 15.6 | 16.0 | 15.9 | 15.6 | 15.4 | 15.7 | 15.3 | 15.4 | 15.6 | -14.4 |
| Warping | 11.7 | 11.4 | 11.2 | 11.1 | 11.0 | 10.6 | 10.9 | 10.9 | 10.8 | 10.8 | 10.7 | 10.9 | 10.6 | 10.6 | 10.7 | 10.7 | 10.6 | -10.1 |
| **Geometric Avg** | 18.8 | 18.7 | 18.3 | 18.2 | 18.2 | 17.9 | 18.0 | 17.8 | 17.8 | 17.6 | 17.7 | 17.7 | 17.6 | 17.6 | 17.7 | 17.5 | 17.4 | -7.7 |

*Table A.23 – Delay vs # of NN Interconnects for Full Radius 1*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 22.4 | 22.5 | 22.6 | 22.7 | 22.7 | 22.8 | 22.9 | 23.0 | 23.1 | 23.1 | 23.2 | 23.3 | 23.4 | 23.5 | 23.5 | 23.6 | 23.7 | 5.7 |
| Apex2 | 32.9 | 33.0 | 33.2 | 33.3 | 33.4 | 33.5 | 33.6 | 33.7 | 33.8 | 33.9 | 34.0 | 34.1 | 34.2 | 34.3 | 34.4 | 34.5 | 34.7 | 5.2 |
| Apex4 | 22.6 | 22.7 | 22.7 | 22.8 | 22.9 | 22.9 | 23.0 | 23.1 | 23.2 | 23.2 | 23.3 | 23.4 | 23.4 | 23.5 | 23.6 | 23.7 | 23.7 | 5.1 |
| Bigkey | 26.6 | 26.7 | 26.9 | 27.0 | 27.2 | 27.3 | 27.5 | 27.6 | 27.8 | 28.0 | 28.1 | 28.3 | 28.5 | 28.7 | 28.9 | 29.1 | 29.3 | 10.2 |
| Clma | 152.1 | 152.8 | 153.6 | 154.3 | 155.0 | 155.6 | 156.2 | 156.6 | 157.1 | 157.6 | 158.0 | 158.5 | 159.0 | 159.4 | 159.9 | 160.4 | 160.8 | 5.7 |
| Des | 35.3 | 35.5 | 35.7 | 35.9 | 36.1 | 36.4 | 36.7 | 37.0 | 37.3 | 37.6 | 37.9 | 38.1 | 38.4 | 38.6 | 38.8 | 39.0 | 39.2 | 11.2 |
| Diffeq | 19.9 | 20.0 | 20.1 | 20.1 | 20.2 | 20.3 | 20.4 | 20.5 | 20.5 | 20.6 | 20.7 | 20.8 | 20.9 | 20.9 | 21.0 | 21.1 | 21.2 | 6.4 |
| Display_chip | 20.5 | 20.5 | 20.6 | 20.7 | 20.8 | 20.9 | 21.0 | 21.1 | 21.2 | 21.4 | 21.5 | 21.6 | 21.7 | 21.9 | 22.0 | 22.1 | 22.2 | 8.7 |
| Dsip | 26.2 | 26.3 | 26.5 | 26.6 | 26.8 | 26.9 | 27.1 | 27.4 | 27.6 | 27.8 | 28.0 | 28.2 | 28.3 | 28.5 | 28.6 | 28.8 | 28.9 | 10.7 |
| Elliptic | 58.9 | 59.1 | 59.3 | 59.5 | 59.7 | 59.9 | 60.1 | 60.3 | 60.5 | 60.7 | 60.8 | 61.0 | 61.2 | 61.4 | 61.6 | 61.8 | 62.0 | 5.4 |
| Ex1010 | 76.6 | 76.8 | 77.1 | 77.4 | 77.6 | 77.9 | 78.1 | 78.4 | 78.6 | 78.9 | 79.1 | 79.4 | 79.6 | 79.9 | 80.1 | 80.4 | 80.6 | 5.3 |
| Ex5p | 18.5 | 18.5 | 18.6 | 18.7 | 18.7 | 18.8 | 18.8 | 18.9 | 18.9 | 19.0 | 19.1 | 19.1 | 19.2 | 19.2 | 19.3 | 19.3 | 19.4 | 4.9 |
| Frisc | 60.4 | 60.5 | 60.7 | 60.9 | 61.1 | 61.3 | 61.5 | 61.6 | 61.8 | 62.0 | 62.2 | 62.4 | 62.6 | 62.8 | 63.0 | 63.3 | 63.5 | 5.2 |
| Img_calc | 152.4 | 153.0 | 153.5 | 154.1 | 154.6 | 155.2 | 155.7 | 156.3 | 156.8 | 157.3 | 157.9 | 158.4 | 159.0 | 159.5 | 160.1 | 160.6 | 161.2 | 5.7 |
| Img_interp | 32.5 | 32.7 | 33.0 | 33.2 | 33.4 | 33.6 | 33.8 | 34.0 | 34.1 | 34.3 | 34.4 | 34.6 | 34.7 | 34.9 | 35.0 | 35.2 | 35.3 | 8.6 |
| Input_chip | 8.8 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 9.2 | 9.2 | 9.3 | 9.3 | 9.3 | 9.4 | 9.4 | 9.5 | 9.5 | 8.0 |
| Misex3 | 22.9 | 23.0 | 23.0 | 23.1 | 23.2 | 23.3 | 23.4 | 23.4 | 23.5 | 23.6 | 23.7 | 23.8 | 23.8 | 23.9 | 24.0 | 24.1 | 24.2 | 5.6 |
| Pdc | 97.8 | 98.1 | 98.3 | 98.6 | 98.9 | 99.1 | 99.4 | 99.6 | 99.9 | 100.1 | 100.4 | 100.6 | 100.9 | 101.1 | 101.4 | 101.6 | 101.9 | 4.1 |
| Peak_chip | 8.4 | 8.5 | 8.5 | 8.6 | 8.6 | 8.6 | 8.7 | 8.7 | 8.8 | 8.8 | 8.9 | 8.9 | 9.0 | 9.0 | 9.0 | 9.1 | 9.1 | 8.3 |
| S298 | 25.2 | 25.3 | 25.4 | 25.5 | 25.7 | 25.8 | 25.9 | 26.0 | 26.1 | 26.2 | 26.3 | 26.4 | 26.5 | 26.6 | 26.7 | 26.8 | 26.9 | 6.8 |
| S38417 | 93.7 | 94.1 | 94.4 | 94.8 | 95.1 | 95.5 | 95.8 | 96.2 | 96.5 | 96.9 | 97.2 | 97.6 | 97.9 | 98.3 | 98.6 | 99.0 | 99.3 | 6.0 |
| S38584.1 | 89.4 | 89.8 | 90.1 | 90.5 | 90.8 | 91.2 | 91.5 | 91.9 | 92.2 | 92.6 | 92.9 | 93.3 | 93.6 | 94.0 | 94.3 | 94.7 | 95.0 | 6.3 |
| Scale125_chip | 29.5 | 29.6 | 29.7 | 29.9 | 30.0 | 30.2 | 30.4 | 30.6 | 30.8 | 31.0 | 31.1 | 31.3 | 31.5 | 31.6 | 31.8 | 31.9 | 32.0 | 8.8 |
| Scale2_chip | 12.6 | 12.6 | 12.7 | 12.8 | 12.8 | 12.9 | 13.0 | 13.0 | 13.1 | 13.2 | 13.2 | 13.3 | 13.4 | 13.4 | 13.5 | 13.5 | 13.6 | 8.2 |
| Seq | 29.0 | 29.1 | 29.2 | 29.3 | 29.4 | 29.5 | 29.6 | 29.7 | 29.8 | 29.9 | 30.0 | 30.1 | 30.2 | 30.3 | 30.4 | 30.5 | 30.6 | 5.4 |
| Spla | 70.3 | 70.5 | 70.7 | 70.9 | 71.1 | 71.3 | 71.5 | 71.7 | 71.9 | 72.1 | 72.3 | 72.5 | 72.7 | 72.9 | 73.1 | 73.3 | 73.5 | 4.5 |
| Tseng | 13.8 | 13.9 | 14.0 | 14.0 | 14.1 | 14.1 | 14.2 | 14.2 | 14.3 | 14.4 | 14.4 | 14.5 | 14.5 | 14.6 | 14.6 | 14.7 | 14.8 | 6.6 |
| Warping | 15.1 | 15.2 | 15.3 | 15.4 | 15.4 | 15.5 | 15.6 | 15.6 | 15.7 | 15.8 | 15.9 | 16.0 | 16.1 | 16.2 | 16.3 | 16.4 | 16.4 | 8.6 |
| **Geometric Avg** | 33.1 | 33.2 | 33.4 | 33.5 | 33.6 | 33.8 | 33.9 | 34.1 | 34.2 | 34.3 | 34.5 | 34.6 | 34.8 | 34.9 | 35.1 | 35.2 | 35.3 | 6.8 |

*Table A.24 – Area vs # of NN Interconnects for Full Radius 1 (Measured Under Constant Track Count)*

| Circuit | Delay (ns) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Delay (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 15.7 | 15.2 | 15.3 | 15.4 | 15.2 | 15.5 | 15.3 | 15.3 | 15.0 | 15.7 | 14.8 | 15.3 | 15.0 | 15.1 | 15.3 | 15.3 | 14.6 | -6.8 |
| Apex2 | 17.0 | 17.1 | 16.9 | 17.1 | 16.8 | 17.1 | 16.7 | 16.9 | 16.6 | 16.9 | 16.6 | 17.2 | 16.7 | 16.9 | 16.8 | 17.3 | 16.9 | -0.3 |
| Apex4 | 15.8 | 15.3 | 15.4 | 15.3 | 15.8 | 15.1 | 15.2 | 15.9 | 15.2 | 15.5 | 15.3 | 15.2 | 15.4 | 15.7 | 15.3 | 15.7 | 15.4 | -2.1 |
| Bigkey | 8.8 | 8.7 | 8.5 | 8.7 | 8.7 | 8.8 | 8.7 | 8.3 | 8.4 | 8.5 | 8.6 | 8.4 | 8.1 | 8.1 | 8.0 | 8.4 | 8.3 | -6.1 |
| Clma | 34.2 | 34.9 | 33.7 | 33.7 | 36.6 | 34.2 | 34.3 | 32.4 | 33.9 | 33.3 | 33.2 | 33.8 | 32.5 | 34.9 | 34.7 | 35.0 | 33.4 | -2.4 |
| Des | 15.6 | 15.3 | 15.8 | 15.1 | 15.1 | 15.4 | 15.1 | 14.9 | 14.9 | 14.8 | 15.3 | 15.0 | 14.9 | 14.9 | 14.8 | 15.0 | 15.2 | -2.8 |
| Diffeq | 18.2 | 17.5 | 17.1 | 16.8 | 16.9 | 16.6 | 16.2 | 16.4 | 16.0 | 16.0 | 15.7 | 15.8 | 15.8 | 15.7 | 15.5 | 15.4 | 15.5 | -14.5 |
| Display_chip | 16.6 | 16.7 | 16.4 | 16.3 | 16.2 | 16.0 | 15.6 | 15.6 | 15.7 | 15.7 | 16.0 | 15.1 | 15.1 | 15.3 | 15.2 | 15.1 | 15.2 | -8.9 |
| Dsip | 8.0 | 8.1 | 8.1 | 8.3 | 8.2 | 8.2 | 8.4 | 8.1 | 8.2 | 7.7 | 7.9 | 8.0 | 8.1 | 7.9 | 7.9 | 8.0 | 7.9 | -2.3 |
| Elliptic | 24.6 | 25.8 | 24.9 | 24.7 | 24.4 | 25.1 | 25.0 | 23.8 | 24.1 | 24.8 | 24.2 | 24.5 | 25.1 | 24.4 | 24.7 | 24.3 | 24.4 | -0.7 |
| Ex1010 | 26.3 | 26.0 | 24.6 | 25.0 | 24.0 | 25.5 | 23.9 | 24.6 | 24.9 | 25.3 | 24.3 | 24.3 | 25.2 | 24.2 | 24.0 | 24.6 | 24.4 | -7.4 |
| Ex5p | 14.9 | 15.6 | 15.1 | 15.0 | 15.9 | 15.2 | 15.1 | 14.9 | 15.4 | 15.2 | 15.6 | 15.3 | 15.3 | 15.4 | 14.9 | 14.5 | 15.3 | 2.7 |
| Frisc | 30.4 | 30.2 | 30.3 | 29.4 | 29.1 | 29.0 | 29.5 | 29.3 | 29.1 | 28.7 | 28.5 | 28.7 | 27.7 | 27.9 | 28.5 | 28.3 | 27.8 | -8.5 |
| Img_calc | 39.5 | 38.3 | 38.2 | 37.4 | 36.8 | 35.9 | 35.6 | 35.3 | 35.2 | 36.3 | 36.0 | 35.6 | 35.4 | 35.1 | 35.2 | 34.7 | 34.8 | -12.0 |
| Img_interp | 22.4 | 21.3 | 20.6 | 20.5 | 20.7 | 20.5 | 20.3 | 20.1 | 20.7 | 20.8 | 20.2 | 20.3 | 20.8 | 20.4 | 20.6 | 20.6 | 20.6 | -8.3 |
| Input_chip | 15.4 | 15.5 | 14.7 | 14.8 | 14.7 | 14.3 | 14.0 | 14.1 | 14.0 | 13.9 | 13.8 | 13.7 | 13.8 | 13.6 | 13.6 | 13.7 | 13.6 | -11.3 |
| Misex3 | 15.3 | 15.0 | 15.1 | 14.2 | 14.7 | 14.7 | 14.5 | 14.7 | 14.6 | 14.7 | 14.9 | 14.8 | 14.3 | 14.4 | 14.3 | 14.6 | 14.7 | -3.8 |
| Pdc | 27.1 | 27.0 | 27.0 | 27.1 | 26.4 | 24.4 | 27.5 | 25.3 | 26.4 | 25.4 | 26.0 | 23.8 | 26.5 | 25.0 | 26.1 | 25.2 | 26.3 | -3.0 |
| Peak_chip | 18.1 | 17.9 | 17.2 | 17.4 | 16.6 | 16.3 | 16.5 | 16.9 | 16.8 | 16.8 | 16.5 | 16.2 | 16.2 | 16.1 | 16.5 | 16.3 | 16.3 | -9.7 |
| S298 | 32.0 | 32.5 | 29.4 | 31.0 | 29.6 | 29.4 | 30.4 | 30.7 | 30.1 | 30.8 | 29.9 | 30.2 | 28.7 | 29.7 | 28.8 | 29.6 | 28.8 | -10.1 |
| S38417 | 20.2 | 20.5 | 19.3 | 19.8 | 19.3 | 19.0 | 19.1 | 19.0 | 19.0 | 19.8 | 19.6 | 19.0 | 19.6 | 19.2 | 18.9 | 19.2 | 19.1 | -5.1 |
| S38584.1 | 15.2 | 15.4 | 15.0 | 15.1 | 14.9 | 14.6 | 15.3 | 14.8 | 14.9 | 14.7 | 14.9 | 14.8 | 14.5 | 14.8 | 14.6 | 14.5 | 14.8 | -2.3 |
| Scale125_chip | 24.3 | 23.4 | 22.7 | 22.4 | 22.3 | 22.4 | 22.0 | 22.1 | 22.0 | 20.9 | 21.1 | 21.1 | 20.9 | 21.0 | 21.0 | 20.7 | 20.4 | -16.4 |
| Scale2_chip | 18.8 | 18.6 | 17.8 | 17.8 | 17.5 | 17.1 | 17.3 | 17.0 | 17.3 | 17.1 | 16.6 | 16.5 | 16.9 | 16.2 | 16.6 | 16.3 | 16.1 | -14.4 |
| Seq | 15.8 | 15.1 | 15.6 | 15.8 | 15.8 | 15.5 | 15.4 | 15.5 | 14.7 | 14.8 | 15.4 | 15.1 | 15.3 | 15.2 | 14.8 | 15.3 | 15.1 | -4.6 |
| Spla | 22.9 | 23.0 | 23.4 | 22.6 | 23.7 | 21.8 | 22.5 | 22.1 | 20.8 | 22.2 | 21.6 | 21.8 | 21.7 | 21.4 | 23.0 | 21.9 | 21.2 | -7.5 |
| Tseng | 18.2 | 17.5 | 16.9 | 16.5 | 16.0 | 15.7 | 16.0 | 15.7 | 15.6 | 15.6 | 15.9 | 15.2 | 15.6 | 15.4 | 15.0 | 15.1 | 15.3 | -15.7 |
| Warping | 11.7 | 11.4 | 11.2 | 11.1 | 11.0 | 10.6 | 10.9 | 10.9 | 10.8 | 10.4 | 10.2 | 10.2 | 10.3 | 9.9 | 10.3 | 10.2 | 10.1 | -14.0 |
| **Geometric Avg** | 18.8 | 18.7 | 18.3 | 18.2 | 18.2 | 17.9 | 18.0 | 17.8 | 17.8 | 17.8 | 17.7 | 17.6 | 17.6 | 17.5 | 17.5 | 17.6 | 17.5 | -7.2 |

*Table A.25 – Delay vs # of NN Interconnects for Full Radius 1 Using Nearest-Side Input Pin Connection Strategy*

| Circuit | Area (x10E+05 Minimum Width Transistors) For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Area (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 19.9 | 19.8 | 19.8 | 19.8 | 19.7 | 19.7 | 20.3 | 20.2 | 20.0 | 20.0 | 20.1 | 20.4 | 20.2 | 20.6 | 20.0 | 20.5 | 20.5 | 3.0 |
| Apex2 | 29.1 | 28.5 | 28.9 | 28.7 | 28.5 | 29.0 | 28.8 | 28.9 | 29.4 | 28.8 | 29.2 | 29.0 | 29.1 | 29.5 | 29.8 | 29.4 | 29.9 | 2.9 |
| Apex4 | 20.0 | 19.9 | 19.7 | 19.7 | 19.6 | 19.9 | 19.8 | 19.9 | 19.9 | 19.9 | 20.1 | 20.0 | 20.1 | 20.2 | 20.2 | 20.3 | 20.4 | 2.0 |
| Bigkey | 23.8 | 24.0 | 23.8 | 24.2 | 24.4 | 24.0 | 23.9 | 24.1 | 24.2 | 24.8 | 24.6 | 24.9 | 25.3 | 25.0 | 25.2 | 25.5 | 25.5 | 7.3 |
| Clma | 133.4 | 135.2 | 135.0 | 136.5 | 135.5 | 134.3 | 136.3 | 134.4 | 137.0 | 135.9 | 136.9 | 136.7 | 138.1 | 138.6 | 139.0 | 138.2 | 138.3 | 3.6 |
| Des | 31.5 | 31.8 | 31.7 | 31.1 | 30.8 | 31.6 | 31.8 | 31.6 | 31.9 | 31.2 | 31.9 | 31.7 | 32.8 | 32.1 | 32.4 | 32.9 | 32.2 | 2.1 |
| Diffeq | 17.7 | 17.8 | 17.8 | 17.6 | 17.6 | 17.6 | 17.7 | 17.8 | 17.6 | 17.6 | 17.8 | 17.9 | 17.8 | 18.0 | 18.0 | 18.1 | 18.2 | 2.8 |
| Display_chip | 18.7 | 18.7 | 18.9 | 18.7 | 18.7 | 18.7 | 18.5 | 18.8 | 18.7 | 18.6 | 18.8 | 18.7 | 19.0 | 19.0 | 19.2 | 19.0 | 19.3 | 3.3 |
| Dsip | 23.2 | 23.4 | 23.2 | 23.7 | 23.3 | 23.3 | 23.9 | 23.9 | 23.9 | 24.1 | 24.0 | 24.3 | 24.5 | 24.3 | 24.8 | 24.4 | 24.9 | 7.1 |
| Elliptic | 52.2 | 52.1 | 52.0 | 52.8 | 52.5 | 52.2 | 52.4 | 52.6 | 52.8 | 53.4 | 52.2 | 52.7 | 52.9 | 53.6 | 53.5 | 53.6 | 53.8 | 2.9 |
| Ex1010 | 67.8 | 67.3 | 67.9 | 67.8 | 67.6 | 68.4 | 67.3 | 67.8 | 68.6 | 68.6 | 68.1 | 68.8 | 68.3 | 69.9 | 69.3 | 69.9 | 69.3 | 2.3 |
| Ex5p | 16.6 | 16.8 | 16.7 | 16.7 | 16.9 | 16.8 | 16.6 | 16.8 | 16.8 | 16.9 | 16.7 | 16.8 | 16.8 | 16.9 | 16.9 | 16.9 | 17.1 | 3.1 |
| Frisc | 53.1 | 53.1 | 52.5 | 53.7 | 53.3 | 53.3 | 53.8 | 53.4 | 53.4 | 54.4 | 53.8 | 54.4 | 55.4 | 54.3 | 55.7 | 55.3 | 55.1 | 3.7 |
| Img_calc | 135.1 | 135.7 | 134.4 | 134.5 | 133.7 | 133.8 | 134.3 | 134.3 | 134.0 | 133.9 | 133.5 | 134.5 | 134.0 | 133.1 | 134.5 | 134.1 | 134.2 | -0.7 |
| Img_interp | 29.4 | 30.1 | 29.5 | 29.6 | 29.1 | 29.4 | 29.4 | 29.5 | 29.5 | 29.2 | 29.5 | 29.6 | 29.8 | 29.8 | 29.6 | 30.1 | 30.3 | 3.0 |
| Input_chip | 8.2 | 8.3 | 8.3 | 8.3 | 8.2 | 8.3 | 8.2 | 8.2 | 8.3 | 8.1 | 8.3 | 8.1 | 8.2 | 8.2 | 8.2 | 8.3 | 8.3 | 1.5 |
| Misex3 | 20.3 | 20.2 | 20.1 | 20.1 | 20.2 | 20.2 | 20.8 | 20.4 | 20.4 | 20.2 | 20.3 | 20.6 | 20.5 | 20.6 | 20.7 | 20.9 | 20.8 | 2.2 |
| Pdc | 85.2 | 83.5 | 84.3 | 84.8 | 85.3 | 85.4 | 84.9 | 84.3 | 86.7 | 84.9 | 85.8 | 86.3 | 87.7 | 87.9 | 86.7 | 88.5 | 87.0 | 2.1 |
| Peak_chip | 7.7 | 8.1 | 8.0 | 7.9 | 8.0 | 7.8 | 7.9 | 7.9 | 8.0 | 7.9 | 7.7 | 7.9 | 7.8 | 7.9 | 7.9 | 8.1 | 8.0 | 3.9 |
| S298 | 22.1 | 22.0 | 21.8 | 21.7 | 22.0 | 21.7 | 21.7 | 22.2 | 22.2 | 22.1 | 22.4 | 22.3 | 22.3 | 22.4 | 22.6 | 22.8 | 22.7 | 2.9 |
| S38417 | 83.3 | 83.0 | 83.0 | 83.0 | 82.8 | 83.1 | 83.9 | 83.6 | 83.9 | 83.8 | 83.3 | 84.4 | 84.6 | 83.9 | 83.8 | 84.6 | 84.6 | 1.5 |
| S38584.1 | 80.7 | 80.4 | 81.0 | 80.1 | 80.8 | 81.5 | 80.8 | 80.7 | 82.2 | 81.2 | 80.9 | 81.9 | 81.6 | 81.3 | 82.6 | 82.7 | 83.6 | 3.7 |
| Scale125_chip | 26.6 | 27.0 | 26.7 | 26.8 | 26.8 | 26.6 | 26.6 | 26.9 | 26.6 | 26.7 | 26.8 | 26.8 | 26.8 | 27.0 | 27.0 | 27.0 | 27.2 | 2.2 |
| Scale2_chip | 11.7 | 11.8 | 11.7 | 11.7 | 11.7 | 11.7 | 11.6 | 11.7 | 11.6 | 11.5 | 11.5 | 11.7 | 11.5 | 11.7 | 11.8 | 11.9 | 11.8 | 0.5 |
| Seq | 25.8 | 25.5 | 25.9 | 26.1 | 26.2 | 26.0 | 26.1 | 25.9 | 26.3 | 26.2 | 26.3 | 26.3 | 26.3 | 26.4 | 26.5 | 27.1 | 26.9 | 4.3 |
| Spla | 61.4 | 61.1 | 61.6 | 61.8 | 60.7 | 62.1 | 61.2 | 61.2 | 62.3 | 61.7 | 63.1 | 61.8 | 62.7 | 62.8 | 62.8 | 63.3 | 63.8 | 3.9 |
| Tseng | 12.2 | 12.3 | 12.2 | 12.1 | 12.3 | 12.1 | 12.4 | 12.5 | 12.5 | 12.4 | 12.2 | 12.4 | 12.5 | 12.4 | 12.6 | 12.6 | 12.6 | 3.3 |
| Warping | 13.7 | 13.9 | 13.7 | 13.6 | 13.7 | 13.7 | 13.8 | 13.8 | 13.8 | 13.9 | 13.8 | 13.9 | 13.9 | 13.9 | 14.2 | 14.2 | 14.1 | 2.9 |
| **Geometric Avg** | 29.5 | 29.6 | 29.6 | 29.6 | 29.5 | 29.6 | 29.7 | 29.7 | 29.8 | 29.7 | 29.8 | 29.9 | 30.0 | 30.1 | 30.2 | 30.4 | 30.4 | 3.0 |

*Table A.26 – Area vs # of NN Interconnects for Full Radius 1 (Measured Under Varying Track Count)*

| Circuit | Wmin For Various Quantities of NN Interconnects | | | | | | | | | | | | | | | | | Change In Wmin (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | |
| Alu4 | 30 | 29 | 29 | 29 | 29 | 28 | 28 | 29 | 27 | 28 | 28 | 29 | 28 | 29 | 27 | 28 | 28 | -6.0 |
| Apex2 | 36 | 35 | 36 | 36 | 35 | 36 | 35 | 35 | 35 | 34 | 35 | 34 | 34 | 35 | 35 | 34 | 35 | -3.3 |
| Apex4 | 36 | 35 | 35 | 34 | 35 | 34 | 34 | 34 | 35 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | 34 | -6.7 |
| Bigkey | 20 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 20 | 20 | 19 | 19 | 20 | 19 | 19 | 19 | 19 | -5.0 |
| Clma | 44 | 44 | 44 | 44 | 44 | 44 | 43 | 43 | 43 | 43 | 43 | 43 | 44 | 44 | 44 | 43 | 43 | -2.7 |
| Des | 21 | 21 | 20 | 20 | 20 | 20 | 19 | 20 | 20 | 19 | 20 | 19 | 20 | 19 | 19 | 19 | 18 | -12.4 |
| Diffeq | 25 | 25 | 25 | 25 | 24 | 24 | 23 | 24 | 24 | 23 | 23 | 23 | 23 | 23 | 23 | 23 | 23 | -8.0 |
| Display_chip | 20 | 20 | 19 | 20 | 19 | 19 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | 18 | -10.0 |
| Dsip | 21 | 21 | 21 | 21 | 20 | 20 | 20 | 20 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 19 | 20 | -5.7 |
| Elliptic | 37 | 36 | 36 | 36 | 36 | 35 | 36 | 36 | 35 | 36 | 34 | 35 | 35 | 35 | 35 | 35 | 35 | -5.4 |
| Ex1010 | 37 | 37 | 37 | 37 | 37 | 36 | 37 | 36 | 36 | 36 | 36 | 36 | 35 | 36 | 36 | 36 | 35 | -4.3 |
| Ex5p | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 36 | 35 | 35 | 35 | 35 | 35 | 35 | 35 | -2.2 |
| Frisc | 41 | 41 | 40 | 40 | 40 | 40 | 40 | 39 | 39 | 40 | 39 | 40 | 41 | 39 | 41 | 40 | 40 | -3.4 |
| Img_calc | 35 | 35 | 35 | 34 | 34 | 34 | 34 | 34 | 33 | 32 | 32 | 32 | 32 | 31 | 32 | 31 | 31 | -11.4 |
| Img_interp | 22 | 23 | 22 | 21 | 21 | 21 | 21 | 20 | 21 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | -8.2 |
| Input_chip | 17 | 17 | 17 | 17 | 16 | 16 | 16 | 16 | 15 | 15 | 16 | 15 | 15 | 15 | 15 | 15 | 15 | -11.8 |
| Misex3 | 32 | 30 | 31 | 30 | 31 | 31 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | -6.9 |
| Pdc | 53 | 51 | 51 | 51 | 52 | 51 | 51 | 51 | 52 | 50 | 51 | 51 | 52 | 52 | 50 | 52 | 50 | -5.3 |
| Peak_chip | 15 | 16 | 16 | 15 | 15 | 15 | 14 | 15 | 14 | 14 | 13 | 14 | 13 | 13 | 14 | 14 | 14 | -9.3 |
| S298 | 24 | 23 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 21 | 21 | 21 | 22 | 21 | -11.7 |
| S38417 | 32 | 32 | 32 | 31 | 31 | 31 | 31 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 29 | 30 | 29 | -8.1 |
| S38584.1 | 30 | 30 | 30 | 30 | 29 | 29 | 29 | 29 | 29 | 29 | 28 | 29 | 28 | 28 | 29 | 28 | 29 | -4.0 |
| Scale125_chip | 21 | 21 | 20 | 20 | 20 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 19 | 18 | 18 | 18 | -14.3 |
| Scale2_chip | 17 | 17 | 16 | 16 | 16 | 15 | 15 | 15 | 16 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 14 | -15.3 |
| Seq | 34 | 35 | 34 | 34 | 33 | 34 | 34 | 34 | 33 | 33 | 33 | 33 | 33 | 33 | 33 | 34 | 33 | -1.8 |
| Spla | 46 | 45 | 45 | 46 | 45 | 44 | 45 | 44 | 45 | 44 | 45 | 44 | 45 | 45 | 44 | 45 | 45 | -2.2 |
| Tseng | 23 | 23 | 22 | 22 | 22 | 22 | 22 | 22 | 21 | 22 | 21 | 21 | 22 | 21 | 21 | 21 | 21 | -7.8 |
| Warping | 19 | 19 | 18 | 18 | 18 | 18 | 18 | 18 | 17 | 18 | 17 | 17 | 17 | 17 | 17 | 17 | 17 | -11.6 |
| **Geometric Avg** | 27.9 | 27.7 | 27.4 | 27.1 | 26.8 | 26.7 | 26.5 | 26.5 | 26.3 | 26.2 | 26.1 | 26.1 | 26.1 | 25.9 | 26.0 | 26.0 | 25.8 | -7.4 |

*Table A.27 – $W_{min}$ vs # of NN Interconnects for Full Radius 1*

| Buffer Size | Propagation Delay (50% Rise to 50% Fall) (ps) |
|---|---|
| 1x | 29 |
| 2x | 62 |
| 4x | 86 |
| 5x | 108 |
| 10x | 140 |

*Table A.28 – Cascaded Buffer Delays Modelled in 0.18µm CMOS technology*

| Appendix Table | Figure / Table | Page |
|---|---|---|
| A.1 | Fig 3.8, 3.16, 3.20, 4.1, Table 4.4 | 34, 47, 51, 58, 64 |
| A.2 | Fig 4.1 | 58 |
| A.3 | Fig 3.16 | 47 |
| A.4 | Fig 3.8 | 34 |
| A.5 | Fig 3.18 | 49 |
| A.6 | Fig 3.18 | 49 |
| A.7 | Fig 3.20 | 51 |
| A.8 | Fig 3.12, 3.17, 4.2 | 39, 48, 59 |
| A.9 | Fig 4.2 | 59 |
| A.10 | Fig 3.17 | 48 |
| A.11 | Fig 3.12 | 39 |
| A.12 | Fig 3.19 | 49 |
| A.13 | Fig 3.19 | 49 |
| A.14 | Fig 3.9, 4.3 | 35, 60 |
| A.15 | Fig 4.3 | 60 |
| A.16 | Fig 3.9 | 35 |
| A.17 | Fig 4.6 | 65 |
| A.18 | Fig 4.7 | 66 |
| A.19 | Fig 4.4 | 61 |
| A.20 | Fig 4.4 | 61 |
| A.21 | Fig 4.6 | 65 |
| A.22 | Fig 4.7 | 66 |
| A.23 | Fig 3.13, 4.5, Table 4.4 | 40, 62, 64 |
| A.24 | Fig 4.5 | 62 |
| A.25 | Fig 3.13 | 40 |
| A.26 | Fig 4.6 | 65 |
| A.27 | Fig 4.7 | 66 |
| A.28 | N/A | N/A |

*Table A.29 – Key Table Referring Appendix Tables to Figures and Tables in Chapters 3 and 4*

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