University of Toronto

Term Test 2

Date — Nov 20, 2023: 4:10pm

Duration — 50 min

ECE 331 — Analog Electronics

Lecturer — D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

- Equation sheet is on the last page of this test.
- Notation: 15e3 is equivalent to 15×10^3
- · Non-programmable calculator is allowed; No other aids are allowed
- Write using a non-erasable ink.
- Grading indicated by []. Attempt all questions since a blank answer will certainly get 0.

Last Name: _____

First Name: _____

Student #: _____

Question	1	2	3	Total
Points:	5	5	5	15
Score:				

Grading Table

Q1. Consider the circuit shown below where v_o is defined to be $v_{op} - v_{on}$ and all pmos transistors have $V_{ovp} = 0.11V$ while all nmos transistors have $V_{ovn} = 0.25V$. Also, $V_{CM} = 0.88V$ and $I_{D5} = 100\mu$ A.

$$V_{DD} = 1.8V$$

$$V_{tp} = -0.39V$$

$$r_{o3} = r_{o4} = 54k\Omega$$

$$V_{cM} + v_{id}/2$$

$$M_{1}$$

$$M_{2}$$

$$V_{CM} - v_{id}/2$$

$$V_{cM} - v_{id}/2$$

$$V_{tn} = 0.19V$$

$$r_{o1} = r_{o2} = 50k\Omega$$

$$r_{o5} = 60k\Omega$$

[3] [2]

- (a) Find the small-signal gain v_o/v_{id}
- (b) Assuming the small-signal gain is so large that you can ignore the voltage swing on the input differential signal, find the max and minimum output voltage for v_{op} such that transistors remain in the active region.

Solution

(a) This a balanced circuit so we can find the gain of the half circuit M_1/M_3 assuming the source of M_1 is grounded.

In this circuit, $v_o/v_{id} = -(v_{on}/(v_{id}/2))$ due to the following... Define $A_1 = v_{on}/(v_{id}/2)$ (A_1 is a negative gain) $v_{on} = A_1(v_{id}/2)$ and $v_{op} = A_1(-v_{id}/2)$ $v_o = v_{op} - v_{on} = -A_1(v_{id}/2) - A_1(v_{id}/2) = -A_1v_{id}$ So $v_o/v_{id} = -A_1$ where A_1 is the negative gain of the half circuit. Carrying on, we have $I_{D1} = I_{D5}/2 = (100e-6)/2 = 50\mu A$ $g_{m1} = (2 * I_{D1})/V_{ovn} = (2 * (50e-6))/(0.25) = 400\mu A/V$ $R_o = r_{o1}||r_{o3} = (50e3)||(54e3) = 25.96k\Omega$ $v_{on}/(v_{id}/2) = -g_{m1} * R_o = -(400e-6) * (25.96e3) = -10.38V/V$ $v_o/v_{id} = -v_{on}/(v_{id}/2) = -(-10.38) = 10.38V/V$

 $v_o/v_{id} = 10.38 V/V$

(b) With the assumption of a very large small-signal gain, we can assume the input voltage remains at the common-mode voltage, V_{CM} .

The maximum voltage for v_{op} occurs when M_4 is at the edge of triode/active. This occurs when the drain of M_4 one threshold voltage higher than the gate of M_4 (in other words, higher by $|V_{tp}|$).

 $v_{op,max} = V_{B2} + |V_{tp}| = (1.3) + |(-0.39)| = 1.69V$

 $v_{op,max} = 1.69V$

(another approach is to look for V_{SD} of M_4 reaching the overdrive voltage)

The minimum voltage for v_{op} occurs when M_2 is at the edge of triode/active. This occurs when the drain of M_2 is one threshold voltage below the gate of M_2

 $v_{op,min} = V_{CM} - V_{tn} = (0.88) - (0.19) = 0.69 V$

$v_{op,min} = 0.6$	<u>ور</u>	V
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[2]

Q2. A transfer-function has the equation

$$T(s) = \frac{8.8e3(1 + s/1.19e5)}{(1 + s/8.8e1)(1 + s/2.29e3)}$$

- [3] (a) Estimate the gain (in dB) at $\omega = 1.19$ Mrad/s. For this estimate, assume $\omega = 1.19$ Mrad/s is much greater than all the pole/zero frequencies.
 - (b) Estimate the phase (in degrees) at $\omega = 1.19$ Mrad/s. For this estimate, take into account the zero at 1.19e5 while assuming $\omega = 1.19$ Mrad/s is much greater than the pole frequencies.

Solution

(a) Since $\omega = 1.19$ Mrad/s is much greater than each of 1.19e5, 8.8e1, 2.29e3 so we can ignore the "1" in each term so

$$\begin{split} |T(j\omega)| &\approx \frac{|8.8e3(j\omega/1.19e5)|}{|(j\omega/8.8e1)(j\omega/2.29e3)|} \\ |T(j\omega)| &\approx \frac{|8.8e3(j1.19e6/1.19e5)|}{|(j1.19e6/8.8e1)(j1.19e6/2.29e3)|} \\ |T(j\omega)| &\approx 1.25e-2 \\ \text{and in dB, we have} \\ T_{dB} &= 20 * log_{10}(|T(j\omega)|) = -38 \text{ dB} \\ \text{(b) Since } \omega &= 1.19 \text{Mrad/s is much greater than each of } 8.8e1, 2.29e3 \text{ we can write} \\ &\angle T(j\omega) &= \angle (8.8e3) + \angle (1 + j\omega/1.19e5) - \angle (1 + j\omega/8.8e1) - \angle (1 + j\omega/2.29e3) \\ &\angle T(j\omega) \approx 0^\circ + \angle (1 + j1.19e6/1.19e5) - 90^\circ - 90^\circ \\ \text{where we have used } \angle (1 + jk) \approx 90^\circ \text{ when } k \gg 1 \\ &\angle T(j\omega) \approx \arctan[(1.19e6/1.19e5)/(1)] - 180^\circ \\ &\angle T(j\omega) \approx -95.71^\circ \end{split}$$

[2]

[3]

Q3. The small signal model for a common-source amp is shown below.



(a) Find the midBand gain A_M

(b) Use Millers Theorem to find the 2 pole locations, F_1 and F_2 in Hz.

Solution

(a) For the midband gain, we assume all the capacitors limiting the high freq gain are open circuited (in this case, all the capacitors in this circuit).

 $A_M = -g_m * R_L = -(1.8e-3) * (26e3) = -46.8V/V$

(b) Using Millers Theorem, we break C_{gd} into 2 grounded capacitors, C_{m1}/C_{m2}



 $\begin{aligned} C_{m1} &= C_{gd} * (1 - A_M) = (77e - 15) * (1 - (-46.8)) = 3.681 \text{pF} \\ C_{m2} &= C_{gd} * (1 - (1/A_M)) = (77e - 15) * (1 - (1/(-46.8))) = 78.65 \text{fF} \\ \text{So we have 2 poles and the 2 nodes in the circuit resulting in} \\ F_1 &= 1/(2 * \pi * (C_{gs} + C_{m1}) * R_1) = 1/(2 * (3.142) * ((1.3e - 12) + (3.681e - 12)) * (8.8e3)) = 3.631 \text{MHz} \\ F_2 &= 1/(2 * \pi * (C_{m2} + C_L) * R_L) = 1/(2 * (3.142) * ((78.65e - 15) + (770e - 15)) * (26e3)) = 7.213 \text{MHz} \end{aligned}$

Equation Sheet

