

University of Toronto

Term Test 1

Date - Oct 23, 2015 (1:10pm to 2:00pm)

Duration: 50 min

ECE331 — Analog Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY

1. Equation sheet is on last page of test.
 2. Unless otherwise stated, use transistor parameters on equation sheet and assume $g_m r_o \gg 1$.
 3. Non-programmable calculator allowed; No other aids allowed
 4. Grading indicated by []. Attempt all questions since a blank answer will certainly get 0.
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Question	Mark
1	
2	
3	
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Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 24)

[6] Question 1:

a) Find the intrinsic gain of a transistor with $L = 0.25\mu\text{m}$ and $V_{\text{ov}} = 0.2\text{V}$ (based on the 0.18 μm parameters given on the equation sheet)

b) If a $g_m = 2\text{mA/V}$ is required for the transistor in a), what must I_D and W be?

[6] **Question 2:** Assume an nmos transistor (based on the 0.18 μ m parameters given on the equation sheet) with $W = 4\mu\text{m}$, $L = 0.25\mu\text{m}$ is biased with $V_{ov} = 0.3\text{V}$ and $V_{DS} = 0.8\text{V}$.

a) Find the r_o for this device.

b) If V_{DS} is decreased by 0.1V, what is the corresponding change in I_D ?

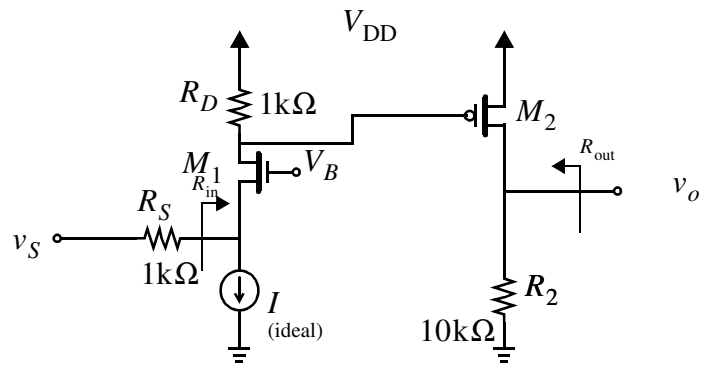
c) If a cascode current mirror makes use of two nmos transistors biased with the same current as in a), find r_o and the change in I_D for a 0.1V change in the mirror output voltage. (assume both transistors remain in the active region).

[6] Question 3:

a) Given 2 current sources from V_{DD} where each are $10\mu\text{A}$, design a wide-swing cascode current-mirror circuit (including bias voltage generation) that gives an nmos output of $30\mu\text{A}$. Assume all transistor lengths are $0.18\mu\text{m}$ and the nmos current mirror output transistors have $W = 3\mu\text{m}$. Show the widths of all transistors on your schematic. (Hint: there should be 5 nmos transistors and 2 current sources on your schematic).

b) Assuming $V_{tn} = 0.3\text{V}$ and $V_{ov} = 0.2\text{V}$, show on your circuit above, the values for the 2 bias voltages.

[6] Question 4: Consider the circuit below.



$$g_{m1} = g_{m2} = 2\text{mA/V}$$

$$r_{o1} = r_{o2} = 20\text{k}\Omega$$

a) Find R_{in} and R_{out} .

b) Find v_o/v_s

Analog Electronics

Equation Sheet

Constants: $k = 1.38 \times 10^{-23} \text{ JK}^{-1}$; $q = 1.602 \times 10^{-19} \text{ C}$; $V_T = kT/q \approx 26\text{mV}$ at $300 \text{ }^\circ\text{K}$;

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}; k_{ox} = 3.9; C_{ox} = (k_{ox}\epsilon_0)/t_{ox}$$

NMOS: $k_n = \mu_n C_{ox} (W/L)$; $V_{in} > 0$; $v_{DS} \geq 0$; $v_{ov} = v_{GS} - V_{in}$

(triode) $v_{DS} \leq v_{ov}$ (or $v_D < v_G - V_{in}$); $i_D = k_n((v_{ov})v_{DS} - (v_{DS}^2/2))$

(active) $v_{DS} \geq v_{ov}$; $i_D = 0.5k_n v_{ov}^2 (1 + \lambda v_{DS})$; $g_m = k_n V_{ov} = 2I_D/V_{ov} = \sqrt{2k_n I_D}$; $r_s = 1/g_m$; $r_o = L/(|\lambda|I_D)$

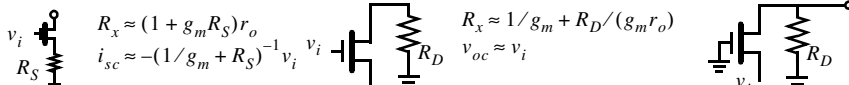
PMOS: $k_p = \mu_p C_{ox} (W/L)$; $V_{tp} < 0$; $v_{SD} \geq 0$; $v_{ov} = v_{SG} - |V_{tp}|$

(triode) $v_{SD} \leq v_{ov}$ (or $(v_D > v_G + |V_{tp}|)$); $i_D = k_p((v_{ov})v_{SD} - (v_{SD}^2/2))$

(active) $v_{SD} \geq v_{ov}$; $i_D = 0.5k_p v_{ov}^2 (1 + |\lambda|v_{SD})$; $g_m = k_p V_{ov} = 2I_D/V_{ov} = \sqrt{2k_p I_D}$; $r_s = 1/g_m$; $r_o = L/(|\lambda|I_D)$

BJT: (active) $i_C = I_S e^{(v_{BE}/V_T)} (1 + (v_{CE}/V_A))$; $g_m = \alpha/r_e = I_C/V_T$; $r_e = V_T/I_E$; $r_\pi = \beta/g_m$; $r_o = |V_A|/I_C$

$$i_C = \beta i_B; i_E = (\beta + 1)i_B; \alpha = \beta/(\beta + 1); i_C = \alpha i_E; R_b = (\beta + 1)(r_e + R_E); R_e = (R_B + r_\pi)/(\beta + 1)$$

Cascode:  $R_x \approx (1 + g_m R_S) r_o$; $i_{sc} \approx -(1/g_m + R_S)^{-1} v_i$; $R_x \approx 1/g_m + R_D/(g_m r_o)$; $v_{oc} \approx v_i$; $v_o/v_i \approx g_m(r_o \parallel R_D)$ (Approx due to $g_m r_o \gg 1$)

Diff Pair: $A_d = g_m R_D$; $A_{CM} = -(R_D/(2R_{SS}))((\Delta R_D)/R_D)$; $A_{CM} = -(R_D/(2R_{SS}))((\Delta g_m)/g_m)$

$$V_{os} = \Delta V_i; V_{os} = (V_{ov}/2)((\Delta R_D)/R_D); V_{os} = (V_{ov}/2)((\Delta(W/L))/(W/L))$$

1st order: step response $y(t) = Y_\infty - (Y_\infty - Y_{0+})e^{-t/\tau}$ unity gain freq for $T(s) = \frac{A_M}{1 + s/\omega_{3dB}}$ $f_t \approx |A_M|\omega_{3dB}$ when $A_M \gg 1$

Freq: for real axis poles/zeros $T(s) = k_{dc} \frac{(1 + s/z_1)(1 + s/z_2) \dots (1 + s/z_m)}{(1 + s/\omega_1)(1 + s/\omega_2) \dots (1 + s/\omega_n)}$

OTC estimate $f_H = 1/(2\pi \sum \tau_i)$; dominant pole estimate $f_H = 1/(2\pi \tau_{max})$

Miller: $Z_1 = Z/(1 - K)$; $Z_2 = Z/(1 + K)$

Mos caps: $C_{gs} = (2/3)WLC_{ox} + WL_{ov}C_{ox}$; $C_{gd} = WL_{ov}C_{ox}$; $C_{db} = C_{db0}/(\sqrt{1 + V_{db}/V_0})$

$$f_t = g_m/(2\pi(C_{gs} + C_{gd}))$$
 assuming $C_{gd} \ll C_{gs}$ $f_t = (3\mu V_{ov})/(4\pi L^2)$

Feedback: $A_f = A/(1 + A\beta)$; $x_i = (1/(1 + A\beta))x_s$; $dA_f/A_f = (1/(1 + A\beta))dA/A$; $\omega_{Hf} = \omega_H(1 + A\beta)$; $\omega_{Lf} = \omega_L/(1 + A\beta)$

Loop Gain $L \equiv -s_r/s_i$; $A_f = A_\infty(L/(1 + L)) + d/(1 + L)$; $Z_{port} = Z_{p0}((1 + L_S)/(1 + L_O))$

PM = $\angle L(j\omega_1) + 180$; GM = $-|L(j\omega_{180})|_{dB}$

Pole Splitting $\omega_{p1}' \approx 1/(g_m R_2 C_f R_1)$; $\omega_{p2}' \approx (g_m C_f)/(C_1 C_2 + C_f(C_1 + C_2))$

Pole Pair: $s^2 + (\omega_o/Q)s + \omega_o^2 = 0$; $Q \leq 0.5 \Rightarrow$ real poles; $Q > 1/\sqrt{2} \Rightarrow$ freq resp peaking

Power Amps: Class A: $\eta = (1/4)(\hat{V}_o/(IR_L))(\hat{V}_o/V_{CC})$ Class B: $\eta = (\pi/4)(\hat{V}_o/V_{CC})$; $P_{DN_max} = V_{CC}^2/(\pi^2 R_L)$

Class AB: $i_n i_p = I_Q^2$

2-stage cmos opamp: $\omega_{p1} \approx (1/(R_1 G_{m2} R_2 C_c))$; $\omega_{p2} \approx (G_{m2}/C_2)$; $\omega_z \approx (1/(C_c((1/G_{m2}) - R)))$

$$SR = I/C_c = \omega_i V_{ov1}; \text{ will not SR limit if } \omega_i \hat{V}_o < SR$$

MOS Transistor: CMOS basic parameters. Channel length = $0.18\mu m$

	V_t (V)	μC_{ox} ($\mu A/V^2$)	λ' ($\mu m/V$)	C_{ox} ($fF/\mu m^2$)	t_{ox} (nm)	L_{ov} (μm)	$\frac{C_{db0}}{W}$ ($\frac{fF}{\mu m}$)
NMOS	0.4	240	0.05	8.5	4	0.04	0.3
PMOS	-0.4	60	-0.05	8.5	4	0.04	0.3