Problem Set 3

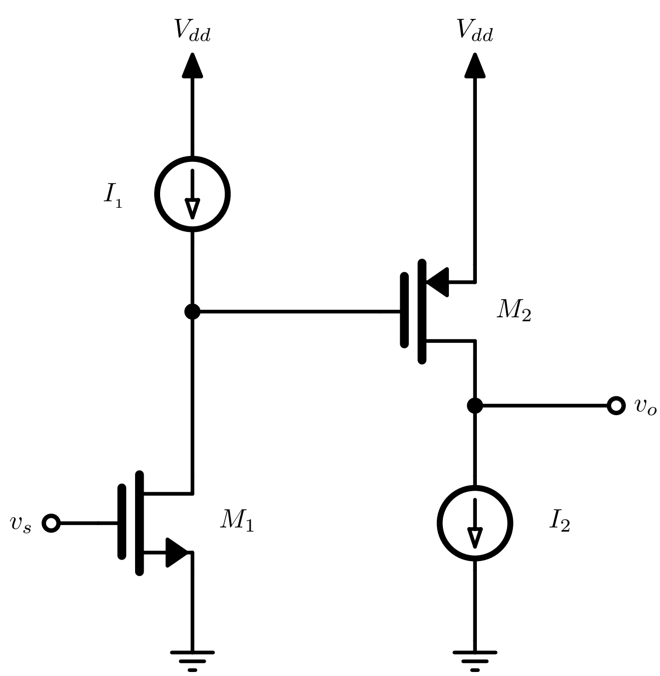
Q1. Given an NMOS transistor fabricated in a process for which $k_n' = 200\,\mu\text{A/V}^2$ and $V_A' = 20\,\text{V}/\mu\text{m}$, determine the intrinsic gain A_o and design parameters I_D and W assuming $gm = 2\,\text{mA/V}$, $L = 500\,\text{nm}$ and $V_{ov} = 0.25\,\text{V}$.

Q2. Given an NMOS transistor fabricated in a certain process, an intrinsic gain of $A_{o1} = 80\,\text{V/V}$ can be achieved with $I_{D1} = 100\,\mu\text{A}$.
a) Determine the achievable intrinsic gain for the same transistor with a bias current of $I_{D2} = 25\,\mu\text{A}$ and $I_{D3} = 400\,\mu\text{A}$.
b) For each current, find the factor by which A_o changes relative to its initial value.

Q3. Given an $0.18\mu m$ NMOS transistor fabricated with $k_n' = 387\,\mu\text{A/V}^2$ and $V_A' = 5\,\text{V}/\mu\text{m}$, an intrinsic gain of $A_o = 25\,\text{V/V}$ and a $gm = 1\,\text{mA/V}$ is required. Find the required W, W/L and bias current I_D. (Assume $L = 0.3\mu m$).

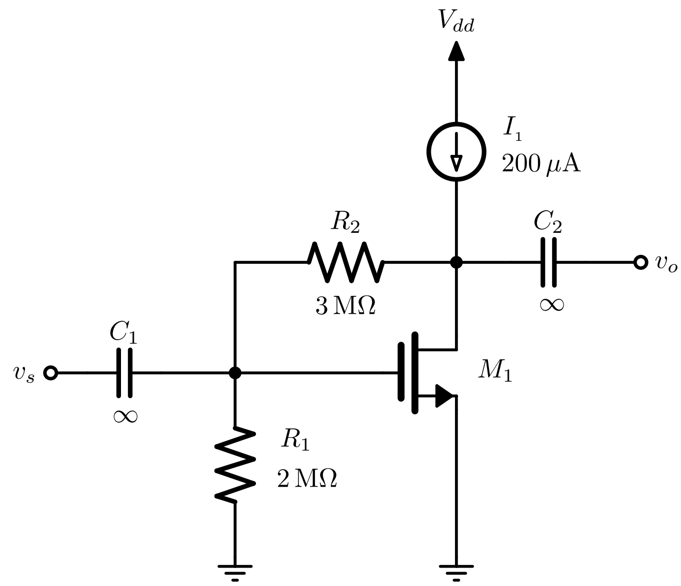
Q4. Given a process with $k_n' = 200\,\mu\text{A/V}^2$ and $V_A' = 20\,\text{V}/\mu\text{m}$, design a current-source-loaded common-source amplifier for operation at $I_D = 50\,\mu\text{A}$ with $V_{ov} = 0.2\,\text{V}$. The amplifier must achieve an open-circuit voltage gain of $A_{oc} = -100\,\text{V/V}$. Determine L and W/L. (Assume the current-source load is ideal).

Q5. Given a two-stage common-source amplifier where $V_{AN} = |V_{AP}|$ and assuming the biasing current sources I_1 and I_2 have output resistances equal to those of M_1 and M_2 respectively, determine an expression for the total voltage gain in terms of gm_1, gm_2, r_{o1} and r_o2.



Q6. Given transistor M_1 which has $k_n' * W/L = 2\,\text{mA/V}^2$, $V_A' = 20\,\text{V}/\mu\text{m}$, and $V_t = 0.5\,\text{V}$:
a) Ignoring any DC current in R_2 and assuming $r_o \to \infty$, determine V_{GS}.
b) Now determine the DC current in R_2, determine V_{DS}, and justify your neglection of the DC current when calculating V_{GS}.

c) Determine the small-signal voltage gain V_o/V_s. (Assume an ideal current source)
d) Assuming the negative swing of the output limits the overall output swing, what is the min output voltage, max output voltage and output peak-to-peak swing?
e) What is the corresponding input amplitude?



Q7. In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 40. If the transistor is operated at $V_{ov} = 0.2\,\mathrm{V}$, what must its V_A be? If the process technology specifies V_A' as $5\,\mathrm{V}/\mu\mathrm{m}$, what channel length must the transistor have?

Q8. Design the cascode amplifier of Fig. 1 to obtain $g_{m1} = 1\,\mathrm{mA/V}$ and $R_o = 400\,\mathrm{k}\Omega$. Use a 0.18-$\mu m$ technology for which $V_{tn} = 0.5\,\mathrm{V}$, $V_A' = 5\,\mathrm{V}/\mu\mathrm{m}$ and $k_n' = 400\,\mu\mathrm{A/V}^2$. Determine L, W/L, V_{G2}, and I. Use identical transistors operated at $V_{ov} = 0.2\,\mathrm{V}$, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

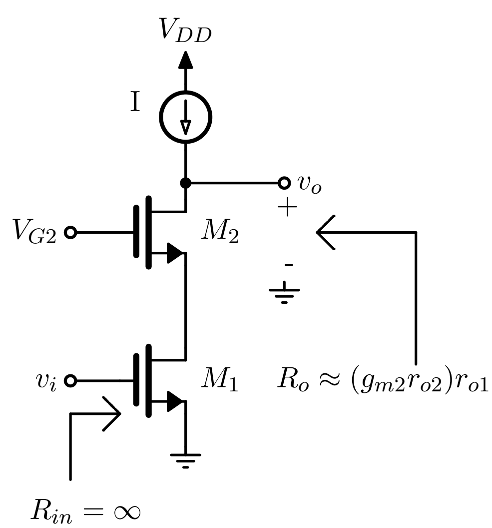


Figure 1: cascode amplifier

Q9. Design the circuit of Fig. 2 to provide an output of $100\,\mu$A. Use $V_{DD} = 3.3\,\mathrm{V}$, and assume the PMOS transistors to have $\mu_p C_{ox} = 60\,\mu\mathrm{A/V}^2$, $V_{tp} = -0.8\,\mathrm{V}$, and $|V_A| = 5\,\mathrm{V}$. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2\,\text{V}$, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4}. What is the highest allowable voltage at the output? What is the value of R_o?

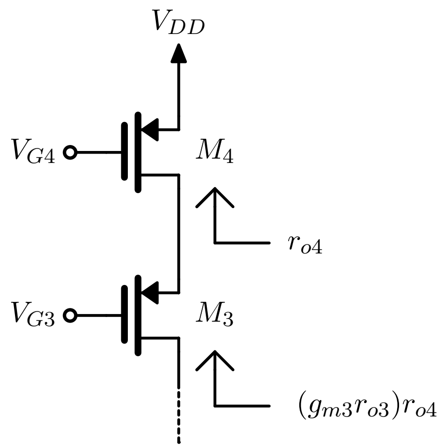


Figure 2: cascode PMOS source

Q10. For $V_{DD} = 1.8\,\text{V}$ and using $I_{ref} = 100\,\mu\text{A}$, it is required to design the circuit of Fig. 3 to obtain an output current whose nominal value is $100\,\mu\text{A}$. Find R if M_1 and M_2 are matched with channel lengths of 500 nm, channel widths of $4\,\mu\text{m}$, $V_t = 0.5\,\text{V}$, and $k'_n = 400\,\mu\text{A/V}^2$. What is the lowest possible value for V_o? Assuming that for this process technology the Early voltage is $V'_A = 10\,\text{V}/\mu\text{m}$, find the output resistance of the current source. Also, find the current change in output current resulting from a $+0.5\,\text{V}$ change in V_o

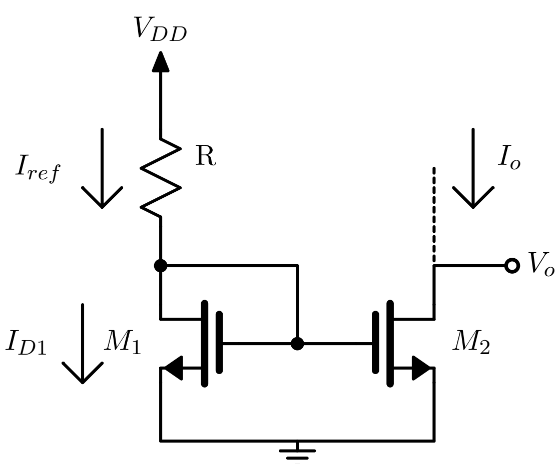
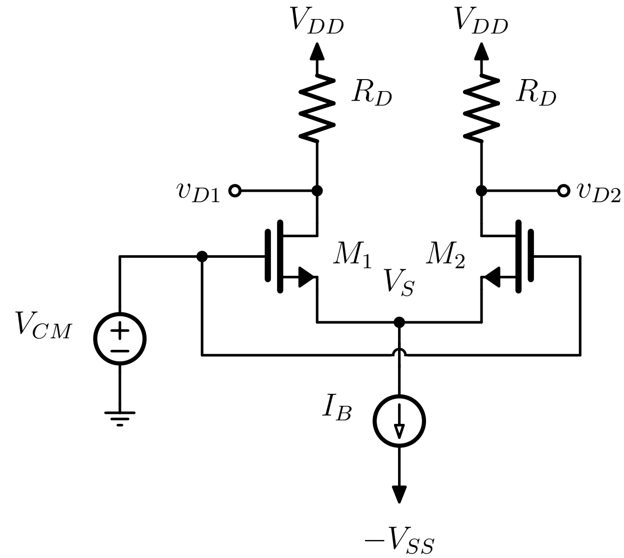


Figure 3: NMOS current mirror

Q11. Consider the NMOS diff pair shown below with a common-mode input, V_{CM} and $V_{DD} = 1\,\text{V}$, $V_{SS} = 1.1\,\text{V}$, $\mu_n C_{ox} = 400\,\mu\text{A/V}^2$, $(W/L)_{1,2} = 12.5$, $V_{tn} = 0.4\,\text{V}$, $I_B = 200\,\mu\text{A}$, $R_D = 5\,\text{k}\Omega$. In addition, the minimum voltage required across I_B is $0.2\,\text{V}$ so that the current source transistor creating I_B does not leave the active region. Ignore channel length modulation.

(a) For $V_{CM} = 0.1\,\text{V}$, find V_{ov1}, V_{GS1}, V_S, I_{D1} and V_{D1}
(b) What is the highest value for V_{CM} such than no transistors leave the active region?



(c) What is the lowest value for V_{CM} such than no transistors leave the active region?