Problem Set 3

Q1. Given an NMOS transistor fabricated in a process for which $k'_n = 200\,\mu\text{A/V}^2$ and $V'_A = 20\,\text{V}/\mu\text{m}$, determine the intrinsic gain A_o and design parameters I_D and W assuming $gm = 2\,\text{mA/V}$, $L = 500\,\text{nm}$ and $V_{ov} = 0.25\,\text{V}$.

Solution

First, the required current is determined.
As per the equation: $g_m = 2 * I_D/V_{ov}$, a rearange can be performed:
$I_D = gm * V_{ov}/2 = (2e-3) * (0.25)/2 = 250\,\mu\text{A}$
$I_D = 250\,\mu\text{A}$

Second, the width is determined. (Hint: match up the units!)
As per the equation: $I_D = (k'_n/2)(W/L)V_{ov}^2$ where $k'_n = u_n * C_{ox}$, a rearange can be performed:
$W = (2 * I_D * L)/(k'_n * V_{ov}^2) = (2 * (250e-6) * (500e-9))/((200e-6) * (0.25)^2) = 20\,\mu\text{m}$
$W = 20\,\mu\text{m}$

Finally, the intrinsic gain can be determinde. With a rearange of equation $A_o = gm * r_o$, we get:
$A_o = V'_A * 10^6 * \sqrt{2 * k'_n * W * L}/\sqrt{I_D} = (20) * 10^6 * \sqrt{2 * (200e-6) * (20e-6) * (500e-9)}/\sqrt{(250e-6)} = 80$ V
$A_o = 80\,\text{V/V}$

Answer

$I_D = 250\,\mu\text{A}$; $W = 20\,\mu\text{m}$; $A_o = 80\,\text{V/V}$

Q2. Given an NMOS transistor fabricated in a certain process, an intrinsic gain of $A_{o1} = 80\,\text{V/V}$ can be achieved with $I_{D1} = 100\,\mu\text{A}$.
a) Determine the achievable intrinsic gain for the same transistor with a bias current of $I_{D2} = 25\,\mu\text{A}$ and $I_{D3} = 400\,\mu\text{A}$.
b) For each current, find the factor by which A_o changes relative to its initial value.

Solution

As we know: $A_o = gm * r_o = V'_A * \sqrt{2 * u_n * C_{ox} * W * L}/\sqrt{I_D}$.
As such the constants can be determined:
$V'_A * \sqrt{2 * u_n * C_{ox} * W * L} = A_{o1} * \sqrt{I_{D1}} = (80) * \sqrt{(100e-6)} = 0.8\,\text{A}$

With this:
$A_{o2} = V'_A * \sqrt{2 * u_n * C_{ox} * W * L}/\sqrt{I_{D2}} = (0.8)/\sqrt{(25e-6)} = 160\,\text{V/V}$
$A_{o2} = 160\,\text{V/V}$

$A_{o3} = V'_A * \sqrt{2 * u_n * C_{ox} * W * L}/\sqrt{I_{D3}} = (0.8)/\sqrt{(400e-6)} = 40\,\text{V/V}$
$A_{o3} = 40\,\text{V/V}$

The gm ratios can now be calculated as they are proportional to the change in intrinsic gain:
$K_a = A_{o2}/A_{o1} = (160)/(80) = 2$
$K_a = 2$

$K_b = A_{o3}/A_{o1} = (40)/(80) = 0.5$
$K_b = 0.5$

Answer

$A_{o2} = 160\,\text{V/V}$; $A_{o3} = 40\,\text{V/V}$; $K_a = 2$; $K_b = 0.5$

Q3. Given an 0.18μm NMOS transistor fabricated with $k'_n = 387\,\mu\text{A/V}^2$ and $V'_A = 5\,\text{V}/\mu\text{m}$, an intrinsic gain of $A_o = 25\,\text{V/V}$ and a $gm = 1\,\text{mA/V}$ is required. Find the required W, W/L and bias current I_D. (Assume $L = 0.3\mu m$).

Solution

As we know, the intrinsic gain of a transistor is $A_o = gm * r_o$.
By substitution, we get the equation:
$A_o = V'_A * \sqrt{2 * u_n * C_{ox} * W * L}/\sqrt{I_D}$ where $k'_n = u_n * C_{ox}$.

With further rearanging, we get:
$W * L/I_D = (A_o/V'_A/10^6)^2/(2 * k'_n) = ((25)/(5)/10^6)^2/(2 * (387e - 6)) = 32.3\,\text{nm}^2/\text{A}$
$W/I_D = W * L/I_D/L = (32.3e - 9)/(300e - 9) = 0.1077\,\text{m/A}$

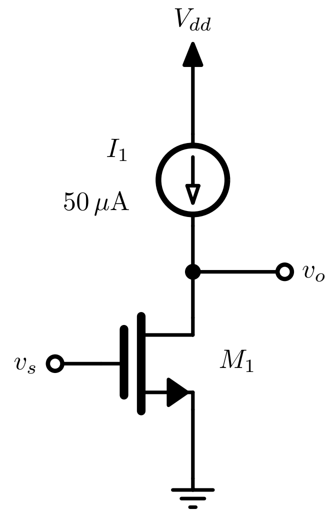
We have one equation with two unknowns. We can thus arbitrarily chose a value for the current, suppose $I_D = 60\,\mu\text{A}$:
$W = W/I_D * I_D = (0.1077) * (60e - 6) = 6.46\,\mu\text{m}$
$I_D = 60\,\mu\text{A}$; $W = 6.46\,\mu\text{m}$
And finally:
$W/L = W/L = (6.46e - 6)/(300e - 9) = 21.53$
$W/L = 21.53$
Note: many answers are possible!

Answer

$W = 6.46\,\mu\text{m}$; $W/L = 21.53$; $I_D = 60\,\mu\text{A}$

Q4. Given a process with $k'_n = 200\,\mu\text{A/V}^2$ and $V'_A = 20\,\text{V}/\mu\text{m}$, design a current-source-loaded common-source amplifier for operation at $I_D = 50\,\mu\text{A}$ with $V_{ov} = 0.2\,\text{V}$. The amplifier must achieve an open-circuit voltage gain of $A_{oc} = -100\,\text{V/V}$. Determine L and W/L. (Assume the current-source load is ideal).

Solution



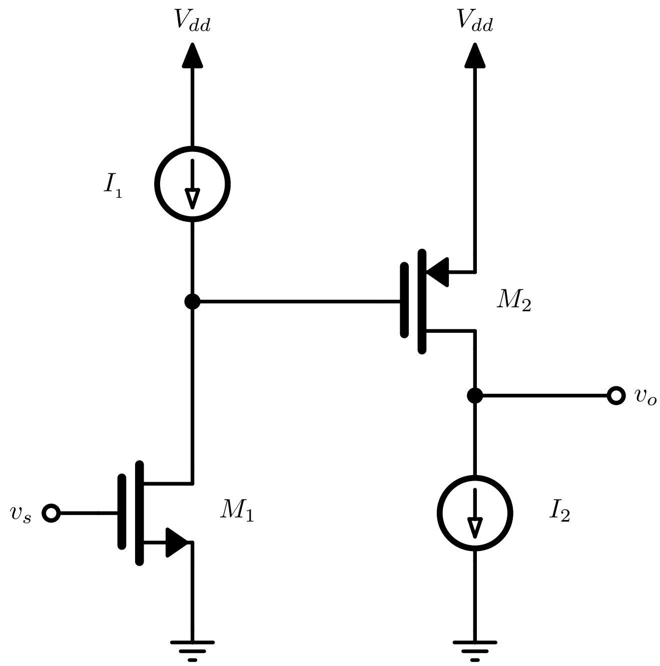
First, the W/L ratio can be determined. By rearanging: $I_D = k_n'/2 * W/L * V_{ov}^2$, we can get:
$W/L = 2 * I_D/(k_n' * V_{ov}^2) = 2 * (50e-6)/((200e-6) * (0.2)^2) = 12.5$
$W/L = 12.5$

Second, the transistor length can be determined:
$A_{oc} = -gm * r_{out} = -2 * I_D/V_{ov} * V_A/I_D$, where $V_A = V_A' * L$.
As such:
$L = -A_{oc} * V_{ov}/(2 * V_A' * 10^6) = -(-100) * (0.2)/(2 * (20) * 10^6) = 500\,\text{nm}$
$L = 500\,\text{nm}$

Answer

$W/L = 12.5\,;\ L = 500\,\text{nm}$

Q5. Given a two-stage common-source amplifier where $V_{AN} = |V_{AP}|$ and assuming the biasing current sources I_1 and I_2 have output resistances equal to those of M_1 and M_2 respectively, determine an expression for the total voltage gain in terms of gm_1, gm_2, r_{o1} and r_o2.



Solution

Looking at the first stage, we get a voltage transfer function of:
$A_1 = -gm_1 * r_{out1} = -gm_1 * r_{o1}/2$

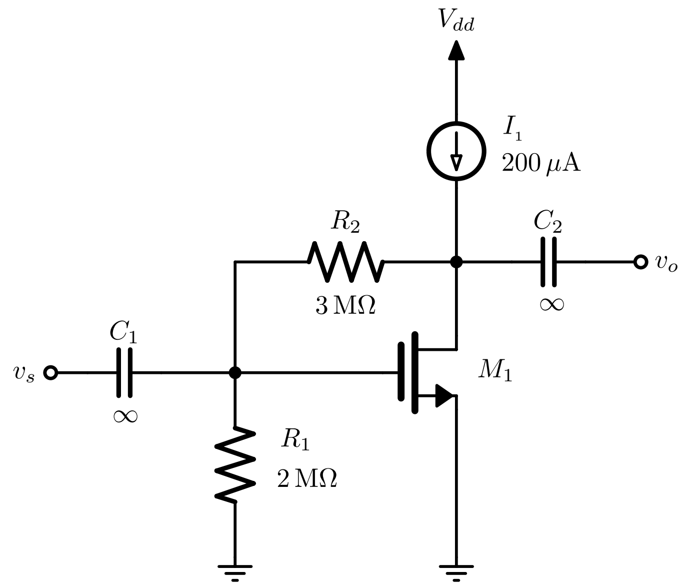
Looking at the second stage, we get a voltage transfer function of:
$A_2 = -gm_2 * r_{out2} = -gm_2 * r_{o2}/2$

As such, the total transfer function is:
$A = A_1 * A_2 = gm_1 * gm_2 * r_{o1} * r_{o2}/4$;
$A = gm_1 * gm_2 * r_{o1} * r_{o2}/4$

Answer

$A = gm_1 * gm_2 * r_{o1} * r_{o2}/4$

Q6. Given transistor M_1 which has $k_n' * W/L = 2\,\text{mA/V}^2$, $V_A' = 20\,\text{V}/\mu\text{m}$, and $V_t = 0.5\,\text{V}$:
a) Ignoring any DC current in R_2 and assuming $r_o \to \infty$, determine V_{GS}.
b) Now determine the DC current in R_2, determine V_{DS}, and justify your neglection of the DC current when calculating V_{GS}.
c) Determine the small-signal voltage gain V_o/V_s. (Assume an ideal current source)
d) Assuming the negative swing of the output limits the overall output swing, what is the min output voltage, max output voltage and output peak-to-peak swing?
e) What is the corresponding input amplitude?



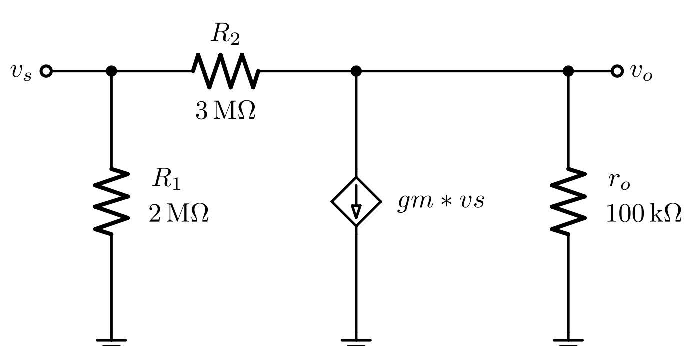
Solution

a) Assuming all the current goes through the channel and none goes into R_2 since it is so large:
$I_D = k'_n/2 * (W/L) * (V_{GS} - V_t)^2$
$V_{GS} = \sqrt{2 * I_D/k'_n * W/L} + V_t = \sqrt{2 * (200e - 6)/(2e - 3)} + (0.5) = 0.9472\,\text{V}$
$V_{GS} = 0.9472\,\text{V}$

b) Rearanging the voltage division rule: $V_{GS} = V_{DS} * R_1/(R_1 + R_2)$
$V_{DS} = V_{GS} + R_2 * V_{GS}/R_1 = (0.9472) + (3e6) * (0.9472)/(2e6) = 2.368\,\text{V}$
$V_{DS} = 2.368\,\text{V}$

As such, the current in R_2 is:
$I_{FB} = V_{DS}/(R_1 + R_2) = (2.368)/((2e6) + (3e6)) = 473.6\,\text{nA}$
This is quite small compared to I_{D1} so ignoring this current in part (a) is justified.

c) First, gm and r_o is calculated:
$gm = 2 * I_D/(V_{GS} - V_t) = 2 * (200e - 6)/((0.9472) - (0.5)) = 894.4\,\mu\text{A/V}$
$r_o = V'_A/I_D = (20)/(200e - 6) = 100\,\text{k}\Omega$



Second, using KCL:
$(V_o - V_i)/R_2 + gm * V_i + V_o/r_o = 0$
$A_v = (1/R_2 - gm)/(1/R_2 + 1/r_o) = (1/(3e6) - (894.4e-6))/(1/(3e6) + 1/(100e3)) = -86.53\,\text{V/V}$
$A_v = -86.53\,\text{V/V}$

d) For M_1 to remain in the active region, we require that $V_{D1} \geq V_{G1} - V_t$
Now let us write V_{G1} as $V_G + \Delta V_G$ and V_{D1} as $V_D + \Delta V_D$
where V_G and V_D are the bias voltages for the gate and drain respectively
So we have the requirement
$V_D + \Delta V_D \geq V_G + \Delta V_G - V_t$
Now, from small-signal analysis, $A_v \equiv \Delta V_D/\Delta V_G$ or $\Delta V_G = \Delta V_D/A_v$. Putting this into the above equation, we have
$V_D + \Delta V_D \geq V_G + (\Delta V_D/A_v) - V_t$
and setting it to equality to find the max ΔV_D (which is the min V_{D1}), we have
$\Delta V_D(1 - 1/A_v) = V_G - V_t - V_D$
Now, in this case, $A_v \gg 1$ so we can ignore $1/A_v$ resulting in
$\Delta V_D = V_G - V_t - V_D = (0.9472) - (0.5) - (2.368) = -1.921$
This give the max output peak-to-peak output swing of
$V_{o,pp} = 2 * |\Delta V_D| = 2 * |(-1.921)| = 3.842\,\text{V}$
$V_{o,min} = V_D + \Delta V_D = (2.368) + (-1.921) = 0.4472\,\text{V}$
$V_{o,max} = V_D - \Delta V_D = (2.368) - (-1.921) = 4.289\,\text{V}$

e) The maximum input swing is related by:
$V_{s,pp} = V_{o,pp}/|A_v| = (3.842)/|(-86.53)| = 44.4\,\text{mV}$
Since V_s is biassed at $V_{GS} = 0.9472\,\text{V}$, the min/max values are
$V_{s,min} = V_{GS} - V_{s,pp}/2 = (0.9472) - (44.4e-3)/2 = 0.925\,\text{V}$
$V_{s,max} = V_{GS} + V_{s,pp}/2 = (0.9472) + (44.4e-3)/2 = 0.9694\,\text{V}$

Note that in this case, since the swing on V_{G1} is so small, we could have determined that the min voltage on V_{D1} was equal to $V_{ov} = V_G - V_t$ and have found the approx answer to part (d) much quicker.

Answer

a) $V_{GS} = 0.9472\,\text{V}$
b) $V_{DS} = 2.368\,\text{V}$
c) $A_v = -86.53\,\text{V/V}$
d) $V_{o,pp} = 3.842\,\text{V}$; $V_{o,min} = 0.4472\,\text{V}$; $V_{o,max} = 4.289\,\text{V}$
e) $V_{s,pp} = 44.4\,\text{mV}$; $V_{s,min} = 0.925\,\text{V}$, $V_{s,max} = 0.9694\,\text{V}$

Q7. In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 40. If the transistor is operated at $V_{ov} = 0.2\,\text{V}$, what must its V_A be? If the process technology specifies V'_A as $5\,\text{V}/\mu\text{m}$, what channel length must the transistor have?

Solution

$K = 40 = g_{m2} r_{o2} = \frac{V_A}{V_{ov}/2}$

so that
$V_A = K * V_{ov}/2 = (40) * (0.2)/2 = 4\,\text{V}$
If $V_A' = 5\,\text{V}/\mu\text{m}$,
$L = V_A/V_A' = (4)/(5e6) = 800\,\text{nm}$

Answer

$V_A = 4\,\text{V}$
$L = 800\,\text{nm}$

Q8. Design the cascode amplifier of Fig. 1 to obtain $g_{m1} = 1\,\text{mA/V}$ and $R_o = 400\,\text{k}\Omega$. Use a 0.18-$\mu m$ technology for which $V_{tn} = 0.5\,\text{V}$, $V_A' = 5\,\text{V}/\mu\text{m}$ and $k_n' = 400\,\mu\text{A/V}^2$. Determine L, W/L, V_{G2}, and I. Use identical transistors operated at $V_{ov} = 0.2\,\text{V}$, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

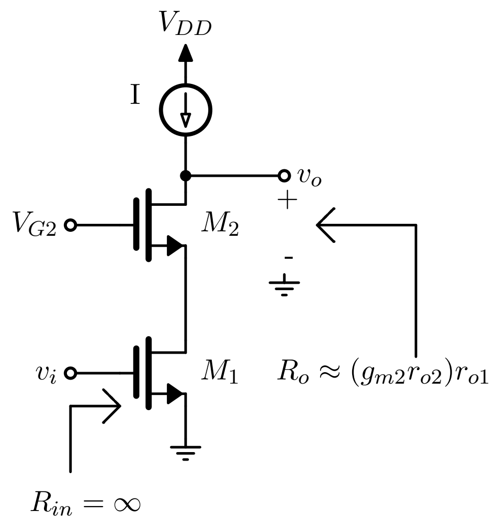


Figure 1: cascode amplifier

Solution

$g_{m1} = \frac{2I_D}{V_{ov}}$, so, $I_D = g_{m1} * V_{ov}/2 = (1e-3) * (0.2)/2 = 100\,\mu\text{A}$
$I_D = 100\,\mu\text{A}$
$R_o = (g_{m2}r_{o2})r_{o1}$
However, if we make $g_{m2} = g_{m1} = g_m$ and $r_{o1} = r_{o2} = r_o$, we can say that:
$r_o = \sqrt{R_o/g_{m1}} = \sqrt{(400e3)/(1e-3)} = 20\,\text{k}\Omega$
Since $r_o = 20\,\text{k}\Omega = \frac{V_A' L}{I_D}$,
$L = I_D * r_o/V_A' = (100e-6) * (20e3)/(5e6) = 400\,\text{nm}$
$L = 400\,\text{nm}$
$g_m = \sqrt{2k_n'(W/L)I_D}$ so that
$W/L = g_m^2/(2 * k_n' * I_D) = (1e-3)^2/(2 * (400e-6) * (100e-6)) = 12.5$
$W/L = 12.5$

For maximum negative excursion at the output, we want the MOSFETs to be biased so that each transistor can reach $V_{DS} = V_{ov} = 0.2\,\text{V}$.
Set $V_{G2} = V_{tn} + V_{ov} + V_{ov} = (0.5) + (0.2) + (0.2) = 0.9\,\text{V}$
$V_{G2} = 0.9\,\text{V}$
Minimum output voltage will be:

$V_{omin} = 2 * V_{ov} = 2 * (0.2) = 0.4\,\text{V}$
$V_{omin} = 0.4\,\text{V}$

Answers

$I_D = 100\,\mu\text{A}$
$L = 400\,\text{nm}$
$W/L = 12.5$
$V_{G2} = 0.9\,\text{V}$
$V_{omin} = 0.4\,\text{V}$

Q9. Design the circuit of Fig. 2 to provide an output of $100\,\mu$A. Use $V_{DD} = 3.3\,\text{V}$, and assume the PMOS transistors to have $\mu_p C_{ox} = 60\,\mu\text{A/V}^2$, $V_{tp} = -0.8\,\text{V}$, and $|V_A| = 5\,\text{V}$. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2\,\text{V}$, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4}. What is the highest allowable voltage at the output? What is the value of R_o?

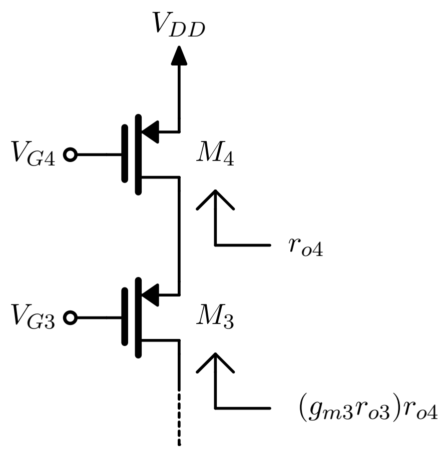


Figure 2: cascode PMOS source

Solution

$I_{D3} = I_{D4} = I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)V_{ov}^2$
$W/L = 2 * I_D/(\mu_p C_{ox} * V_{ov}^2) = 2 * (100e-6)/((60e-6) * (0.2)^2) = 83.33$
$W/L = 83.33$
For V_{G4} :
$V_{G4} = V_{DD} - |V_{tp}| - |V_{ov}| = (3.3) - |(-0.8)| - |(0.2)| = 2.3\,\text{V}$
$V_{G4} = 2.3\,\text{V}$
For maximum swing:
$V_{SDmin} = |V_{ov}| = 0.2\,\text{V}$
so, V_{D4} would be:
$V_{D4} = V_{DD} - V_{ov} = (3.3) - (0.2) = 3.1\,\text{V}$
V_{G3} must be:
$V_{G3} = V_{D4} - |V_{tp}| - |V_{ov}| = (3.1) - |(-0.8)| - |(0.2)| = 2.1\,\text{V}$
$V_{G3} = 2.1\,\text{V}$
The highest allowable output will be:
$V_{omax} = V_{DD} - |V_{ov}| - |V_{ov}| = 2.9\,\text{V}$
$V_{omax} = 2.9\,\text{V}$
From Fig. 2, $R_o = (g_{m3}r_{o3})r_{o4}$

$r_{o3} = r_{o4} = r_o = |V_A|/|I_D| = (5)/|(100e-6)| = 50\,\text{k}\Omega$
$g_m = |I_D|/(|V_{ov}|/2) = |(100e-6)|/(|(0.2)|/2) = 1\,\text{mA/V}$
$R_o = g_m * r_o^2 = (1e-3)*(50e3)^2 = 2.5\,\text{M}\Omega$
$R_o = 2.5\,\text{M}\Omega$

Answers

$W/L = 83.33$
$V_{G4} = 2.3\,\text{V}$
$V_{G3} = 2.1\,\text{V}$
$V_{omax} = 2.9\,\text{V}$
$R_o = 2.5\,\text{M}\Omega$

Q10. For $V_{DD} = 1.8\,\text{V}$ and using $I_{ref} = 100\,\mu\text{A}$, it is required to design the circuit of Fig. 3 to obtain an output current whose nominal value is $100\,\mu\text{A}$. Find R if M_1 and M_2 are matched with channel lengths of 500 nm, channel widths of $4\,\mu\text{m}$, $V_t = 0.5\,\text{V}$, and $k'_n = 400\,\mu\text{A/V}^2$. What is the lowest possible value for V_o? Assuming that for this process technology the Early voltage is $V'_A = 10\,\text{V}/\mu\text{m}$, find the output resistance of the current source. Also, find the current change in output current resulting from a $+0.5\,\text{V}$ change in V_o

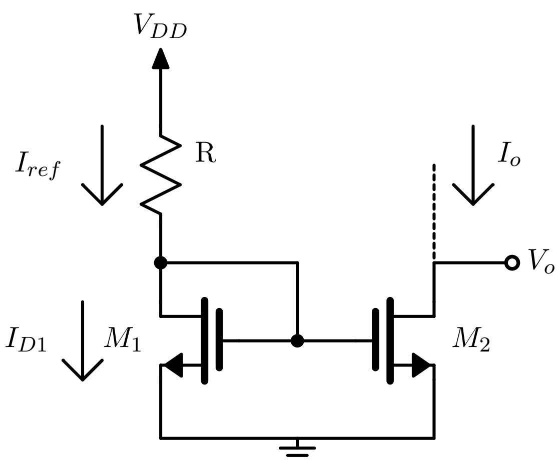


Figure 3: NMOS current mirror

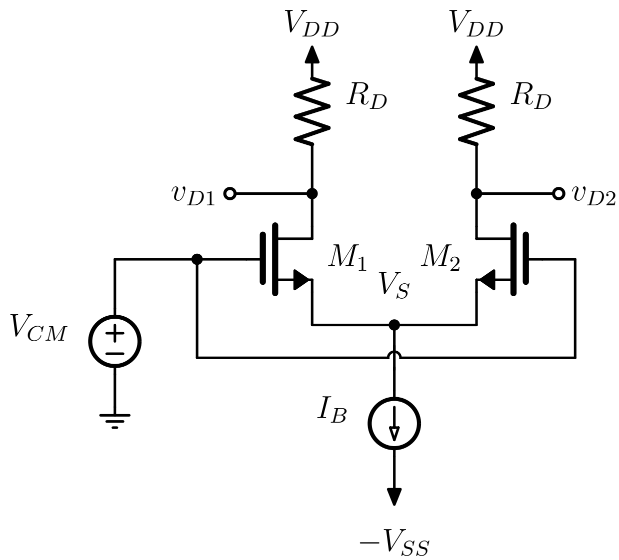
Solution

$I_o = I_{ref} = \frac{1}{2}k'_n(W/L)V_{ov}^2 \Rightarrow$
$V_{ov} = \sqrt{2 * I_o/(k'_n * (W/L))} = \sqrt{2*(100e-6)/((400e-6)*((4e-6)/(500e-9)))} = 0.25\,\text{V}$
$V_{DS} = V_{GS} = V_t + V_{ov} = (0.5) + (0.25) = 0.75\,\text{V}$
$R = (V_{DD} - V_{GS})/I_{ref} = ((1.8) - (0.75))/(100e-6) = 10.5\,\text{k}\Omega$
$R = 10.5\,\text{k}\Omega$
The lowest V_o will be when
$V_{DS2min} = V_{ov} = 0.25\,\text{V}$
$r_o = V'_A * L/I_o = (10e6)*(500e-9)/(100e-6) = 50\,\text{k}\Omega$
$r_o = 50\,\text{k}\Omega$
$\Delta I_D = \Delta V_o/r_o = (0.5)/(50e3) = 10\,\mu\text{A}$
$\Delta I_D = 10\,\mu\text{A}$

Answers

$R = 10.5\,\mathrm{k\Omega}$
$V_{DS2min} = 0.25\,\mathrm{V}$
$r_o = 50\,\mathrm{k\Omega}$
$\Delta I_D = 10\,\mu\mathrm{A}$

Q11. Consider the NMOS diff pair shown below with a common-mode input, V_{CM} and $V_{DD} = 1\,\mathrm{V}$, $V_{SS} = 1.1\,\mathrm{V}$, $\mu_n C_{ox} = 400\,\mu\mathrm{A/V^2}$, $(W/L)_{1,2} = 12.5$, $V_{tn} = 0.4\,\mathrm{V}$, $I_B = 200\,\mu\mathrm{A}$, $R_D = 5\,\mathrm{k\Omega}$. In addition, the minimum voltage required across I_B is $0.2\,\mathrm{V}$ so that the current source transistor creating I_B does not leave the active region. Ignore channel length modulation.



(a) For $V_{CM} = 0.1\,\mathrm{V}$, find V_{ov1}, V_{GS1}, V_S, I_{D1} and V_{D1}
(b) What is the highest value for V_{CM} such than no transistors leave the active region?
(c) What is the lowest value for V_{CM} such than no transistors leave the active region?

Solution
(a) $I_{D1} = I_B/2 = (200e-6)/2 = 100\,\mu\mathrm{A}$ and using the active equation $I_D = (\mu_n C_{ox}/2)(W/L)(V_{ov})^2$, we have

$V_{ov1} = \sqrt{(2*I_{D1})/(\mu_n C_{ox}*(W/L)_{1,2})} = \sqrt{(2*(100e-6))/((400e-6)*(12.5))} = 0.2\,\mathrm{V}$

$V_{GS1} = V_{ov1} + V_{tn} = (0.2) + (0.4) = 0.6\,\mathrm{V}$

$V_S = V_{CM} - V_{GS1} = (0.1) - (0.6) = -0.5\,\mathrm{V}$

$V_{D1} = V_{DD} - I_{D1} * R_D = (1) - (100e-6) * (5e3) = 0.5\,\mathrm{V}$

(b) As V_{CM} increases, the current through M_1 remains constant so V_{D1} remains at $0.5\,\mathrm{V}$. M_1 will go into triode when the drain of M_1 is one threshold below the gate of M_1, so the max gate voltage is
$V_{CM,max} = V_{D1} + V_{tn} = (0.5) + (0.4) = 0.9\,\mathrm{V}$

(c) We are given $V_{CS,min} = 0.2\,\mathrm{V}$ as the minimum voltage required across the current source, I_B. As V_{CM} decreases, V_S decreases with it and when V_S goes too low, the current source I_B will leave the active region. This occurs at
$V_{CM,min} = -1 * V_{SS} + V_{CS,min} + V_{GS1} = -1*(1.1) + (0.2) + (0.6) = -0.3\,\mathrm{V}$