11.1 A class A emitter follower, biased using the circuit shown in Fig. 11.2, uses $V_{CC} = 5$ V, $R = R_L = 1$ kΩ, with all transistors (including Q_3) identical. Assume $V_{BE} = 0.7$ V, $V_{CEsat} = 0.3$ V, and β to be very large. For linear operation, what are the upper and lower limits of output voltage, and the corresponding inputs? How do these values change if the emitter–base junction area of Q_3 is made twice as big as that of Q_2? Half as big?

11.2 A source-follower circuit using NMOS transistors is constructed following the pattern shown in Fig. 11.2. All three transistors used are identical, with $V_t = 1$ V and $\mu_n C_{ox} W/L = 20$ mA/V^2; $V_{CC} = 5$ V, $R = R_L = 1$ kΩ. For linear operation, what are the upper and lower limits of the output voltage, and the corresponding inputs?

D 11.3 Using the follower configuration shown in Fig. 11.2 with ±9-V supplies, provide a design capable of ±7-V outputs with a 1-kΩ load, using the smallest possible total supply current. You are provided with four identical, high-β BJTs and a resistor of your choice.

D 11.4 An emitter follower using the circuit of Fig. 11.2, for which the output voltage range is ±5 V, is required using $V_{CC} = 10$ V. The circuit is to be designed such that the current variation in the emitter-follower transistor is no greater than a factor of 10, for load resistances as low as 100 Ω. What is the value of R required? Find the incremental voltage gain of the resulting follower at $v_O = +5$, 0, and –5 V, with a 100-Ω load. What is the percentage change in gain over this range of v_O?

11.11 Consider the complementary-BJT class B output stage and neglect the effects of finite V_{BE} and V_{CEsat}. For ±10-V power supplies and a 100-Ω load resistance, what is the maximum sine-wave output power available? What supply power corresponds? What is the power-conversion efficiency? For output signals of half this amplitude, find the output power, the supply power, and the power-conversion efficiency.

D 11.12 A class B output stage operates from ±5-V supplies. Assuming relatively ideal transistors, what is the output voltage for maximum power-conversion efficiency? What is the output voltage for maximum device dissipation? If each of the output devices is individually rated for 1-W dissipation, and a factor-of-2 safety margin is to be used, what is the smallest value of load resistance that can be tolerated, if operation is always at full output voltage? If operation is allowed at half the full output voltage, what is the smallest load permitted? What is the greatest possible output power available in each case?

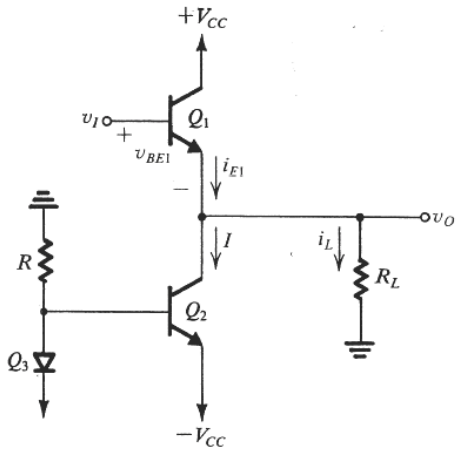

Fig. 11.2

D 11.13 A class B output stage is required to deliver an average power of 100 W into a 16-Ω load. The power supply should be 4 V greater than the corresponding peak sine-wave output voltage. Determine the power-supply voltage required (to the nearest volt in the appropriate direction), the peak current from each supply, the total supply power, and the power-conversion efficiency. Also, determine the maximum possible power dissipation in each transistor for a sine-wave input.