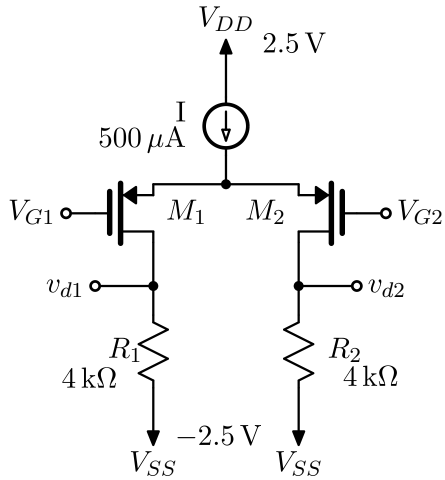
Problem Set 4

Q1. Consider the PMOS differential amplifier shown below let $V_{tp} = -0.8\,\text{V}$ and $k_p' W/L = 4\,\text{mA/V}^2$. Neglect channel-length modulation.



(a) For $V_{G1} = V_{G2} = 0V$, find V_{ov} and V_{GS} for each of M1 and M2. Also find V_S, V_{D1}, and V_{D2}.

(b) If the current source requires a minimum voltage of 0.5V, find the input common-mode range.

Solution

(a) $|V_{ov}| = \sqrt{I/(k_p' W/L)} = \sqrt{(500e-6)/((4e-3))} = 0.3536\,\text{V}$

$|V_{ov}| = 0.3536\,\text{V}$

$|V_{GS}| = |V_{tp}| + |V_{ov}| = |(-0.8)| + (0.3536) = 1.154\,\text{V}$

$|V_{GS}| = 1.154\,\text{V}$

$V_S = V_G + |V_{GS}| = (0) + (0)S = 1.154\,\text{V}$

$V_S = 1.154\,\text{V}$

$V_{D1} = -2.5 + I/2 * R = -2.5 + (500e-6)/2 * (4e3) = -1.5\,\text{V}$

$V_{D2} = V_{D1} = -1.5\,\text{V}$

(b) Current source requires $0.5V$.

$V_{CMmax} = V_{DD} - 0.5 - |V_{GS}| = (2.5) - 0.5 - (1.154) = 0.8464\,\text{V}$

$V_{CMmax} = 0.8464\,\text{V}$

$V_{CMmin} = V_{D1} + V_{tp} = (-1.5) + (-0.8) = -2.3\,\text{V}$

$V_{CMmin} = -2.3\,\text{V}$

Answers

(a) $|V_{ov}| = 0.3536\,\text{V}$

$|V_{GS}| = 1.154\,\text{V}$

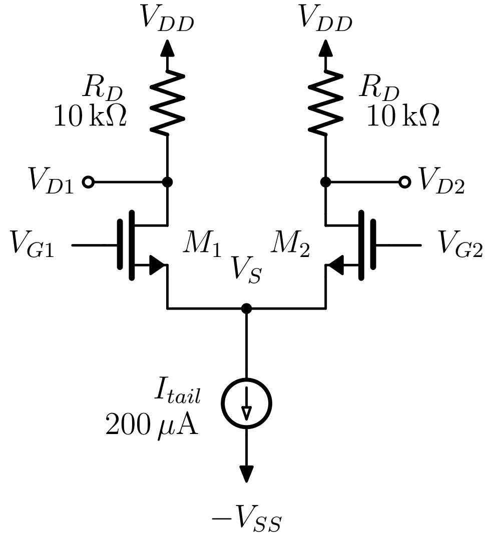
$V_S = 1.154\,\text{V}$

$V_{D2} = V_{D1} = -1.5\,\text{V}$

(b) $V_{CMmax} = 0.8464\,\text{V}$

$V_{CMmin} = -2.3\,\text{V}$

Q2. Consider the differential amp below and let the two inputs $V_{G2} = 0\,\text{V}$ and $V_{G1} = v_{id}$. For each case below, find $v_{id}, V_s, V_{D1}, V_{D2}$ and $V_{D2} - V_{D1}$



$\mu_n C_{ox} = 400\,\mu\text{A/V}^2$
$W/L = 12.5$
$V_t = 0.5\,\text{V}$
$V_{DD} = 1\,\text{V}$
$V_{SS} = 1\,\text{V}$

a) $I_{D1} = I_{D2} = 100\,\mu\text{A}$
b) $I_{D1} = 150\,\mu\text{A}$ and $I_{D2} = 50\,\mu\text{A}$
c) $I_{D1} = 200\,\mu\text{A}$ and $I_{D2} = 0\,\text{A}$
d) $I_{D1} = 50\,\mu\text{A}$ and $I_{D2} = 150\,\mu\text{A}$
e) $I_{D1} = 0\,\text{A}$ and $I_{D2} = 200\,\mu\text{A}$

You can make the assumption that $v_{id}/2 \ll V_{ov}$

Solution

a)
When the differential pair is balanced, we can calculate the overdrive voltage, in equilibrium:
$V_{ov} = \sqrt{(2 * I_{D1})/(\mu_n C_{ox} * W/L)} = \sqrt{(2 * (100e-6))/((400e-6) * (12.5))} = 0.2\,\text{V}$
$V_{GS} = V_{ov} + V_t = (0.2) + (0.5) = 0.7\,\text{V}$
$V_S = V_{G2} - V_{GS} = (0) - (0.7) = -0.7\,\text{V}$
$V_{D1} = V_{DD} - I_{D1} * R_D = (1) - (100e-6) * (10e3) = 0\,\text{V}$
$V_{D2} = V_{D1} = (0) = 0\,\text{V}$
$V_{D2} - V_{D1} = 0\text{V}$

b)
Using the large signal equation for the current in a diff pair
$i_{D1} = (I/2) + (I/V_{ov})(v_{id}/2)(1 - (v_{id}/2V_{ov})^2)^{1/2}$
we can ignore the square-root term since we assume $v_{id}/2 \ll V_{ov}$ resulting in
$I_{D1} = \frac{I_{tail}}{2} + \frac{I_{tail}}{V_{OV}}\frac{v_{id}}{2}$, then
$v_{id} = (2 * I_{D1}/I_{tail} - 1) * V_{ov} = (2 * (150e-6)/(200e-6) - 1) * (0.2) = 0.1\,\text{V}$
$V_{GS1} = \sqrt{(2 * I_{D1})/(\mu_n C_{ox} * W/L)} + V_t = \sqrt{(2 * (150e-6))/((400e-6) * (12.5))} + (0.5) = 0.7449\,\text{V}$
$V_{G1} = v_{id} = (0.1) = 0.1\,\text{V}$
$V_S = V_{G1} - V_{GS1} = (0.1) - (0.7449) = -0.6449\,\text{V}$
$V_{D1} = V_{DD} - I_{D1} * R_D = (1) - (150e-6) * (10e3) = -0.5\,\text{V}$
$V_{D2} = V_{DD} - I_{D2} * R_D = (1) - (50e-6) * (10e3) = 0.5\,\text{V}$
$V_{D2} - V_{D1} = 1\text{V}$

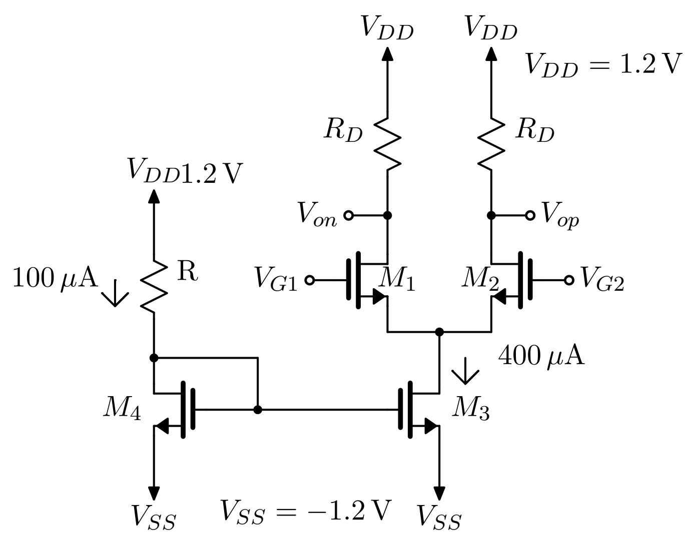
c)
$v_{id} = \sqrt{2} * V_{ov} = \sqrt{2} * (0.2) = 0.2828\,\text{V}$
$V_{G1} = v_{id} = (0.2828) = 0.2828\,\text{V}$

$V_{GS1} = \sqrt{(2*I_{D1})/(\mu_n C_{ox}*W/L)} + V_t = \sqrt{(2*(200e-6))/((400e-6)*(12.5))} + (0.5) = 0.7828\,\text{V}$
$V_S = V_{G1} - V_{GS1} = (0.2828) - (0.7828) = -0.5\,\text{V}$
$V_{D1} = V_{DD} - I_{D1}*R_D = (1) - (200e-6)*(10e3) = -1\,\text{V}$
$V_{D2} = V_{DD} - I_{D2}*R_D = (1) - (0)*(10e3) = 1\,\text{V}$
$V_{D2} - V_{D1}$ =2V

d)
$v_{id} = (2*I_{D1}/I_{tail} - 1)*V_{ov} = (2*(50e-6)/(200e-6) - 1)*(0.2) = -0.1\,\text{V}$
$V_{GS1} = \sqrt{(2*I_{D1})/(\mu_n C_{ox}*W/L)} + V_t = \sqrt{(2*(50e-6))/((400e-6)*(12.5))} + (0.5) = 0.6414\,\text{V}$
$V_{G1} = v_{id} = (-0.1) = -0.1\,\text{V}$
$V_S = V_{G1} - V_{GS1} = (-0.1) - (0.6414) = -0.7414\,\text{V}$
$V_{D1} = V_{DD} - I_{D1}*R_D = (1) - (50e-6)*(10e3) = 0.5\,\text{V}$
$V_{D2} = V_{DD} - I_{D2}*R_D = (1) - (150e-6)*(10e3) = -0.5\,\text{V}$
$V_{D2} - V_{D1}$ =-1V

e)
$v_{id} = -1*\sqrt{2}*V_{ov} = -1*\sqrt{2}*(0.2) = -0.2828\,\text{V}$
$V_{G1} = v_{id} = (-0.2828) = -0.2828\,\text{V}$
$V_{GS1} = \sqrt{(2*I_{D1})/(\mu_n C_{ox}*W/L)} + V_t = \sqrt{(2*(0))/((400e-6)*(12.5))} + (0.5) = 0.5\,\text{V}$
$V_S = V_{G1} - V_{GS1} = (-0.2828) - (0.5) = -0.7828\,\text{V}$
$V_{D1} = V_{DD} - I_{D1}*R_D = (1) - (0)*(10e3) = 1\,\text{V}$
$V_{D2} = V_{DD} - I_{D2}*R_D = (1) - (200e-6)*(10e3) = -1\,\text{V}$
$V_{D2} - V_{D1}$ =-2V

Q3. Design the circuit below to obtain a dc voltage of +0.2 V at each of the drains of M1 and M2 when $V_{G1} = V_{G2} = 0V$. Operate all transistors at $V_{ov} = 0.2\,\text{V}$ and assume that for the process technology in which the circuit is fabricated, $V_{tn} = 0.5\,\text{V}$ and $\mu_n C_{ox} = 250\,\mu\text{A/V}^2$. Neglect channel-length modulation. Determine the values of R, R_D, and the W/L ratios of M1, M2, M3, and M4. What is the input common-mode voltage range for your design?



Solution

$V_{GS} = V_{tn} + V_{ov} = (0.5) + (0.2) = 0.7\,\text{V}$

$V_{G4} = V_{D4} = V_{SS} + V_{GS} = (-1.2) + (0.7) = -0.5\,\mathrm{V}$
$R = (V_{DD} - V_{D4})/I_{bias} = ((1.2) - (-0.5))/(100e-6) = 17\,\mathrm{k\Omega}$
$R = 17\,\mathrm{k\Omega}$
$R_D = (V_{DD} - V_D)/(I_{tail}/2) = ((1.2) - (0.2))/((400e-6)/2) = 5\,\mathrm{k\Omega}$
$R_D = 5\,\mathrm{k\Omega}$

$I_{D1} = I_{tail}/2 = 1/2\mu_n C_{ox}(W/L)_1 V_{ov}^2 \Rightarrow$
$(W/L)_1 = I_{tail}/(\mu_n C_{ox} * V_{ov}^2) = (400e-6)/((250e-6) * (0.2)^2) = 40$
$(W/L)_2 = (W/L)_1 = 40$
$(W/L)_3 = 2 * I_{tail}/(\mu_n C_{ox} * V_{ov}^2) = 2 * (400e-6)/((250e-6) * (0.2)^2) = 80$
$(W/L)_3 = 80$
$(W/L)_4 = 2 * I_{bias}/(\mu_n C_{ox} * V_{ov}^2) = 2 * (100e-6)/((250e-6) * (0.2)^2) = 20$
$(W/L)_4 = 20$
$V_{CMmax} = V_{tn} + V_{DD} - I_{tail}/2 * R_D = (0.5) + (1.2) - (400e-6)/2 * (5e3) = 0.7\,\mathrm{V}$
$V_{CMmax} = 0.7\,\mathrm{V}$
$V_{CMmin} = V_{SS} + V_{ov3} + V_{tn} + V_{ov1} = (-1.2) + (0.2) + (0.5) + (0.2) = -0.3\,\mathrm{V}$
$V_{CMmin} = -0.3\,\mathrm{V}$

Answers

$R = 17\,\mathrm{k\Omega}$
$R_D = 5\,\mathrm{k\Omega}$
$(W/L)_2 = (W/L)_1 = 40$
$(W/L)_3 = 80$
$(W/L)_4 = 20$
$V_{CMmax} = 0.7\,\mathrm{V}$
$V_{CMmin} = -0.3\,\mathrm{V}$

Q4. An NMOS differential amplifier has a bias current of $I = 400\,\mu\mathrm{A}$. The transistors have $V_t = 0.5\,\mathrm{V}$, $W = 20\,\mu\mathrm{m}$, $L = 500\,\mathrm{nm}$ and $k_n' = 200\,\mu\mathrm{A/V^2}$.
a) Determine V_{GS} and g_m in equilibrium state.
b) Determine v_{ID} for full-current switching.
c) How should the bias current be adjuste such that the value v_{ID} is doubled for full-current switching?

Solution

a) First, V_{GS} will be determined:
$I_D = \frac{k_n'}{2}\frac{W}{L}V_{ov}^2$
Rearanging we get:
$V_{GS} = \sqrt{2 * (I/2)/k_n' * (L/W)} + V_t = \sqrt{2 * ((400e-6)/2)/(200e-6) * ((500e-9)/(20e-6))} + (0.5) = 0.7236\,\mathrm{V}$
$V_{GS} = 0.7236\,\mathrm{V}$

Then calculating g_m:
$g_m = 2 * (I/2)/(V_{GS} - V_t) = 2 * ((400e-6)/2)/((0.7236) - (0.5)) = 1.789\,\mathrm{mA/V}$
$g_m = 1.789\,\mathrm{mA/V}$

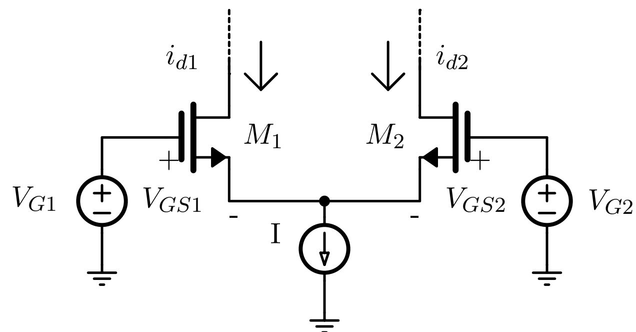
b) Second, v_{ID} is determined: $v_{ID} = \sqrt{2} * (V_{GS} - V_t) = \sqrt{2} * ((0.7236) - (0.5)) = 0.3162\,\mathrm{V}$
$v_{ID} = 0.3162\,\mathrm{V}$

c) Do double v_{ID}, we need to double V_{ov}.
However since $I_D = \frac{k_n'}{2}\frac{W}{L}V_{ov}^2$, I_D is quadrupled.
$I_2 = 4 * I = 4 * (400e - 6) = 1.6\,\mathrm{mA}$
$I_2 = 1.6\,\mathrm{mA}$

Answer

$V_{GS} = 0.7236\,\mathrm{V}$; $g_m = 1.789\,\mathrm{mA/V}$; $v_{ID} = 0.3162\,\mathrm{V}$; $I_2 = 1.6\,\mathrm{mA}$

Q5. Design the the MOS differential amplifier below to operate at $V_{ov} = 0.25\,\mathrm{V}$ and to provide a transconductance g_m of $1\,\mathrm{mA/V}$. Specify the W/L ratios and the bias current. The technology available provides $V_t = 0.8\,\mathrm{V}$ and $\mu_n C_{ox} = 100\,\mu\mathrm{A/V}^2$.



Solution

$I = g_m * V_{ov} = (1e - 3) * (0.25) = 250\,\mu\mathrm{A}$
$I = 250\,\mu\mathrm{A}$
$I_D = I/2 = \frac{1}{2}\mu_n C_{ox} W/L V_{ov}^2$
$W/L = I/(\mu_n C_{ox} * V_{ov}^2) = 40\,\Omega$
$W/L = 40\,\Omega$

Answers

$I = 250\,\mu\mathrm{A}$
$W/L = 40\,\Omega$

Q6. It is required to design an NMOS differential amplifier to operate with a differential input voltage that can be as high as $v_{id} = 0.1\,\mathrm{V}$ while keeping the nonlinear term under the square root in Eq. (1) to a maximum of 50e-3. A transconductance $g_m = 1\,\mathrm{mA/V}$ is needed. Find the required values of V_{ov}, I, W/L. Assume that the technology available has $\mu_n Cox = 200\,\mu\mathrm{A/V}^2$. What differential gain A_d results when $R_D = 10\,\mathrm{k\Omega}$? Assume $\lambda = 0$. What is the resulting output signal corresponding to v_{id} at its maximum value?

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{ov}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2} \tag{1}$$

Solution We assume that

$$\left(\frac{v_{id}/2}{V_{ov}}\right)^2 = 50e-3 \quad (2)$$

Then

$$V_{ov} = \frac{v_{id}/2}{\sqrt{50e-3}} = 0.2236 \quad (3)$$

Having $g_m = 1\,\text{mA/V}$, $V_{ov} = 0.2236\,\text{V}$, and the relation $g_m = I/V_{ov}$, it is possible to find:
a) the current:
$I = g_m * V_{ov} = (1e-3)*(0.2236) = 223.6\,\mu\text{A}$
b) the differential gain:
$A_d = g_m * R_D = (1e-3)*(10e3) = 10\,\text{V/V}$
c) the output swing at maximum v_{id}
$V_{od} = A_d * v_{id} = (10)*(0.1) = 1\,\text{V}$
d) the transistor aspect ratio:
$W/L = I/(\mu_n Cox * V_{ov}^2) = (223.6e-6)/((200e-6)*(0.2236)^2) = 22.36$

Q7. Design a differential amplifier to operate with a supplies of $\pm 1V$ and which dissipates no more than $P = 2\,\text{mW}$ in its equilibrium state. Select V_{ov} such that the differential voltage required to steer current from one-side to the other is $v_{iv} = 0.4\,\text{V}$. Assume the differential voltage gain is $A_d = 5\,\text{V/V}$ and $k_n' = 400\,\mu\text{A/V}^2$. You can ignore the Early effect. Specify I, R_D, and W/L.

Solution

First, the bias current can be determined:
$I = P/(1-(-1)) = (2e-3)/(1-(-1)) = 1\,\text{mA}$
$I = 1\,\text{mA}$

Second, the V_{ov} can be determined:
$v_{iv} = 2\sqrt{2}V_{ov}$
$V_{ov} = v_{iv}/(2*\sqrt{2}) = (0.4)/(2*\sqrt{2}) = 0.1414\,\text{V}$
$V_{ov} = 0.1414\,\text{V}$

Third, R_D can be calculated:
As we know: $g_m = 2 * V_{ov}/I_D$ where $I_D = I/2$ and $A_d = g_m * R_D$, so:
$R_D = A_d * V_{ov}/I = (5)*(0.1414)/(1e-3) = 707.1\,\Omega$
$R_D = 707.1\,\Omega$

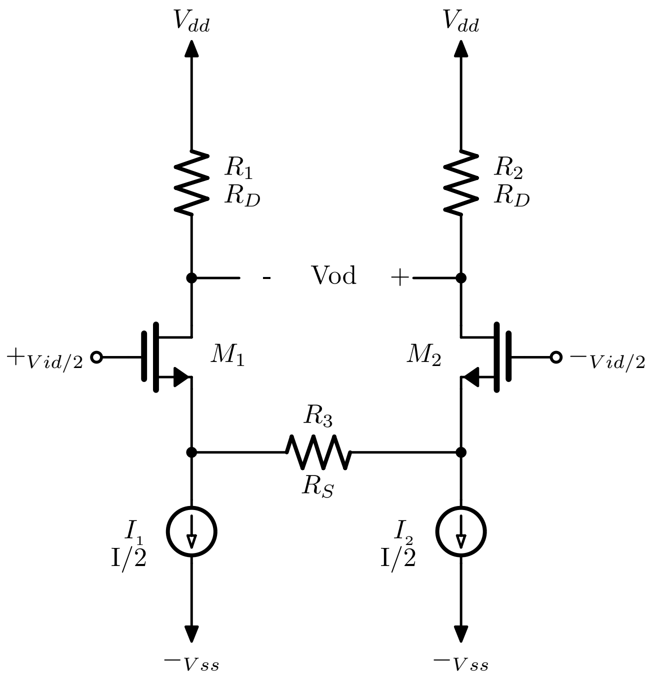
Finally, W/L can be calculated:
$W/L = I/(k_n' * V_{ov}^2) = (1e-3)/((400e-6)*(0.1414)^2) = 125$
$W/L = 125$

Answer

$I = 1\,\text{mA}$; $V_{ov} = 0.1414\,\text{V}$; $R_D = 707.1\,\Omega$; $W/L = 125$;

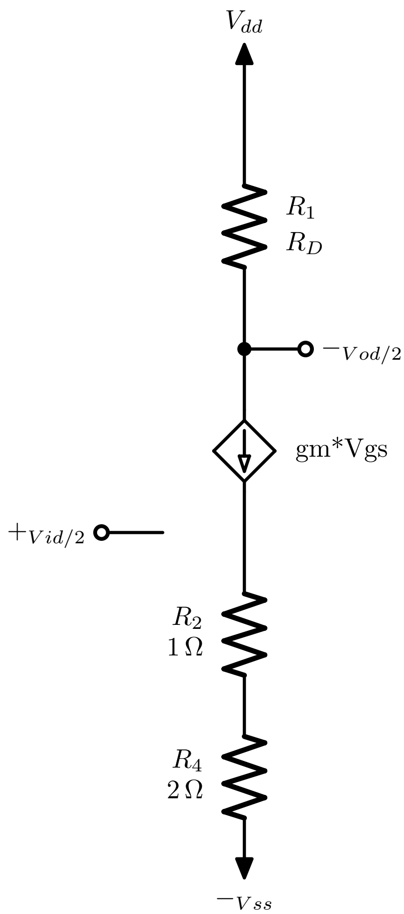
Q8. a) Draw the differential half-circuit for the amplifier below.
b) Derive an expression for the differential gain $A_d = V_{od}/V_{id}$ in terms of g_m, R_D, and R_S (ignore the Early effect).
c) What is the gain if $R_S = 0$?

d) What is the value of R_S in terms of $1/g_m$ that reduces the gain to half this value?



Solution

a) The differential half-circuit is as shown:



b) Calculating the differential current:
$I_D = (v_{id}/2)/(1/g_m + R_S/2)$
Converting current to voltage:
$v_{od}/2 = I_D * R_D$
$v_{od} = -v_{id}/(1/g_m + R_S/2) * R_D$
$A_v = v_{od}/v_{id} = -R_D/(1/g_m + R_S/2) = -g_m * R_D/(1 + R_S * g_m/2)$

c) Substituting 0 for R_S, we get:
$A_v = -g_m * R_D$

d) We want the denominator to be 2, therefore:
$1 + g_m * R_S/2 = 2$
$g_m * R_S = 2$

Answer

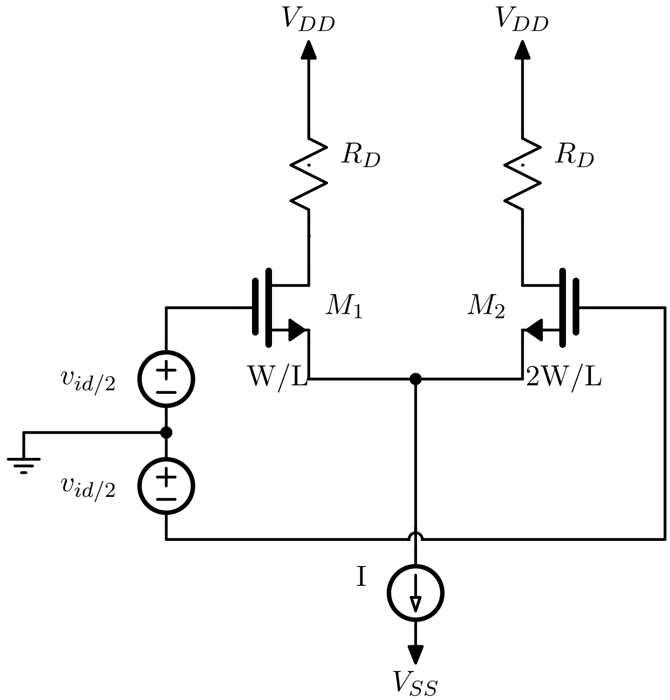
$A_v - g_m * R_D/(1 + R_S * g_m/2)$; $A_v = -g_m * R_D$; $g_m * R_S = 2$

Q9. A design error has resulted in a gross mismatch in the circuit shown below. Specifically, M2 has twice the W/L ratio of M1. If v_{id} is a small sine-wave signal, find:

(a) I_{D1} and I_{D2}.

(b) V_{ov} for each M1 and M2.

(c) The differential gain A_d in terms of R_D, I, and V_{ov}.



Solution

(a) $I_{D1} = \frac{1}{2}k_n' \frac{W}{L}(V_{GS1} - V_t)^2$
$I_{D2} = \frac{1}{2}k_n' \frac{2W}{L}(V_{GS1} - V_t)^2$
Since $V_{GS1} - V_t$ is equal for both transistors: $\Rightarrow \frac{I_{D1}}{I_{D2}} = \frac{1}{2}; I_{D2} = 2I_{D1}$
but $I = I_{D1} + I_{D2} = 3I_{D1}$
$I_{D1} = I/3$
$I_{D2} = 2I/3$

(b) $V_{ov} = V_{GS} - V_t$
$V_{ov1} = V_{ov2} = V_{ov}$
For M1: $\frac{I}{3} = \frac{1}{2}k_n'(W/L)V_{ov}^2$
$\Rightarrow V_{ov} = \sqrt{\frac{2}{3}\frac{I}{k_n'(W/L)}}$

(c) $g_m = \frac{2I_D}{V_{ov}} \Rightarrow g_{m1} = \frac{2I}{3V_{ov}}$
$g_{m2} = \frac{4I}{3V_{ov}}$
$v_{o1} = -g_{m1}\frac{v_{id}}{2}R_D = -\frac{2}{3}\frac{I}{V_{ov}}R_D v_{id}$
$v_{o2} = +g_{m2}\frac{v_{id}}{2}R_D = \frac{4}{3}\frac{I}{V_{ov}}R_D v_{id}$
$\Rightarrow \frac{v_{o2}-v_{o1}}{v_{id}} = \left(\frac{4}{3} + \frac{2}{3}\right)\frac{I}{V_{ov}}R_D$
$= 2\frac{I}{V_{ov}}R_D$

Q10. For the differential amplifier shown in Q2, let M1 and M2 have $k_p'(W/L) = 4\,\text{mA/V}^2$, and assume that the current source has an output resistance of $30\,\text{k}\Omega$. Find $|V_{ov}|$, g_m, $|A_d|$, $|A_{cm}|$, and the CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2 %.

Solution

$|V_{ov}| = \sqrt{I/k_p'(W/L)} = \sqrt{(500e-6)/(4e-3)} = 0.3536\,\text{V}$
$g_m = I/|V_{ov}| = (500e-6)/(0.3536) = 1.414\,\text{mA/V}$
$|A_d| = g_m * R_D = (1.414e-3)*(4e3) = 5.657\,\text{V/V}$
$|A_{cm}| = R_D/(2*R_{SS}) * mismatch = (4e3)/(2*(30e3))*(20e-3) = 1.333\,\text{mV/V}$
$CMRR = 20*log10(|A_d|/|A_{cm}|) = 20*log10((5.657)/(1.333e-3)) = 72.55\,\text{dB}$

Answers

$|V_{ov}| = 0.3536\,\text{V}$

$g_m = 1.414\,\text{mA/V}$

$|A_d| = 5.657\,\text{V/V}$

$|A_{cm}| = 1.333\,\text{mV/V}$

$CMRR = 72.55\,\text{dB}$

Q11. An NMOS differential pair operating at a bias current I of $100\,\mu$A uses transistors for which $k_n' = 250\,\mu\text{A/V}^2$ and $W/L = 10$. Find the three components of input offset voltage under the conditions that $\Delta R_D/R_D = 5\,\%$, $\Delta(W/L)/(W/L) = 5\,\%$, and $\Delta V_t = 5\,\text{mV}$. In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?

Solution

$I_D = I/2 = (100e-6)/2 = 50\,\mu\text{A}$
$V_{ov} = \sqrt{2*I_D/(k_n'*W/L)} = \sqrt{2*(50e-6)/((250e-6)*(10))} = 0.2\,\text{V}$
offset due to $\Delta R_D/R_D$:
$V_{OS1} = V_{ov}/2*\Delta R_D/R_D = (0.2)/2*(50e-3) = 5\,\text{mV}$
$V_{OS1} = 5\,\text{mV}$
offset due to $\Delta(W/L)/(W/L)$:
$V_{OS2} = V_{ov}/2*\Delta(W/L)/(W/L) = (0.2)/2*(50e-3) = 5\,\text{mV}$
$V_{OS2} = 5\,\text{mV}$
offset due to ΔV_t:
$V_{OS3} = \Delta V_t = (5e-3) = 5\,\text{mV}$
$V_{OS3} = 5\,\text{mV}$

Worst case offset is: $V_{OSmax} = V_{OS1} + V_{OS2} + V_{OS3} = (5e-3)+(5e-3)+(5e-3) = 15\,\text{mV}$
$V_{OSmax} = 15\,\text{mV}$
Typical offset is the root-sum-square value:
$V_{OStyp} = \sqrt{V_{OS1}^2 + V_{OS2}^2 + V_{OS3}^2} = \sqrt{(5e-3)^2 + (5e-3)^2 + (5e-3)^2} = 8.66\,\text{mV}$
$V_{OStyp} = 8.66\,\text{mV}$

Answers

$V_{OS1} = 5\,\text{mV}$

$V_{OS2} = 5\,\text{mV}$

$V_{OS3} = 5\,\text{mV}$
$V_{OSmax} = 15\,\text{mV}$
$V_{OStyp} = 8.66\,\text{mV}$

Q12. An active-loaded NMOS differential amplifier operates with a bias current of $I = 100\,\mu\text{A}$. The NMOS transistors are operated at $V_{ov} = 0.2\,\text{V}$ and the PMOS devices at $|V_{ov}| = 0.3\,\text{V}$. The Early voltages are 20 V for the NMOS and 12 V for the PMOS transistors. Find G_m, R_o, and A_d. For what value of load resistance is the gain reduced by a factor or 2?

Solution

Assuming a configuration similar to Fig. 8.32(a) of the textbook,
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_D = I/2 = (100e-6)/2 = 50\,\mu\text{A}$
$g_{m1} = g_{m2} = g_{mn} = I_D/(V_{ov}/2) = (50e-6)/((0.2)/2) = 500\,\mu\text{A/V}$
$G_m = g_{mn} = (500e-6) = 500\,\mu\text{A/V}$
$G_m = 500\,\mu\text{A/V}$
$r_{o1} = r_{o2} = r_{on} = V_{An}/I_D = (20)/(50e-6) = 400\,\text{k}\Omega$
$r_{o3} = r_{o4} = r_{op} = |V_{Ap}|/I_D = (12)/(50e-6) = 240\,\text{k}\Omega$
$R_o = r_{on}||r_{op} = (400e3)||(240e3) = 150\,\text{k}\Omega$
$R_o = 150\,\text{k}\Omega$
$A_d = G_m * R_o = (500e-6) * (150e3) = 75\,\text{V/V}$
$A_d = 75\,\text{V/V}$
Gain will be reduced by a factor of 2, if the load resistance equals R_o:
$R_L = R_o = (150e3) = 150\,\text{k}\Omega$

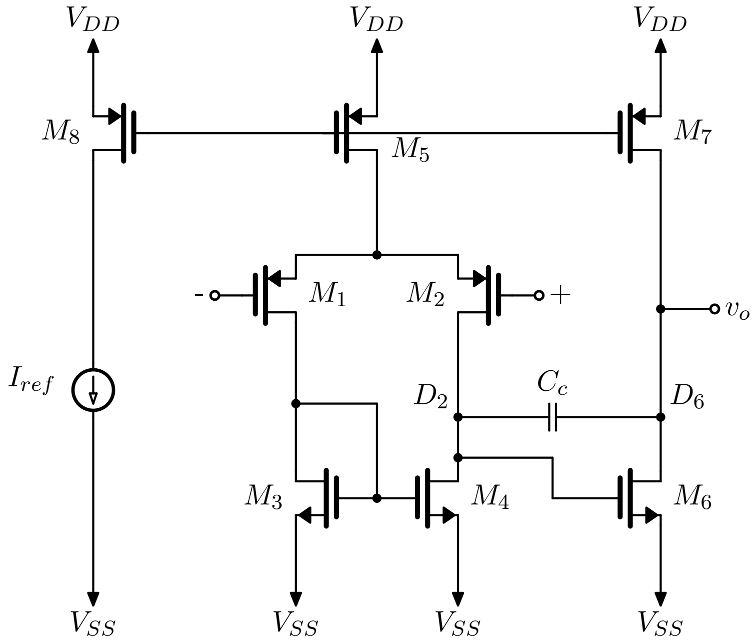
Answers

$G_m = 500\,\mu\text{A/V}$
$R_o = 150\,\text{k}\Omega$
$A_d = 75\,\text{V/V}$
Gain reduced by two when: $R_L = 150\,\text{k}\Omega$

Q13. Consider the input stage of the CMOS op amp below with both inputs grounded. Assume that the two sides of the input stage are perfectly matched except that the threshold voltages of M3 and M4 have a mismatch ΔV_t. Show that a current $g_{m3}\Delta V_t$ appears at the output of the first stage. What is the corresponding input offset voltage? Use the parameters given below:
$\Delta V_t = 2\,\text{mV}$, $I_{REF} = 90\,\mu\text{A}$, $V_{tn} = 0.7\,\text{V}$, $V_{tp} = -0.8\,\text{V}$, $\mu_n C_{ox} = 160\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 40\,\mu\text{A/V}^2$

Transistor	M1	M2	M3	M4	M5	M6	M7	M8
W	$20\,\mu$m	$20\,\mu$m	$5\,\mu$m	$5\,\mu$mm	$40\,\mu$m	$10\,\mu$m	$40\,\mu$m	$40\,\mu$m
L	800 nm	800 nm	800 nm	800 nm	800 nm	800 nm	800 nm	800 nm

Neglect Early voltage.



Solution

Offset current, $I_{OS} = I_{D2} - I_{D4} = I_{D3} - I_{D4}$
$I_{D3} = \frac{1}{2}\mu_n C_{ox}(W/L)_3(V_{GS3} - V_{tn})^2$
$I_{D4} = \frac{1}{2}\mu_n C_{ox}(W/L)_4(V_{GS4} - (V_{tn} + \Delta V_t))^2$
Since M3 and M4 have the same W/L:
$I_{OS} = I_{D3} - I_{D4}$
$= \frac{1}{2}\mu_n C_{ox}(W/L)[(V_{GS} - V_{tn} - V_{GS} + V_{tn} + \Delta V_t)\times$
$(V_{GS} - V_{tn} + V_{GS} - V_{tn} - \Delta V_t)]$
$\approx \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GS} - V_{tn})\Delta V_t$
$I_o = g_{m3}\Delta V_t$
Recall $I_o = G_{m1}V_{OS}$ and $G_{m1} = g_{m1}$
$\Rightarrow V_{OS} = \frac{g_{m3}}{g_{m1}}\Delta V_t$
$I_{D1} = (W/L)_5/(W/L)_8 * I_{REF}/2 = (50)/(50) * (90e-6)/2 = 45\,\mu\text{A}$
$g_{m1} = \sqrt{2 * \mu_p C_{ox} * (W/L)_1 * I_{D1}} = \sqrt{2 * (40e-6) * (25) * (45e-6)} = 300\,\mu\text{A/V}$
Since $I_{D3} = I_{D1} = (45e-6) = 45\,\mu\text{A}$:
$g_{m3} = \sqrt{2 * \mu_n C_{ox} * (W/L)_3 * I_{D1}} = \sqrt{2 * (160e-6) * (6.25) * (45e-6)} = 300\,\mu\text{A/V}$
For $\Delta V_t = 2\,\text{mV}$:
$V_{OS} = g_{m3}/g_{m1} * \Delta V_t = (300e-6)/(300e-6) * (2e-3) = 2\,\text{mV}$
$V_{OS} = 2\,\text{mV}$

Answers

$V_{OS} = 2\,\text{mV}$