Lab 2 NAND gate layout ECE334S

Objective:

The purpose of this lab is to get you familiar with MAX layout environment tools from Micromagic Inc. (www.micromagic.com). We will use MAX to layout a 2-input NAND gate, and to perform the DRC, extraction, LVS, and simulation of the NAND gate.

Preparation

P1) ***MAX Tutorial***

Read through the MAX tutorial before your lab session. This will help you finish your lab in time.

P2) Using coloured markers (or pencils), draw a layout for a two-input NAND gate shown in Figure 1 ignoring the actual design-rule values and not using metal2. (Metal2 is often reserved for longer routing in which case it is not used in circuit cells.) Verify your stick diagram using the layout shown in Figure 2.

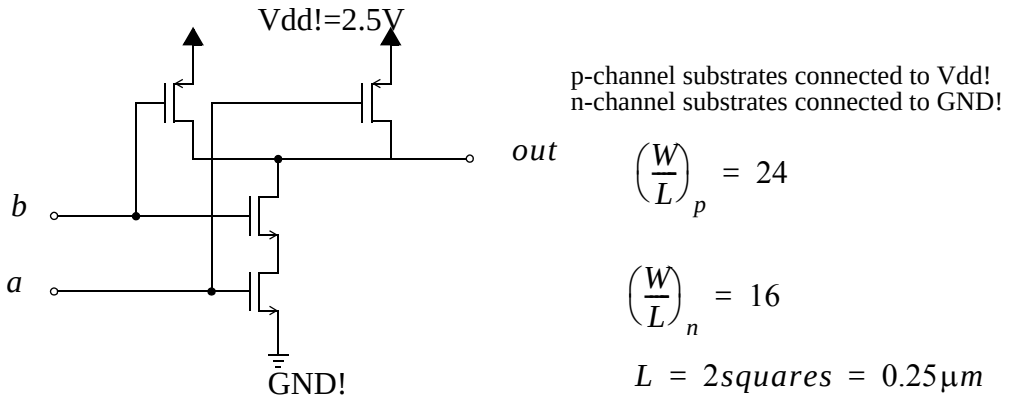

Figure 1: Schematic of 2-input NAND gate

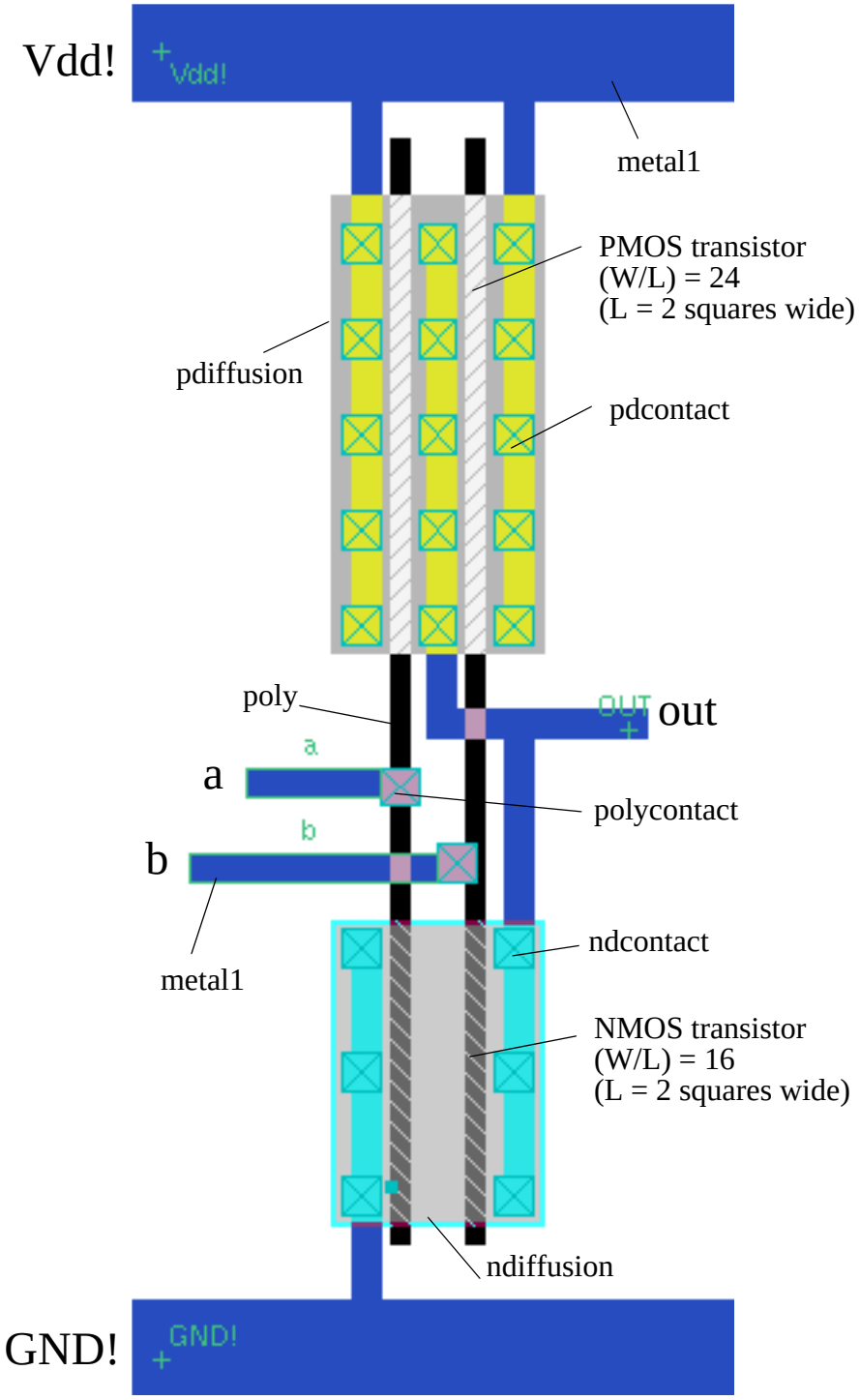

Figure 2: Layout of 2-input NAND gate.

Lab Work

L1) *MAX Tutorial*

1- Start MAX by typing “max”.

2- From the Help menu, select MAX tutorial.

3- Select MAX in the “Which Tutorial” field and click “ View Tutorial in Acroread.” Acrobat should start up with the SUE tutorial.

4- Start the tutorial on page 11 of the PDF (which is page 3 of the tutorial).

5- Follow the instructions and complete the tutorial with the following notes:

- Pages 3-45 do everything.

- Page 45-50: only read “Bigger Designs and Hierarchy”, as you will need it in later labs.

- Pages 50-end: skip the whole MAX_LS section.

Expected Results:

layout plot of the “NAND” cell on page 41.

L2) LAYOUT 2-INPUT NAND GATE

You must now create the layout for a 2-input NAND gate. Start the layout in a new Magic file

lab2.max

and use as your guide either your own layout stick diagram from the Preparation or the layout provided in Figure 2.

HINTS:

- You can re-use parts of the layout of the NAND gate done in L1), but make sure you use the correct transistor sizes.
- If dots appear in some areas in your layout, this is an indication that a design rule (or rules) has been violated. To check which rule was violated, place the box around the error area and type Shift-y or choose “Explain DRC under Box” from the Misc menu. Look for the list of DRC errors in the MAX command window (the window from which you started MAX). You must fix all drc errors.
- Make sure that you have drawn all necessary contacts between layers.
- Label all input, output and supply voltage terminals by selecting the corresponding layer

and typing “t”. The power supply and ground labels must be global (*Vdd!* and *GND*! respectively).

Expected Results:

layout plot of the 2-input NAND gate.

L3) EXTRACT & LVS THE LAYOUT

Doing extraction means obtaining the netlist of an electrical circuit from the layout images. This is done in order to perform circuit level simulation (for example using SPICE). Parasitic capacitances between layout layers should be included in the extracted circuit.
Once the layout is finished, do the extraction by clicking on “extract it” under the Local menu. Observe the messages in MAX command window, make sure you don’t get any error messages. If the extraction is successful, you will see the following message:
done.
Extraction may fail if there is an error in the layout (e.g. the drawn image does not form a transistor). The extractor will report errors and warnings by indicating the area of their occurrence.

LVS stands for layout-versus-schematic, which is used to compare the netlist of your extracted layout to the schematic. This check is used to make sure you have no mistakes in your layout, and it actually corresponds to your schematic.
To LVS your extracted layout you have to create a SUE schematic for the 2-input NAND gate with the same transistor dimensions.

HINTS:

- Make sure you add power, ground, input, and output ports with the same names as in your layout.
- The schematic file must have the same name as the layout file (*samename.sue*).

Following that, use MAX to perform the LVS by clicking on “SUE LVS” under the Tool menu. Observe the messages in MAX command window, if your layout is correct you should see the following message:
LVS is CLEAN!
done.
Now your layout corresponds to the schematic, save your layout and quit Magic.

L4) SIMULATE YOUR DESIGN

1- Run SUE and simulate your 2-input NAND gate. Apply Vdd to input “b” and apply a pulse to input “a” with a height 2.5 volts with rise and fall times of 200ps, a delay time of 0ns, a pulse width of 3ns, and a period of 6ns. Plot the input and output waveforms.

2- Although your schematic and layout correspond to each other, the layout contains physical dimensions. This enables us to estimate the parasitic capacitances associated with different nodes. So we can use the extracted layout to back annotate the parasitic capacitances to each node, and re-simulate the design. To do this, click on the "Back Annotate Caps" in the Sim menu in Sue, this will add the parasitic capacitors associated with each node. Now re-simulate the design with the parasitic capacitors and plot the output waveform. To compare it with the output waveform without parasitic capacitors, click on "Plot Old Net" in the "Sim" menu. Zoom in to see if they are different.

3- Add a 0.1pF load capacitor, and re-simulate. Plot the input and output waveforms, and measure the rise and fall times and the propagation delay of the circuit.

HINTS:

- An interesting feature in Micro-magic tools is cross probing; MAX highlights a net in the layout when you click on it in the schematic (SUE). To try this have both SUE and MAX running at the same time, open your schematic in SUE and the corresponding layout in MAX. Then click on "MAX Cross Probe Init" under "Sim" menu in SUE, a window will pop-up. You don't need to change anything, simply click done. Then click on any wire or node in the schematic and type "k" this will automatically highlight the node in MAX.

Expected Results:

Provide a print-out of the circuit diagram with parasitic capacitors, and a print-out of the required input and output waveforms.

Extra Notes:

- The following summarizes what you will need to demonstrate to your TAs in lab:

L1

- layout of the NAND cell on p. 41 of the MAX tutorial

L2

- layout of the 2-input NAND gate shown in Figure 1 (p. 1) of the lab handout

L4

- schematic of the 2-input NAND gate (Figure 1) with parasitic capacitors in SUE

- inputs and output waveforms (vs. time) plot before back annotating parasitic capacitors

- output waveform (vs. time) plot after back annotating parasitic capacitors

- input and output waveforms (vs. time) plot from the circuit with back-annotated capacitors and a 0.1 pF load capacitor

- measure the rise and fall times and the propagation delay from the above plot

Most Frequently Encountered Problems in Lab:

- In Figure 2 (p.2), please ignore the label "L = 2 squares wide", you don't need this information.

- Drawing the 2-input NAND gate layout in Figure 2, you don't have to match the number of contacts in transistors; only dimensions matters.

- To draw a contact between poly and metal1, you should start wiring from the poly. After dropping a contact, the layer will change to metal1 (refer to the section "Wiring Mode - Changing Layers" on p. 30 of the MAX tutorial).

- Although 0.18um CMOS technology is used in the MAX tutorial, you have to use 0.25um technology in this lab. This is indicated by the transistor length of the NAND gate in Figure 1. To start MAX with 0.25um technology, simply type 'max'.