.2 DIGITAL MOSFET CIRCUIT FAMILIES

1) STATIC CMOS

2) RATIOED CIRCUITS

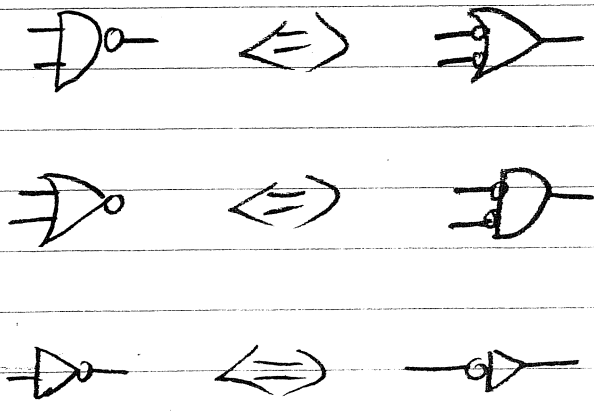
3) CASCODE VOLTAGE SWITCH LOGIC (CVSL)

4) DYNAMIC CIRCUITS

5) PASS TRANSISTOR CIRCUITS

STATIC CMOS

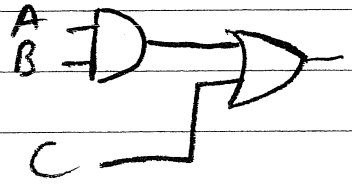
BUBBLE PUSHING (DEMORGAN'S LAW)



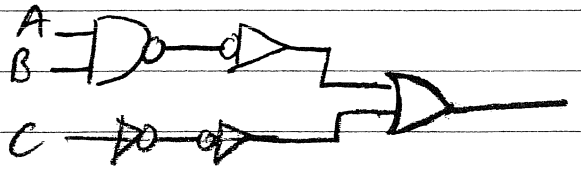
EX COMPUTE $F = AB + C$

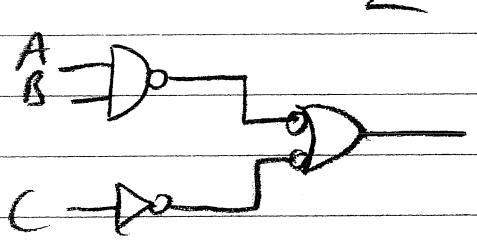
USING NANDS & NORS

START ANDS & ORS

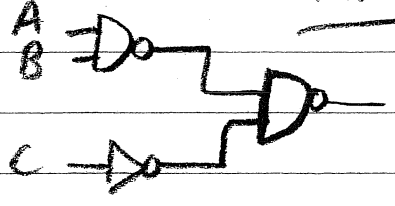


INSERT DOUBLE INVERSIONS



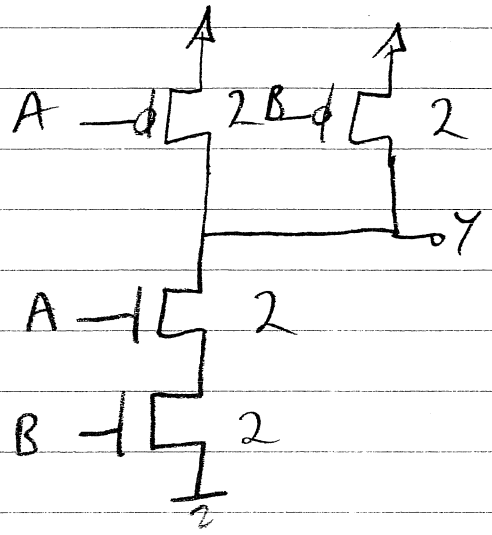


FINAL



PUSH BUBBLES

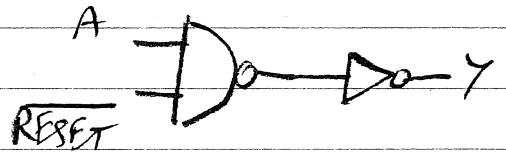
— INPUT ORDERING DELAY



DELAY FROM "A" TO "Y" LESS THAN "B" TO "Y"

A INPUT CAP = 4

ASYMMETRIC GATES

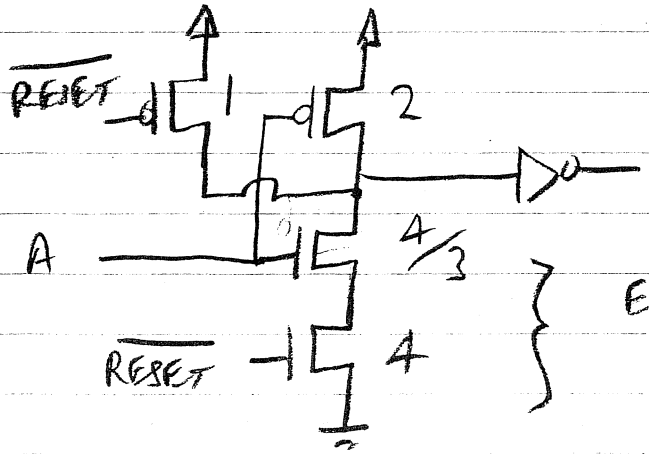


Y = A RESET = 0

Y = D RESET = 1

ASSUMING "A" TO "Y" DELAY CRITICAL

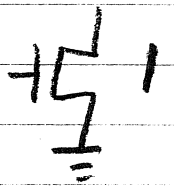
& $\overline{\text{RESET}}$ TO "Y" NOT CRITICAL AT ALL



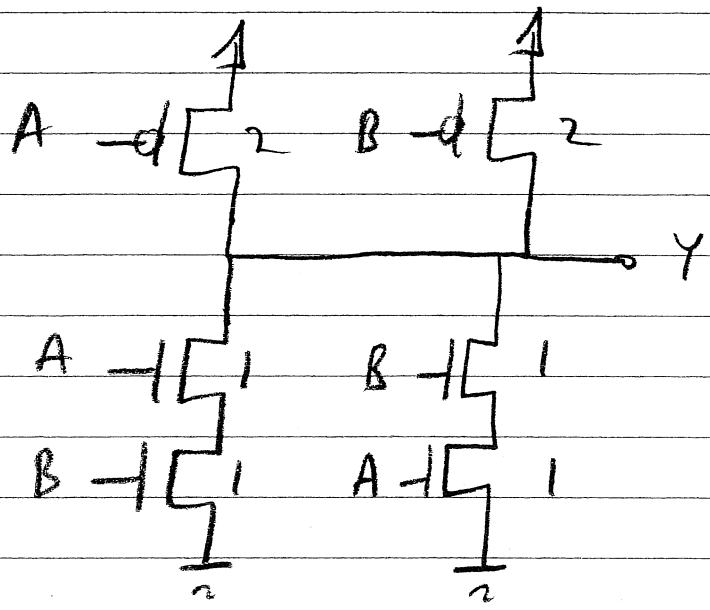
A INPUT CAP = $\frac{4}{3}+2$

$= 3\frac{1}{3}$

EQUIV TO



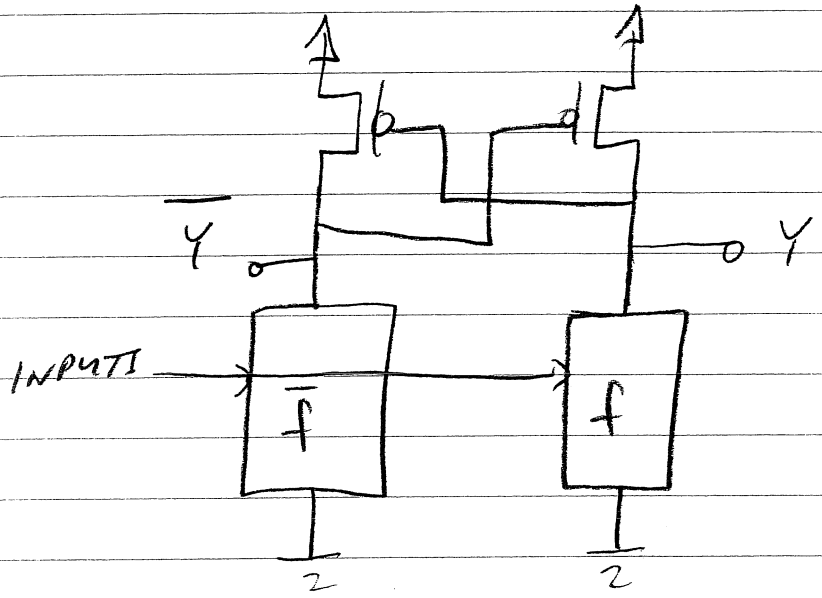
SYMMETRIC NAND



SAME DELAY FOR "A" AND "B" INPUTS

- RATIOD CIRCUITS (PREVIOUSLY DISCUSSED)
  - STATIC CURRENT DRAW
  - MAKE PULL-UP "SMALL" SO SMALL CURRENT DRAW WHEN OUTPUT LOW

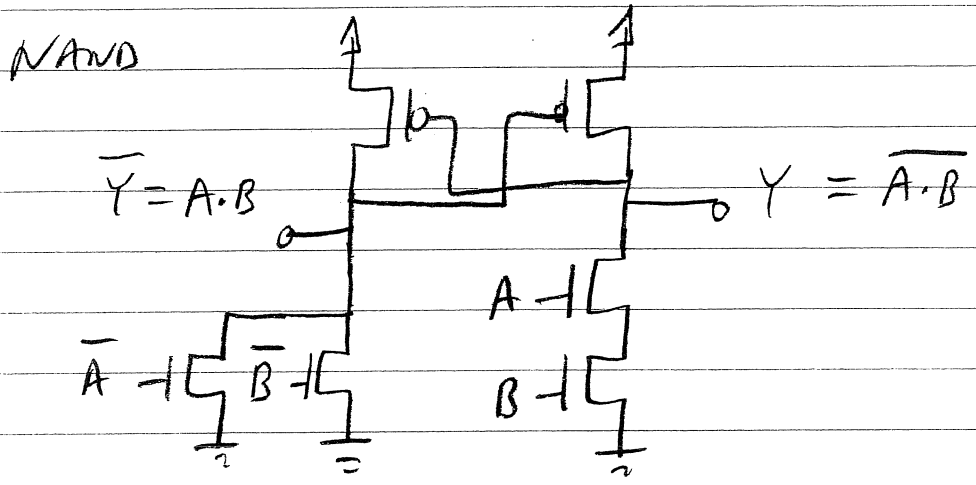
CVSL (CASCODE VOLTAGE SWITCH LOGIC)



GENERATES BOTH $Y + \bar{Y}$

- NO STATIC POWER

(RATIOED LOGIC)



- INTERESTING APPPROACH BUT PROCESS SENSITIVE MAKES SLOWER THAN CMOS

→ SLOW NMOS, FAST PMOS ⇒ MAKE PMOS SMALL SO NMOS CAN OVERCOME IT

SLOW PMOS ⇒ SLOW PULL-UP

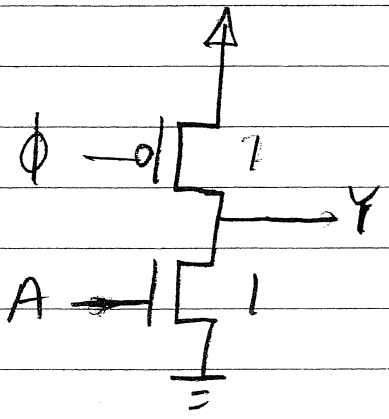
GENERALLY SLOWER THAN CMOS.

& MORE POWER HUNGRY

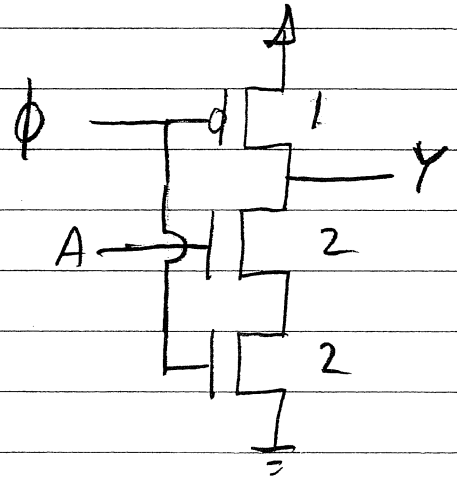
DYNAMIC CIRCUITS

- REQUIRES CLOCK ϕ TO OPERATE
- HAS PRECHARGE PHASE AND EVALUATION PHASE
- OUTPUT ONLY VALID DURING EVAL PHASE
- OUTPUT PRECHARGED TO V_{DD} DURING PRECHARGE PHASE
- FAST, NO STATIC POWER, HIGH DYNAMIC POWER

INVERTER

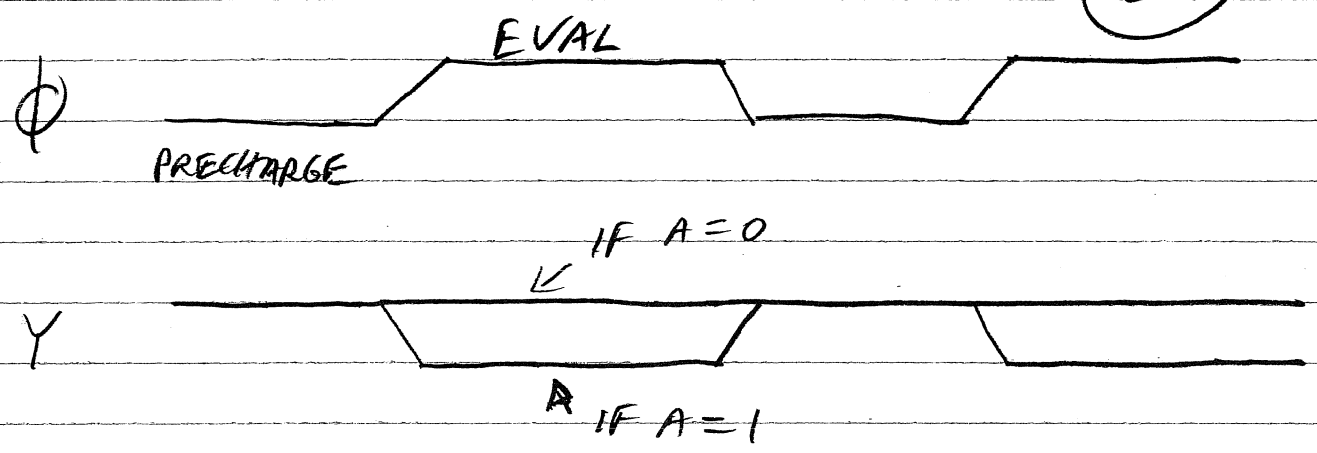


UNFOOTED



FOOTED

- FOOTED ALLOWS INPUT "A" TO BE "1" DURING PRECHARGE PHASE
- UNFOOTED REQUIRES "A" TO BE "0" DURING PRECHARGE PHASE



STRICT REQUIREMENT ON INPUTS

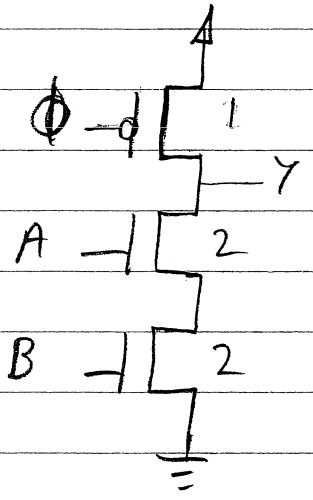
- INPUTS MUST BE MONOTONIC RISING
  ONE OF ...
  - LOW AND STAY LOW
  - LOW AND RISE HIGH ← (ALLOWED IF FOOTED, NOT IF UNFOOTED)
  - HIGH AND STAY HIGH

BUT NOT HIGH AND GO LOW

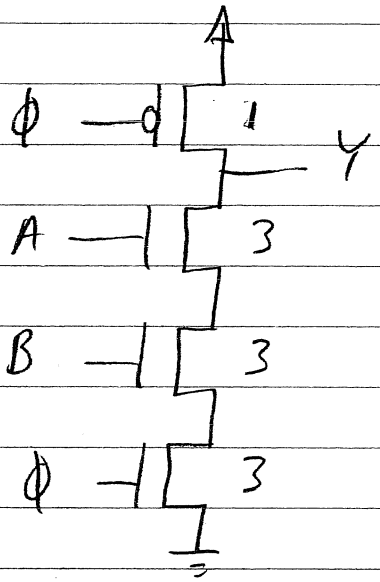
SINCE INPUT IS PRECHARGED HIGH AND CANNOT GO HIGH AGAIN IF DISCHARGED

- FOOTED ALLOWS CMOS GATES TO DRIVE DYNAMIC GATES

NAND 2

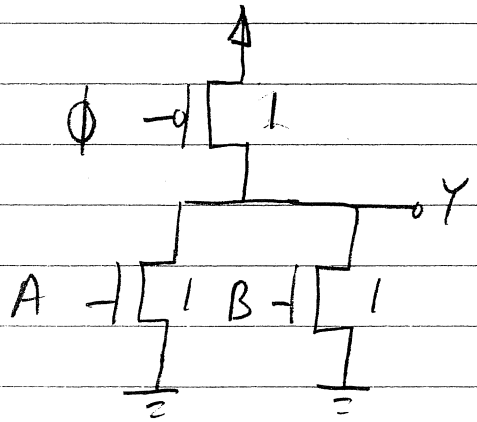


UNFOOTED

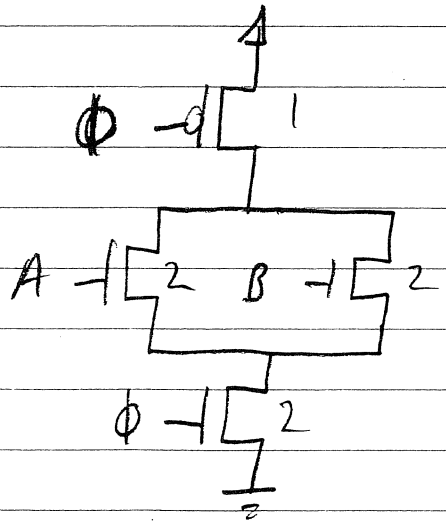


FOOTED

NOR 2



UNFOOTED

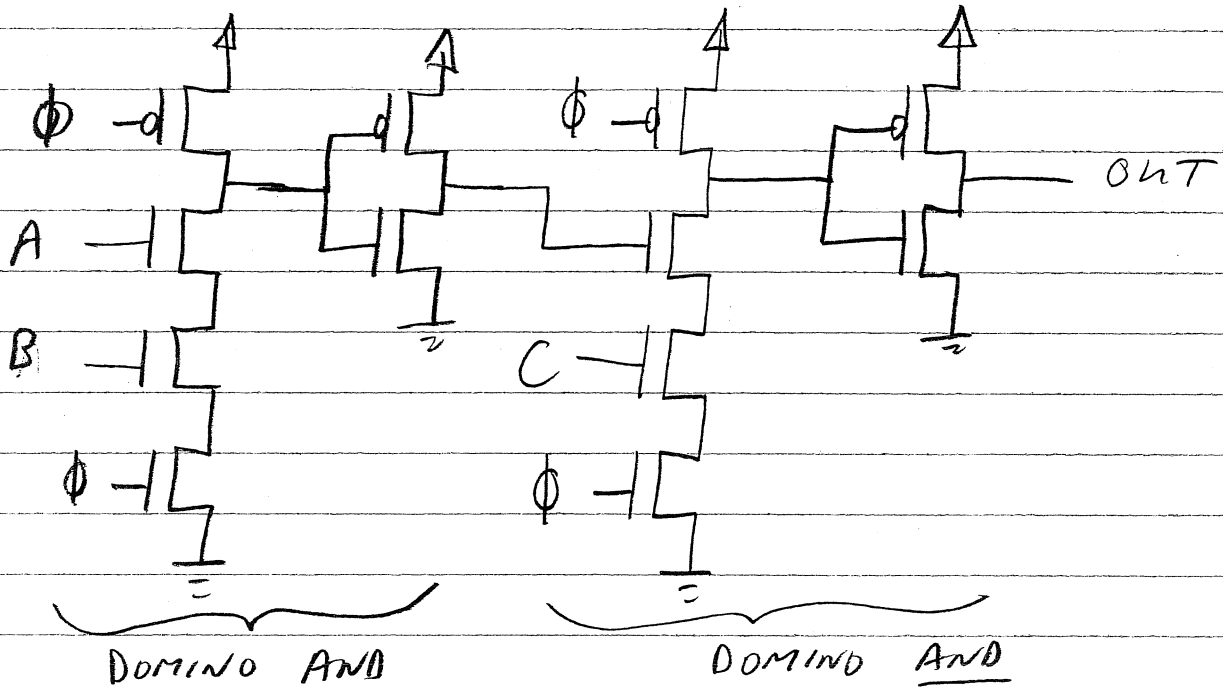


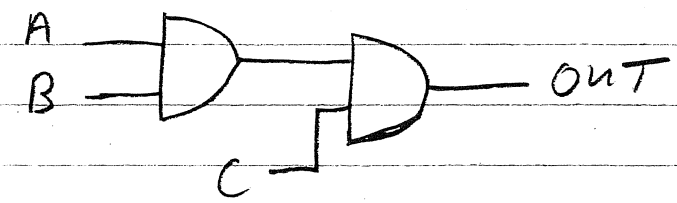
FOOTED

- CANNOT CONNECT Y DIRECTLY TO ANOTHER GATE AS IT VIOLATES ABOVE CONDITION.

- INSERT CMOS INVERTER BETWEEN GATES

  => DOMINO LOGIC (USES DYNAMIC GATES)

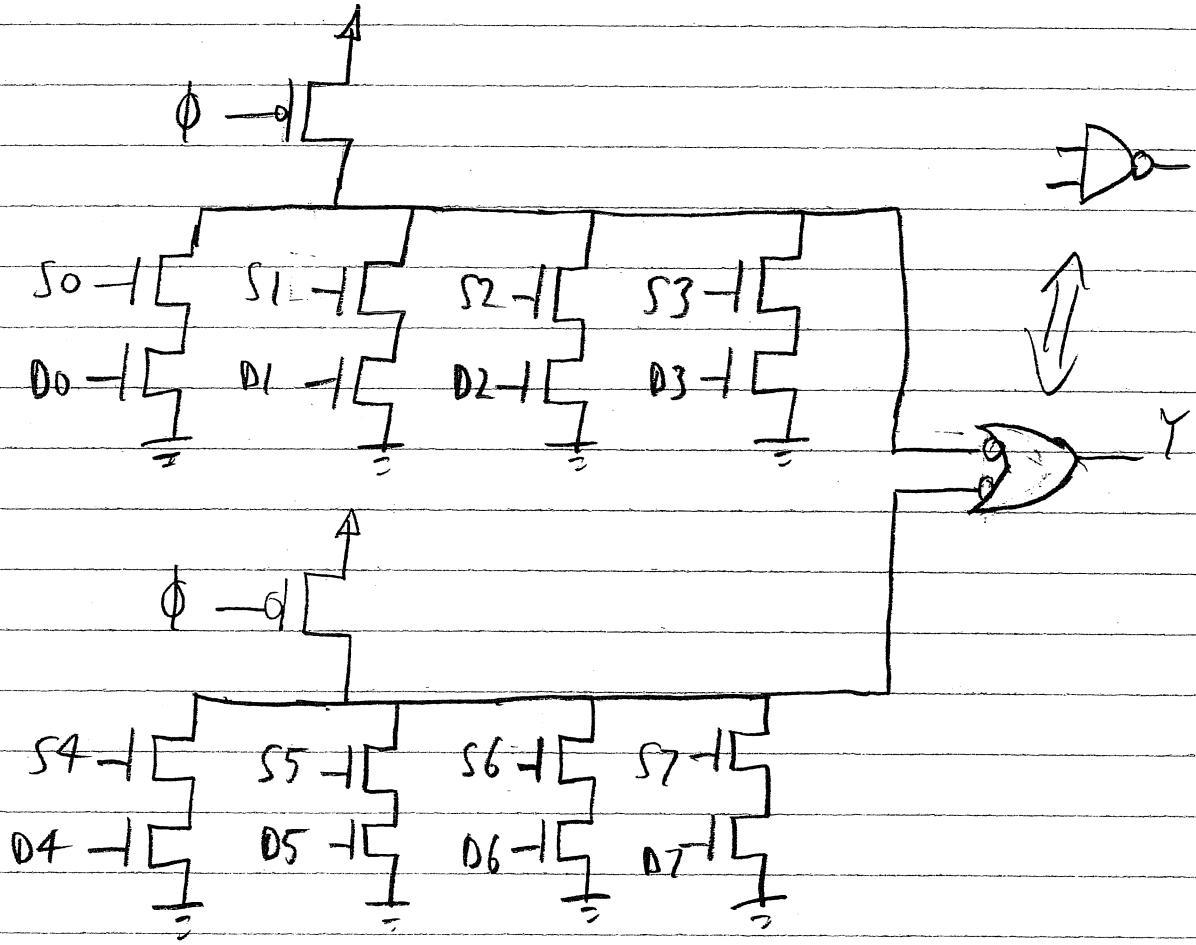




C-9A

CAN BUILD MORE COMPLEX GATES

8 - INPUT MULTIPLEXER USING 2 4 - INPUT MUXES



ONE OF S0 -> S7 HIGH

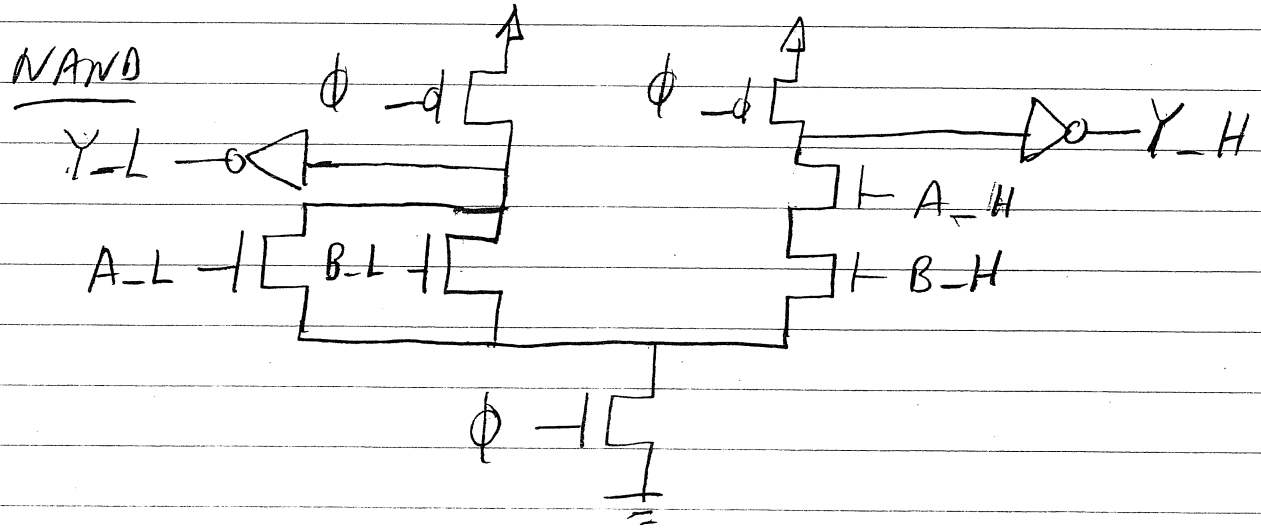
DOMINO GATES INHERENTLY NON-INVERTING

- IF LAST GATE, CAN USE CMOS INVERTER
- IF WITHIN DOMINO GATES, USE DUAL-RAIL DOMINO LOGIC

ALL INPUT/OUTPUT SIGNALS ENCODED AS A PAIR OF SIGNALS

SIG_H	SIG_L	MEANING
0	0	PRECHARGE
0	1	"0"
1	0	"1"
1	1	INVALID

SIMILAR TO CVSL



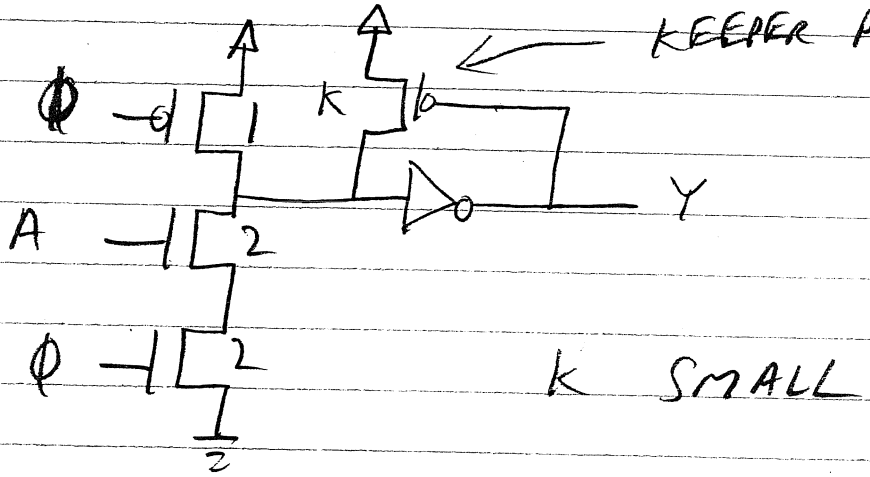
- CLOCK ϕ NEEDS TO ALWAYS RUN FOR LOGIC TO OPERATE

- DYNAMIC POWER HIGH DUE TO DUAL-RAIL AND ACTIVITY FACTOR HIGH DUE TO PRECHARGE PHASE

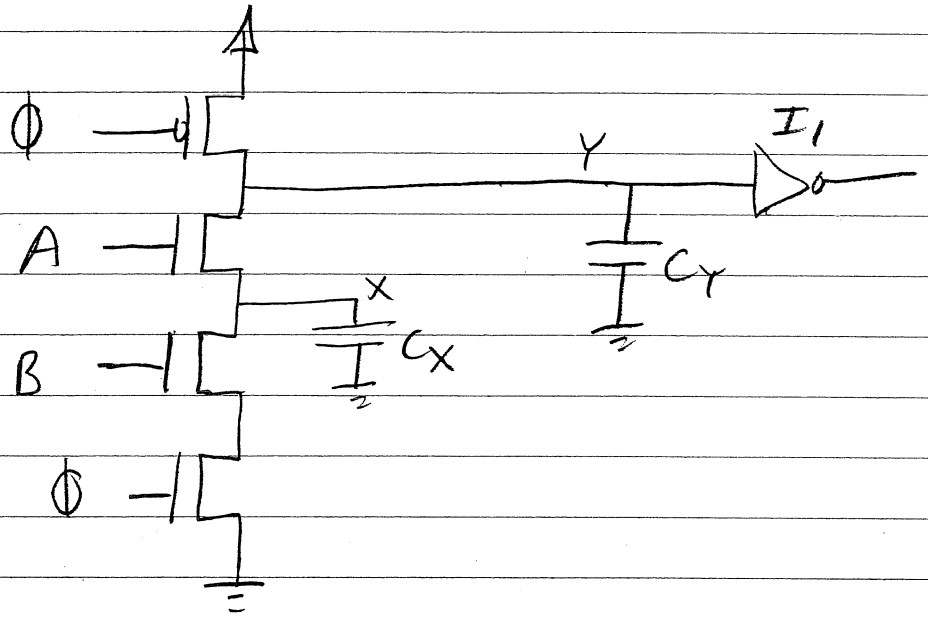
KEEPERS

- IF ϕ STOPPED, CHARGE LEAKAGE ON DYNAMIC NODE CAN CHANGE LOGIC VALUE (ON EVAL PHASE)

- USE SMALL $\frac{W}{L}$ PMOS TRANSISTOR TO OVERCOME LEAKAGE



CHARGE-SHARING ERRORS



IF NODE X NOT PRECHARGED BUT $V_X \approx 0$ + NODE V_Y PRECHARGED TO V_{DD}

CHARGE SHARING OCCURS IF $B=0$ $A=1$

$$V_x = V_y = \frac{C_Y}{C_Y + C_X} V_{DD}$$

MIGHT DROP V_Y BELOW V_{TH} OF I_1 AND ERROR OCCURS

- MIGHT PRECHARGE ALL OR SOME INTERNAL NODES TO REDUCE THIS EFFECT.