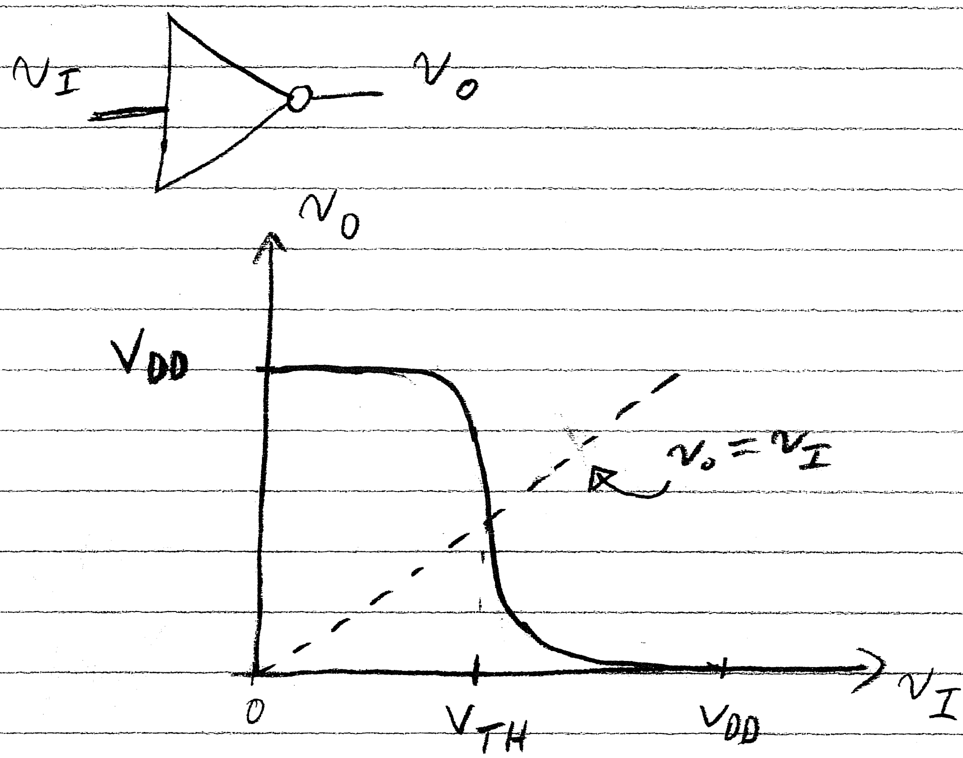
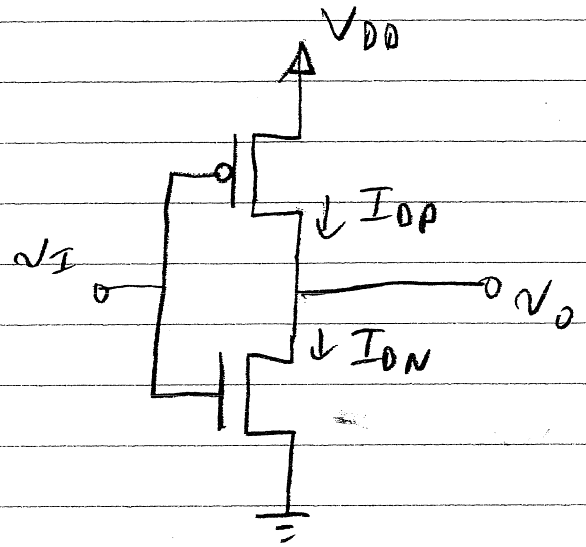
INVERTER DC TRANSFER CHARACTERISTICS



BY DEFINITION, THE THRESHOLD OF THE <u>INVERTER</u> IS WHERE $v_o = v_I$

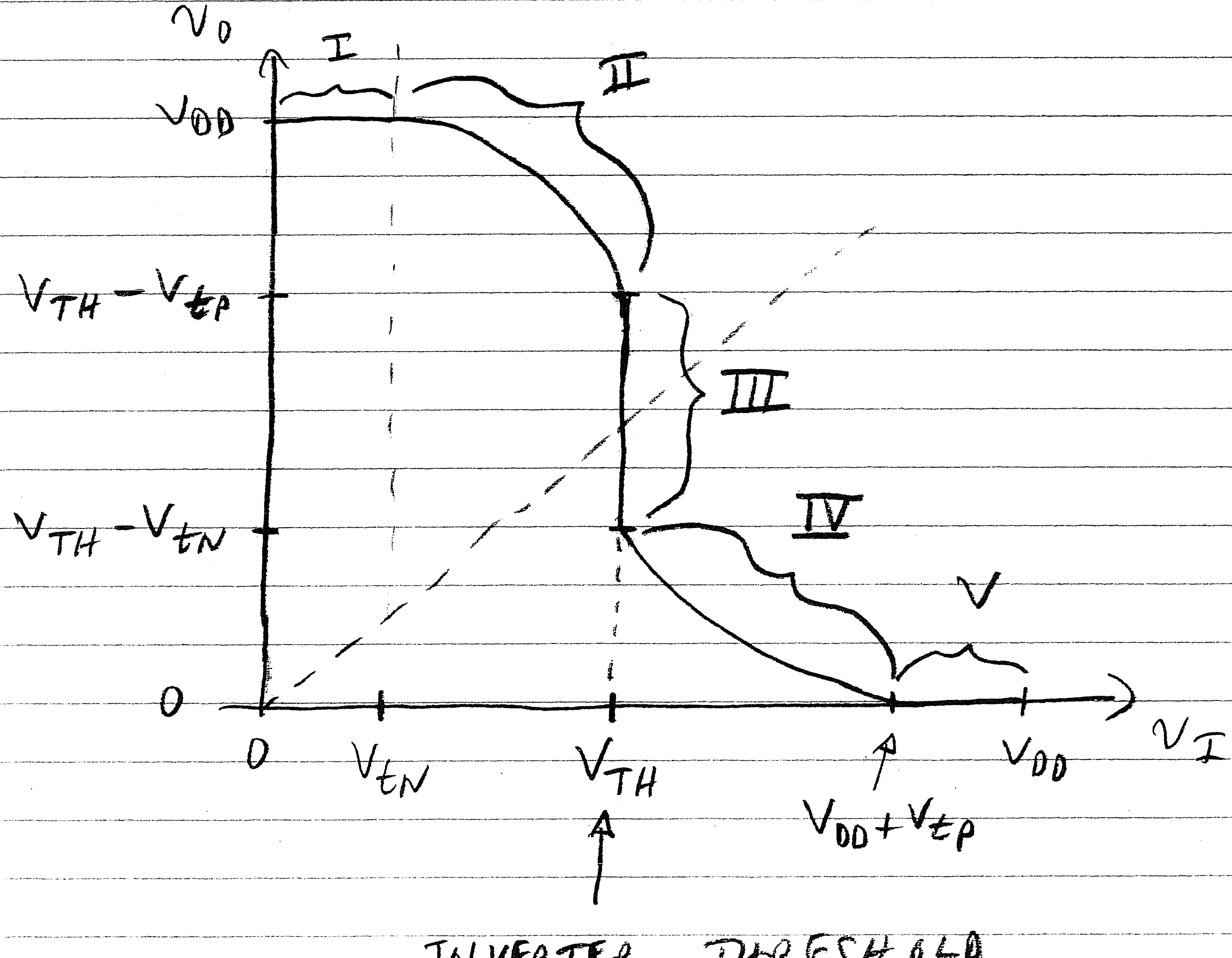
V_{TH} IS <u>INVERTER</u> THRESHOLD
(OR INPUT THRESHOLD)

CMOS INVERTER



PMOS: μ_P, V_{tP}, $\left(\frac{W}{L}\right)_P$

NMOS: μ_N, V_{tN}, $\left(\frac{W}{L}\right)_N$



REGION	NMOS	PMOS
I	CUTOFF	TRIODE
II	ACTIVE	TRIODE
III	ACTIVE	ACTIVE
IV	TRIODE	ACTIVE
V	TRIODE	CUTOFF

IN ALL REGIONS $I_{DN} = I_{DP}$ SINCE WE ARE LOOKING AT DC CURVE SO NO CURRENT FLOWS OUT OF v_o

V_{TH} OCCURS WHEN BOTH NMOS & PMOS ACTIVE (SINCE $V_{DS} = V_{GS}$ FOR BOTH NMOS & PMOS)

$$I_{DN} = \frac{\mu_N C_{ox}}{2}\left(\frac{W}{L}\right)_N (V_{TH} - V_{tN})^2 \quad (1)$$

$$I_{DP} = \frac{\mu_P C_{ox}}{2}\left(\frac{W}{L}\right)_P (V_{TH} - V_{DD} - V_{tP})^2 \quad (2)$$

(1) = (2) AND SOLVE FOR V_{TH}

$$V_{TH} = \frac{V_{DD} + V_{tP} + V_{tN}\, r}{1 + r}$$

WHERE $r = \sqrt{\dfrac{\mu_N (W/L)_N}{\mu_P (W/L)_P}}$

<u>EXAMPLE</u> $V_{tN} = 0.7\,V$ $V_{tp} = -0.8\,V$

$\mu_N C_{ox} = 190\,\mu A/V^2$ $\mu_p C_{ox} = 50\,\mu A/V^2$

$\left(\frac{W}{L}\right)_N = 2$ $\left(\frac{W}{L}\right)_p = 4$

$V_{DD} = 3.3V$ $r = \sqrt{\frac{(190)(2)}{(50)4}} = 1.38$

$$V_{TH} = \frac{3.3 - 0.8 + 0.7(1.38)}{1 + 1.38}$$

$$= 1.46\ V$$

NOTE THAT $V_{DD}/2 = 1.65\ V$

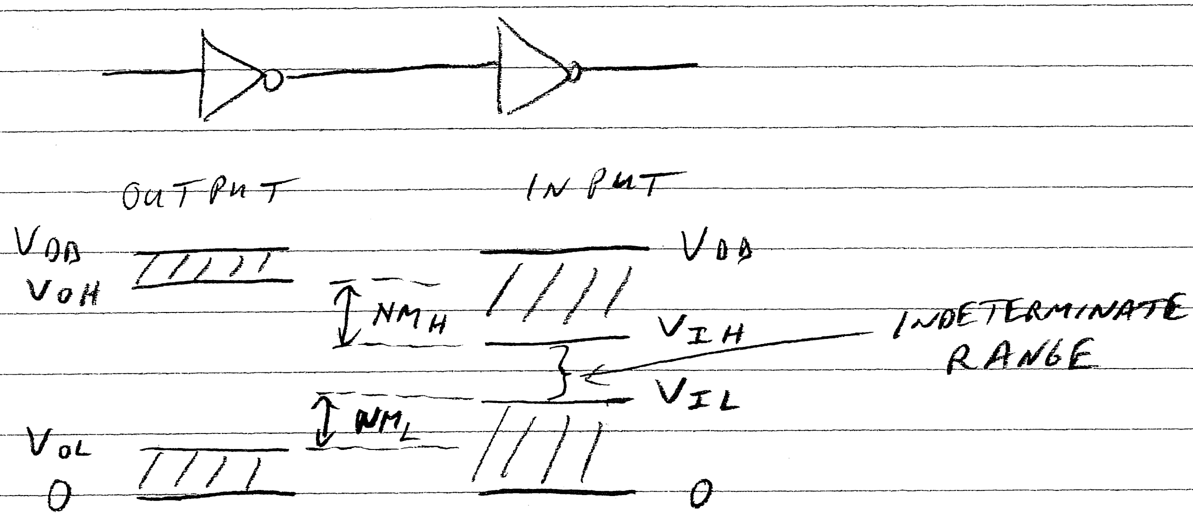
SO $V_{TH} < \frac{V_{DD}}{2}$

TO HAVE $V_{TH} = V_{DD}/2$ WHEN $V_{tN} = -V_{tp}$

LET $r = 1 \Rightarrow \mu_N \left(\frac{W}{L}\right)_N = \mu_p \left(\frac{W}{L}\right)_p$

HOWEVER THIS CHOISE OF V_{TH} IS <u>NOT</u> USUALLY BEST CHOICE FOR SPEED (DISCUSSED LATER)

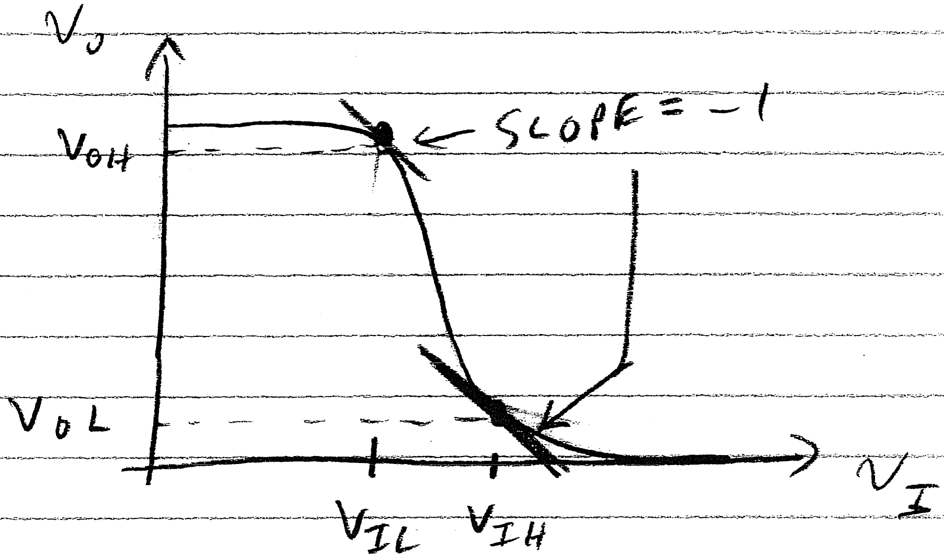
NOISE MARGIN



$$NM_H = V_{OH} - V_{IH}$$

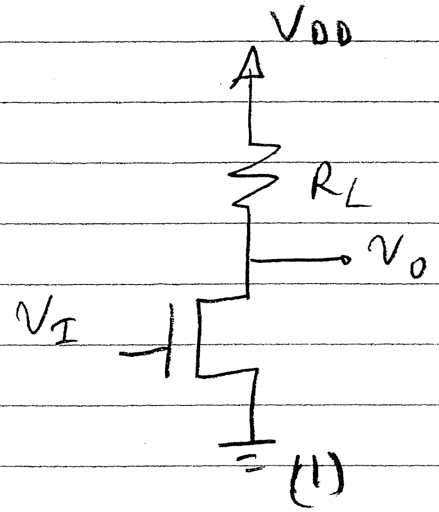
$$NM_L = V_{IL} - V_{OL}$$

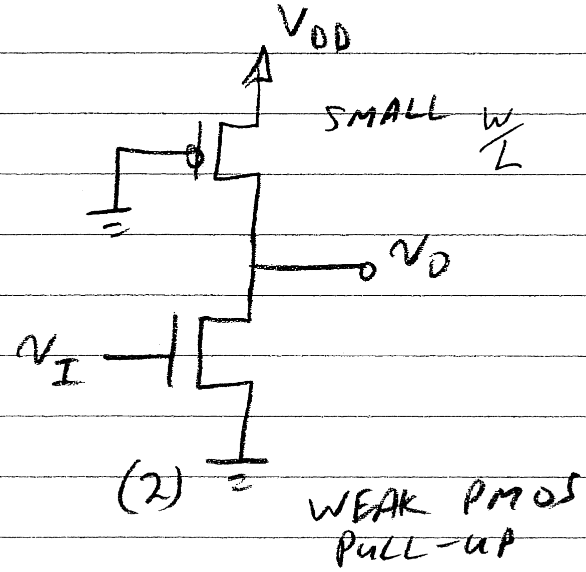
V_{IH} => MIN HIGH INPUT VOLTAGE
V_{IL} => MAX LOW INPUT VOLTAGE
V_{OH} => MIN HIGH OUTPUT VOLTAGE
V_{OL} => MAX LOW OUTPUT VOLTAGE

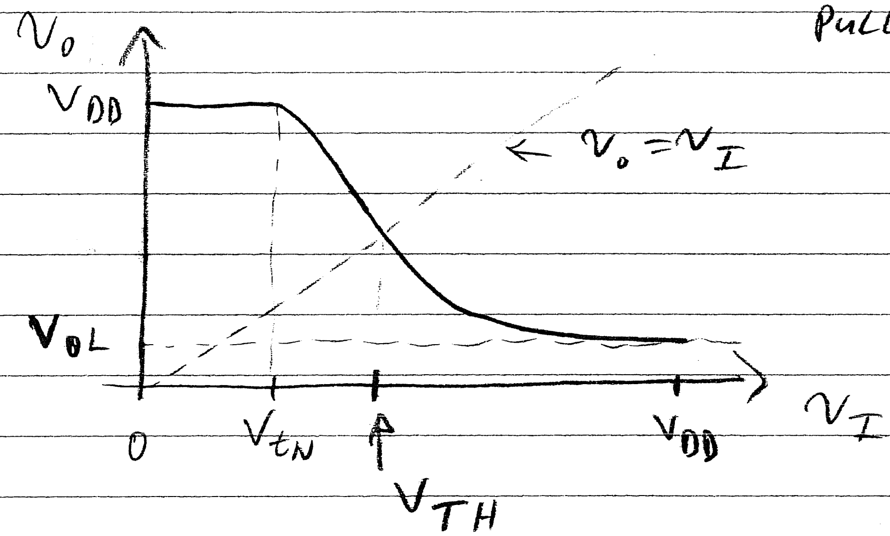


- CONSERVATIVE ESTIMATE OF NOISE MARGINS
- NOT USED IN INDUSTRY MUCH

RATIOED INVERTER LOGIC







<u>EXAMPLE</u> FIND V_{OL} & V_{TH} FOR CIRCUIT (1)

WHEN $R = 10\,k\Omega$, $\mu_N C_{ox} = 200\,\mu A/V^2$

$\left(\frac{W}{L}\right)_N = 10$

$V_{tN} = 0.5\,V$, $V_{DD} = 3\,V$

FOR V_{OL}, NMOS IN TRIODE

$$I_D = \mu_N C_{ox} \left(\frac{W}{L}\right)_N \left[(V_{GS} - V_{tN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = \mu_N C_{ox} \left(\frac{W}{L}\right)_N \left[(V_{DD} - V_{tN}) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

$$I_D = (2e-3)\left[(2.5) V_{OL} - \frac{V_{OL}^2}{2} \right] \quad (1)$$

ALSO

$$I_D = \frac{V_{DD} - V_{OL}}{R} = \frac{3 - V_{OL}}{1e4} \quad (2)$$

(1) = (2)

$$\frac{3 - V_{OL}}{1e4} = (2e-3)\left[2.5 V_{OL} - \frac{V_{OL}^2}{2} \right]$$

$$10 V_{OL}^2 - 51 V_{OL} + 3 = 0$$

$$V_{OL} = 5.04 \text{ OR } \underline{\underline{0.06 \text{ V}}}$$

5.04 ← NOT POSSIBLE

$\underline{V_{TH}}$ NMOS IN ACTIVE SINCE $V_{DS} = V_{GS}$

$$I_D = \frac{\mu_N C_{ox}}{2} \left(\frac{W}{L}\right)_N (V_{GS} - V_{tN})^2$$

$$I_D = (1e-3)(V_{TH} - 0.5)^2 \quad (1)$$

$$I_D = \frac{V_{DD} - V_{TH}}{R} = \frac{3 - V_{TH}}{1e4} \quad (2)$$

(1) = (2)

$$\frac{3 - V_{TH}}{1e4} = (1e-3)(V_{TH} - 0.5)^2$$

$$3 - V_{TH} = 10(V_{TH}^2 - V_{TH} + 0.25)$$

$$10V_{TH}^2 - 9V_{TH} - 0.5 = 0$$

$$V_{TH} = \underline{\underline{0.95}} \quad \text{OR} \quad \cancel{-0.05}$$

NOT POSSIBLE

STATIC POWER DISSIPATION WHEN $v_O = V_{OL}$

$$I_D = \frac{V_{DD} - V_{OL}}{R} = \frac{3 - 0.06}{1e4} = 29.4\,mA$$

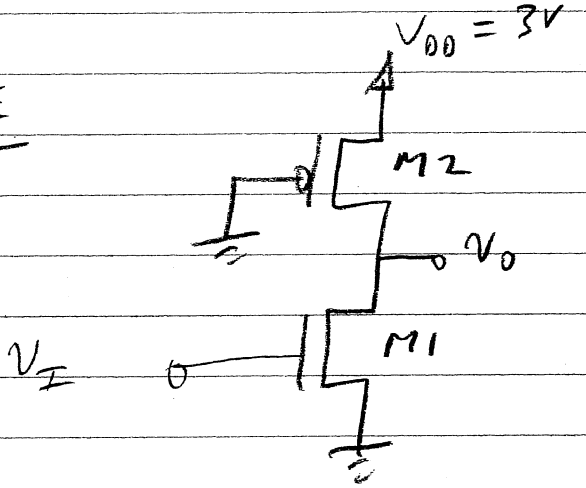
$$P_{DISS} = I_D V_{DD} = (29.4e-3)(3) = \underline{\underline{88.2\,mW}}$$

STATIC POWER DISSIPATION WHEN $V_o = V_{DD}$

$$I_D = \frac{V_{DD} - V_{DD}}{R} = 0$$

$$P_{DISS} = (0)(3) = \underline{\underline{0\ W}}$$

EXAMPLE



PMOS: $\mu_p C_{ox} = 50\ \mu A/V^2$
$V_{tp} = -0.5V$
$(W/L)_p = ?$

NMOS: $\mu_n C_{ox} = 200\ \mu A/V^2$
$(W/L)_N = 10$
$V_{tN} = 0.5V$

FIND SIZE OF $(W/L)_P$ SUCH THAT $V_{OL} = 0.3V$

ALSO FIND V_{TH} FOR INVERTER.

V_{OL} — M1 IN TRIODE SINCE $v_I = V_{DD} = 3V$ $\Rightarrow V_{GS} = 3V$

AN $V_D = 0.3V$
$\Rightarrow V_{DS} = 0.3V$

$$V_{DS} = 0.3V < V_{GS} - V_{tN} = 3 - 0.5 = 2.5V$$

$$I_{DN} = \mu_N C_{ox} \left(\frac{W}{L}\right)_N \left((V_{GS} - V_{tN}) V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$= (200)(10)\left((3 - 0.5) V_{OL} - \frac{V_{OL}^2}{2}\right)$$

$$I_{DN} = 2000\left(2.5(0.3) - \frac{0.3^2}{2}\right)$$

$$I_{DN} = 1410\ \mu A = 1.4\ mA \quad (1)$$

M2 IS IN <u>ACTIVE</u> SINCE

$$V_{GS} = 0 - V_{DD} = -3V$$

$$V_{DS} = V_{OL} - V_{DD} = 0.3 - 3V = -2.7V$$

$$\therefore\ V_{DS} < V_{GS} - V_{tp} = -3V + 0.5 = -2.5V$$

$$I_{Dp} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_p (V_{GS} - V_{tp})^2$$

$$= \frac{50}{2} \left(\frac{W}{L}\right)_p (-3 + 0.5)^2$$

$$= 156.25 \left(\frac{W}{L}\right)_p \quad (2)$$

$$(1) = (2) \Rightarrow \left(\frac{W}{L}\right)_p = \frac{1410}{156.25} = 9.0$$

$$\left(\frac{W}{L}\right)_p = 9.0$$

$\underline{V_{TH}}$ M1 ACTIVE SINCE $V_{DS} = V_{GS}$
SINCE $v_O = v_I$ BY DEFINITION

$$I_{DN} = \frac{\mu_N C_{ox}}{2}\left(\frac{W}{L}\right)_N (V_{GS} - V_{tN})^2$$

$$I_{DN} = 1000\,(V_{TH} - 0.5)^2 \quad (1)$$

M2 TRIODE IF $V_{TH} > 0.5\,V$ (TRUE SINCE I_{DN} ON)

$$I_{DP} = \mu_P C_{ox}\left(\frac{W}{L}\right)_P \left((V_{GS} - V_{tP})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

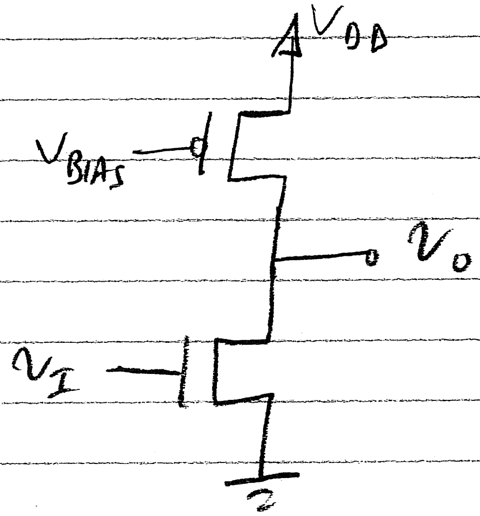
$$I_{DP} = (50)(9)\left[(-3+0.5)(V_{TH}-3) - \frac{(V_{TH}-3)^2}{2}\right] \quad (2)$$

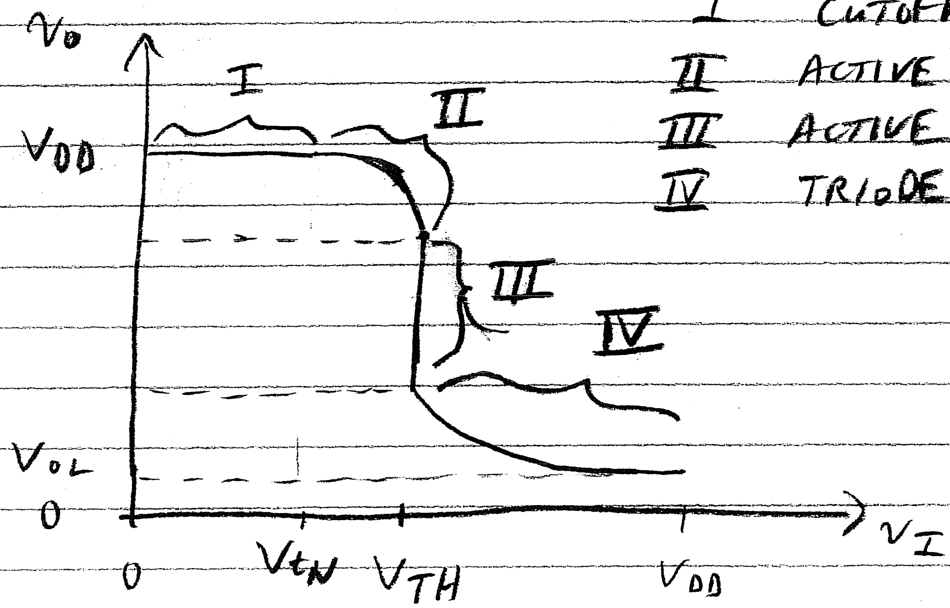
(1) = (2) SOLVE FOR V_{TH}

$V_{TH} = \underline{1.57}$ OR ~~-0.57~~ NOT POSSIBLE

RATIOED INVERTER LOGIC

WITH PULL-UP CURRENT SOURCE





	NMOS	PMOS
I	CUTOFF	TRIODE
II	ACTIVE	TRIODE
III	ACTIVE	ACTIVE
IV	TRIODE	ACTIVE

EXAMPLE PMOS $\left(\frac{W}{L}\right)_P = 20$ $\mu_p C_{ox} = 50\ \mu A/V^2$

$V_{DD} = 3V$ $V_{tP} = -0.5V$ $V_{BIAS} = 1.5V$

NMOS $\left(\frac{W}{L}\right)_N = ?$ $\mu_N C_{ox} = 200\ \mu A/V^2$

$V_{tN} = 0.5V$

FIND $\left(\frac{W}{L}\right)_N$ SUCH THAT $V_{TH} = 1.5\,V$

BOTH ACTIVE

$(V_{TH} - V_{DD})$

$$I_{DP} = \left(\frac{50}{2}\right)(20)(-1.5 + 0.5)^2 = 500\ \mu A \quad (1)$$

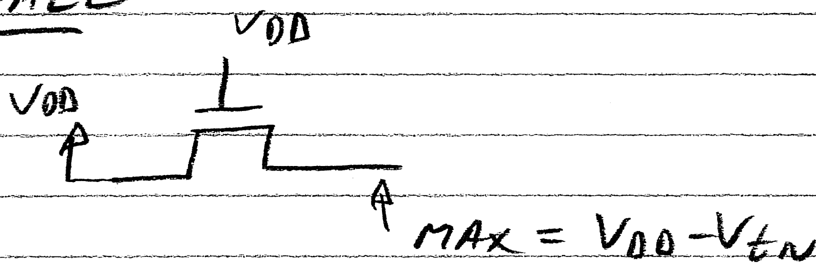
V_{TH}

$$I_{DN} = \left(\frac{200}{2}\right)\left(\frac{W}{L}\right)_N (1.5 - 0.5)^2 \quad (2)$$

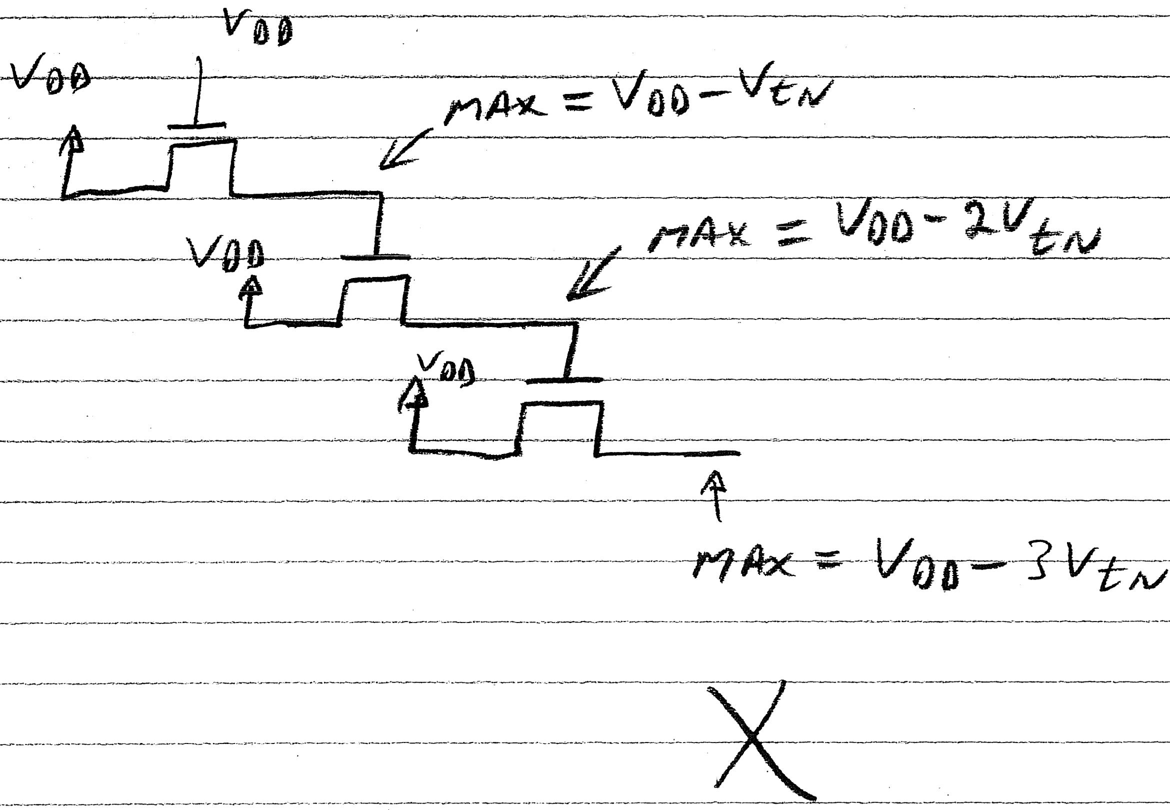
$$(1) = (2) \Rightarrow \left(\frac{W}{L}\right)_N = 5$$

PASS TRANSISTOR AT DC

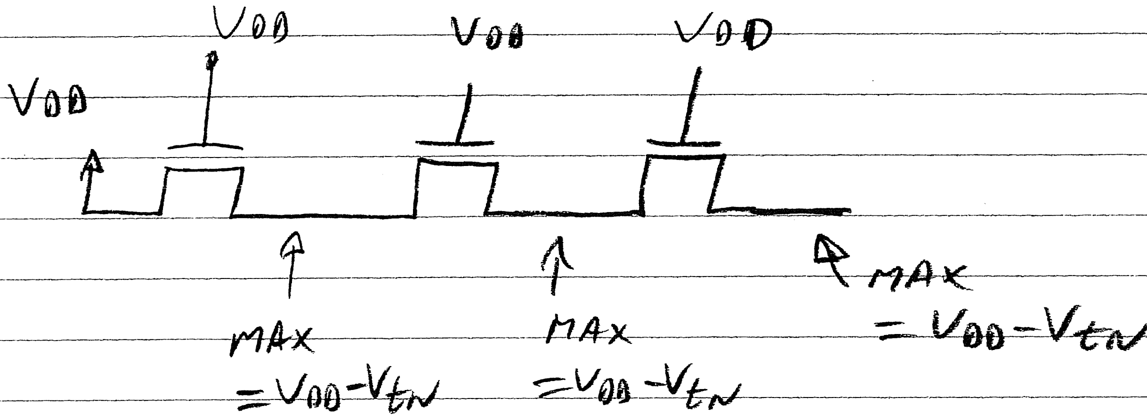
RECALL



BAD DESIGN



OKAY DESIGN (BUT SLOW)



BUT SIGNAL AT LEFT END HAS TO GO THROUGH MULTIPLE TRANSISTORS AS THEY TURN OFF.