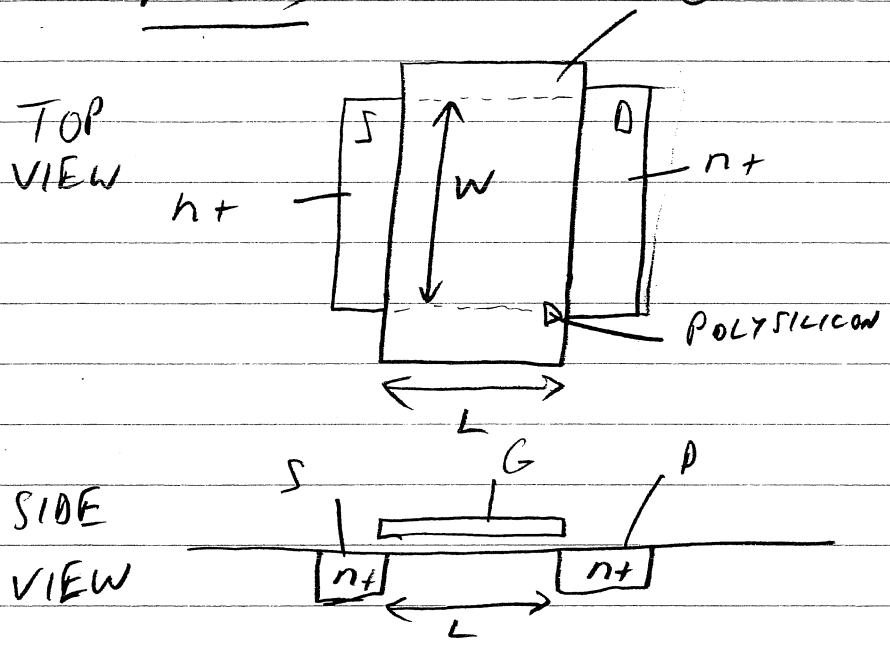
MOS TRANSISTORS

NMOS



G - GATE
D - DRAIN
S - SOURCE
B - BULK
W - WIDTH
L - LENGTH

P - (B)

THRESHOLD VOLTAGE V_{tN} (NOTE $V_{tN} \pm V_T = \frac{kT}{9}$)

$V_{tN} \simeq 0.2V \rightarrow 0.5V$ DEPENDING ON PROCESS

IF $V_{GS} < V_{tN}$ NO CURRENT FLOWS

$I_D = 0$

CHANNEL REMAINS P-TYPE

DEFINE $\beta_N \equiv \mu_N C_{ox}\left(\frac{W}{L}\right)$

$\mu_N \Rightarrow$ MOBILITY OF ELECTRONS IN CHANNEL OF NMOS

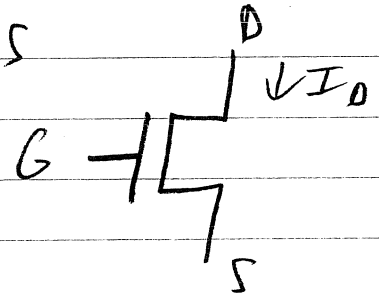
$C_{ox} \Rightarrow$ GATE OXIDE CAPACITANCE PER UNIT AREA

$W \Rightarrow$ TRANSISTOR WIDTH

$L \Rightarrow$ TRANSISTOR LENGTH

SIMPLIFIED MOS MODELLING

NMOS



- SOURCE IS DRAIN/SOURCE JUNCTION WHICH IS AT A LOWER VOLTAGE
- CAN CHANGE DURING OPERATION

$V_{tN} > 0$

$I_D \geq 0$

$V_{DS} \geq 0$

3 REGIONS OF OPERATION

CUTOFF $V_{GS} \leq V_{tN}$

$$I_D = 0$$

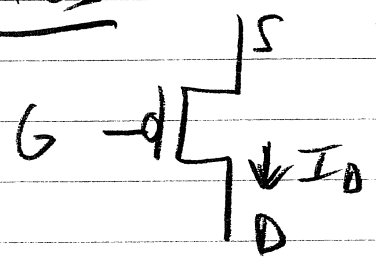
TRIODE $V_{GS} \geq V_{tN}$, $V_{DS} \leq V_{GS} - V_{tN}$

$$I_D = \beta_N \left[(V_{GS} - V_{tN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

ACTIVE (SATURATION) $V_{GS} \geq V_{tN}$, $V_{DS} \geq V_{GS} - V_{tN}$

$$I_D = \frac{\beta_N}{2} (V_{GS} - V_{tN})^2$$

PMOS



SOURCE IS DRAIN/SOURCE JUNCTION AT **HIGHER** VOLTAGE

$$\beta_P \equiv \mu_P C_{ox} \frac{W}{L}$$

$\mu_P \Rightarrow$ MOBILITY OF HOLES IN PMOS CHANNEL

$C_{ox} \Rightarrow$ **SAME AS NMOS**

PMOS

THRESHOLD VOLTAGE, V_{tp}

$V_{tp} < 0$

$I_D \geq 0 \qquad V_{DS} \leq 0$

CUTOFF $\quad V_{GS} \geq V_{tp}$

$I_D = 0$

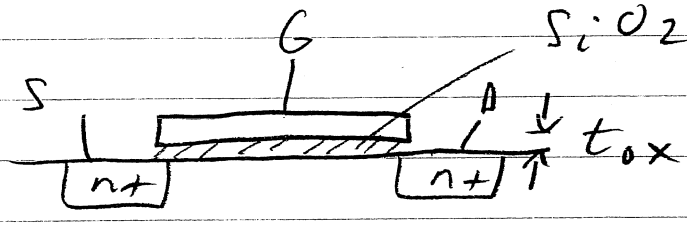
TRIODE $\quad V_{GS} \leq V_{tp}, \quad V_{DS} \geq V_{GS} - V_{tp}$

$$I_D = \beta_p \left[(V_{GS} - V_{tp}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

ACTIVE $\quad V_{GS} \leq V_{tp}, \quad V_{DS} \leq V_{GS} - V_{tp}$

$$I_D = \frac{\beta_p}{2} (V_{GS} - V_{tp})^2$$

C_{ox}



$$C_{ox} = \frac{k_{ox}\,\varepsilon_0}{t_{ox}}$$

UNITS OF F/m^2 [OR $fF/(\mu m)^2$]

k_{ox} => RELATIVE PERMITTIVITY OF SiO_2 RELATIVE TO FREE SPACE

$$k_{ox} \cong 3.9$$

ε_0 => PERMITTIVITY OF FREE SPACE

$$\varepsilon_0 = 8.854 \times 10^{-12}\ F/m$$

t_{ox} => OXIDE THICKNESS

t_{ox} FROM $1.5 \times 10^{-9}\ m$ TO $1 \times 10^{-8}\ m$

(15 Å TO 100 Å)

t_{ox} SAME FOR PMOS & NMOS ON SAME CHIP SO C_{ox} SAME AS WELL.

IF $t_{ox} = 30\ \text{Å}$

$$C_{ox} = \frac{3.9 \times 8.854 \times 10^{-12}}{30 \times 10^{-10}}$$

$$= 1.15e{-}2\ F/m^2$$

$$= 1.15e{-}14\ F/(\mu m)^2$$

$$= 11.5\ fF/(\mu m)^2$$

μ_N + μ_P

$\mu_N \approx 0.06\ m^2/V.s$

$\mu_P \approx 0.015\ m^2/V.s$

$\mu_N \approx 4\,\mu_P$ TYPICALLY

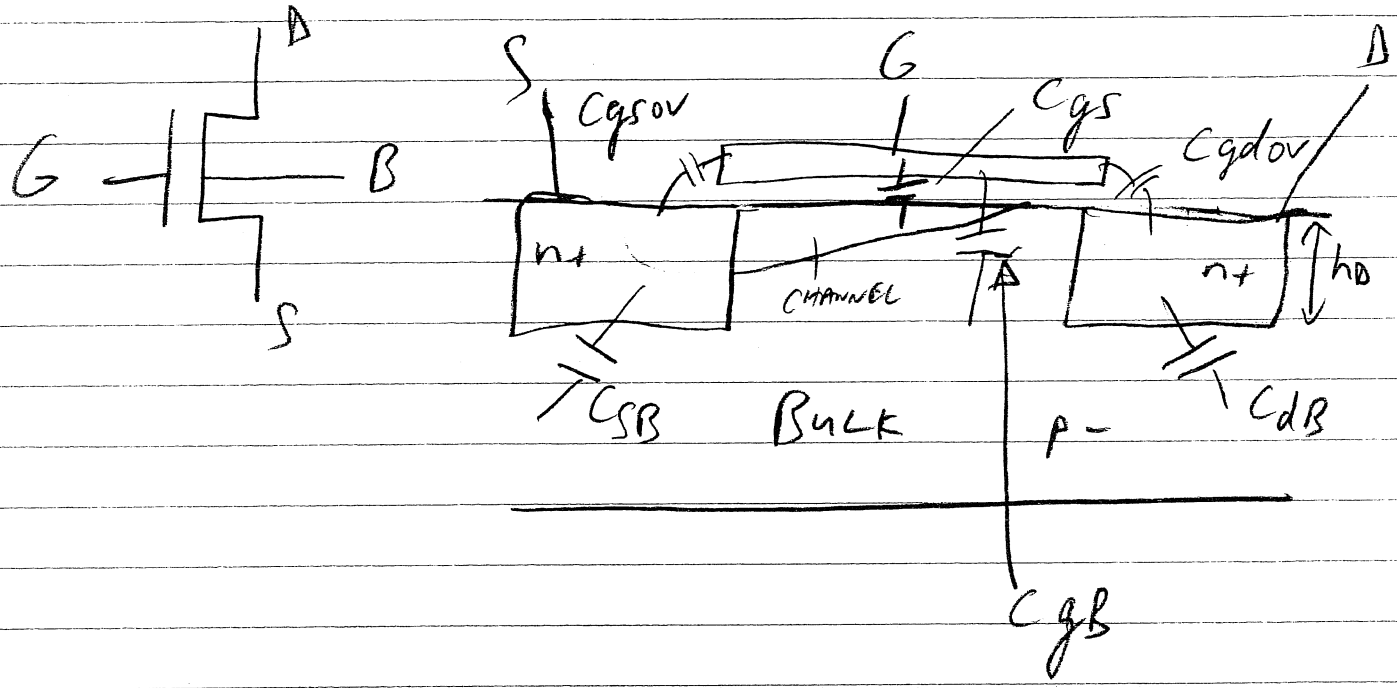
SO IF $|V_{tP}| = |V_{tN}|$ + $\left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_N$

$I_{DN} \approx 4 I_{DP}$ FOR SAME V_{GS}, V_{DS}

SO NMOS FASTER THAN PMOS

TO CHARGE/DISCHARGE CAPACITORS

2.3 MOS CAPACITORS (NMOS OR PMOS)



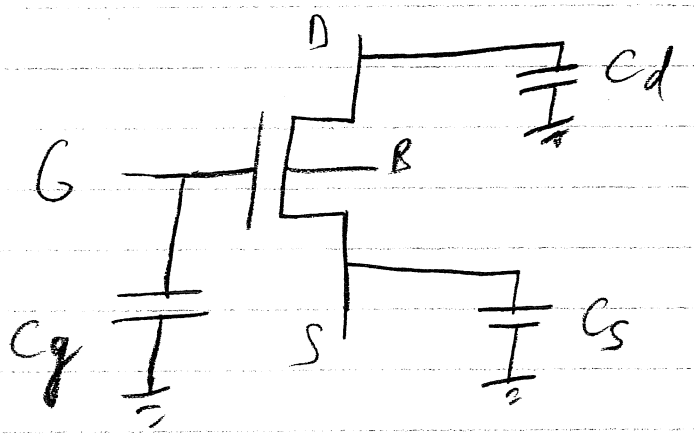
C_{gs} GATE TO SOURCE CAP (CHANNEL CONNECTS TO SOURCE)

$C_{gdov} + C_{gsov}$ GATE OVERLAP CAPACITANCE

C_{dB} & C_{SB} REVERSE BIASED DIODES

C_{gB} GATE TO BULK CAP

SIMPLE MODEL



(L_{MIN} MIN LENGTH ALLOWED)

$$C_g = C_{ox} W L$$

DEFINE $C_{g\mu} \equiv C_{ox} L_{MIN}$

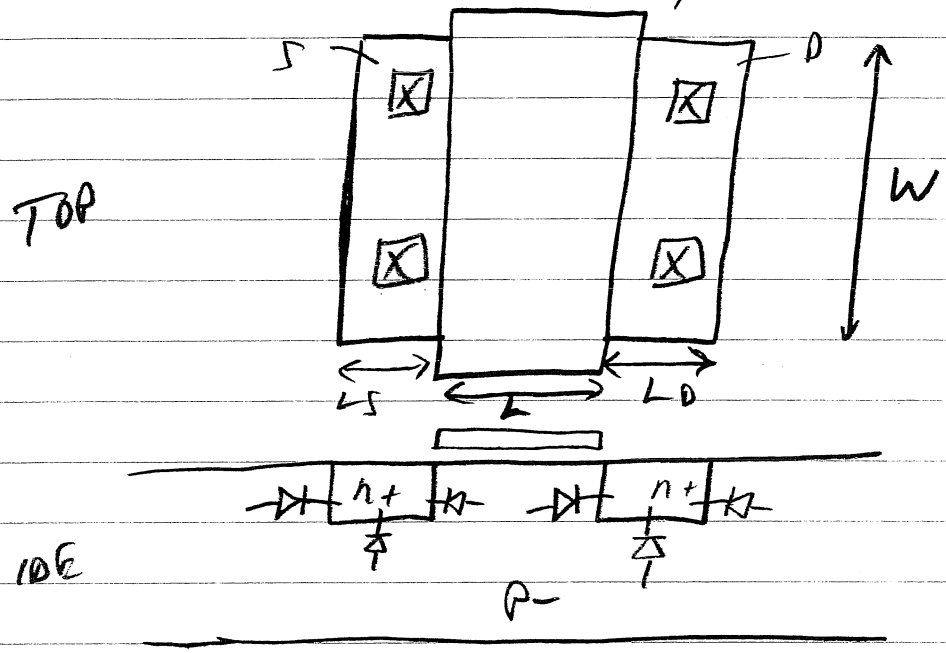
THEN FOR TRANSISTORS USING L_{MIN}

$$\boxed{C_g = C_{g\mu} W}$$

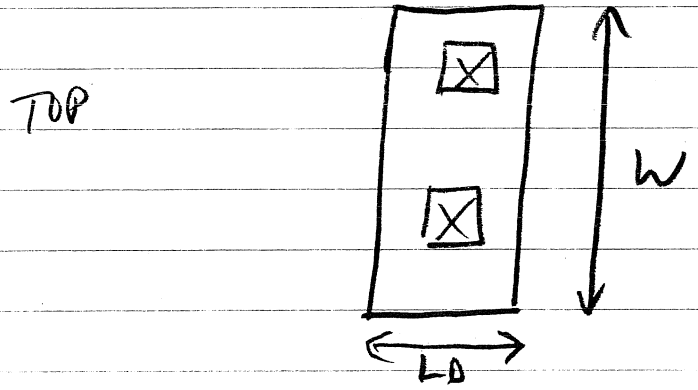
TYPICALLY $C_{g\mu} \approx 2\,fF/\mu m$

FOR MOST TECHNOLOGIES SINCE t_{ox} SCALES AS L_{MIN} SCALES & $C_{ox} = \frac{k_{ox}\,\varepsilon_0}{t_{ox}}$

DRAIN/SOURCE CAPS, C_d + C_S



CONSIDER ONLY DRAIN, C_d



C_{dA}
CAP DUE TO AREA OF DRAIN

C_{dP}
CAP DUE TO PERIMETER OF DRAIN

SIDEWALL CAP (PERIMETER RELATED)

BOTTOM CAP (AREA RELATED)

C_{jbs} CAP PER UNIT AREA OF PN JUNCTION $[F/m^2]$

$$\boxed{C_d = C_{dA} + C_{dp}}$$

WHERE $\boxed{C_{dA} = C_{jbs} W L_D}$

$$C_{dp} = C_{jbs}(W + L_D + W + L_D) h_D$$
$$= C_{jbs}(2W + 2L_D) h_D$$

DEFINE

$$C_{jbsw} \equiv C_{jbs} h_D \quad [F/m]$$

$$\boxed{C_{dp} = C_{jbsw}(2(W + L_D))}$$

WL_D AREA OF DRAIN

$2(W + L_D)$ PERIMETER OF DRAIN

$$C_d = C_{jbs} W L_D + C_{jbsw}(2)(W + L_D) \quad (1)$$

IF L_D IS MINIMUM $L_{D_{MIN}}$

DEFINE $C_{d\mu} \equiv C_{jbs} L_{D_{MIN}} + 2 C_{jbsw}$

0% ① BECOMES

$$C_d = C_{d_\mu} W + 2 L_{D_{MIN}} C_{jbsw}$$

BUT $C_{d_\mu} W \gg 2 L_{D_{MIN}} C_{jbsw}$

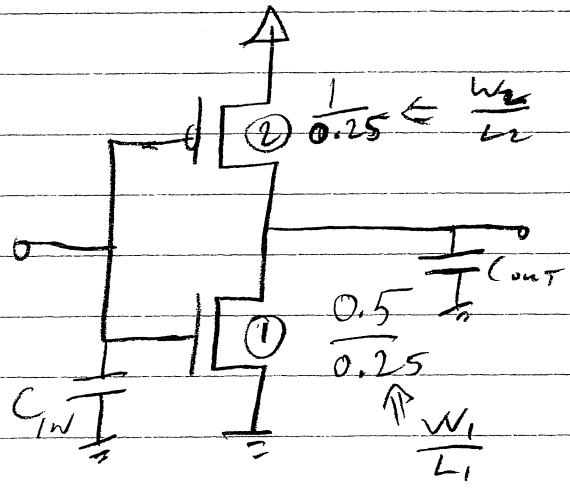
SO $\boxed{C_d \approx C_{d_\mu} W}$

SIMILAR FOR

$$\boxed{C_s \approx C_{s_\mu} W}$$

TYPICALLY $C_{d_\mu} = C_{s_\mu} \approx 1\text{-}2\ fF/\mu m$

EXAMPLE $L_{MIN} = 0.25\,\mu m$ $C_{gu} = 2\,fF/\mu m$ $C_{du} = 1\,fF/\mu m$



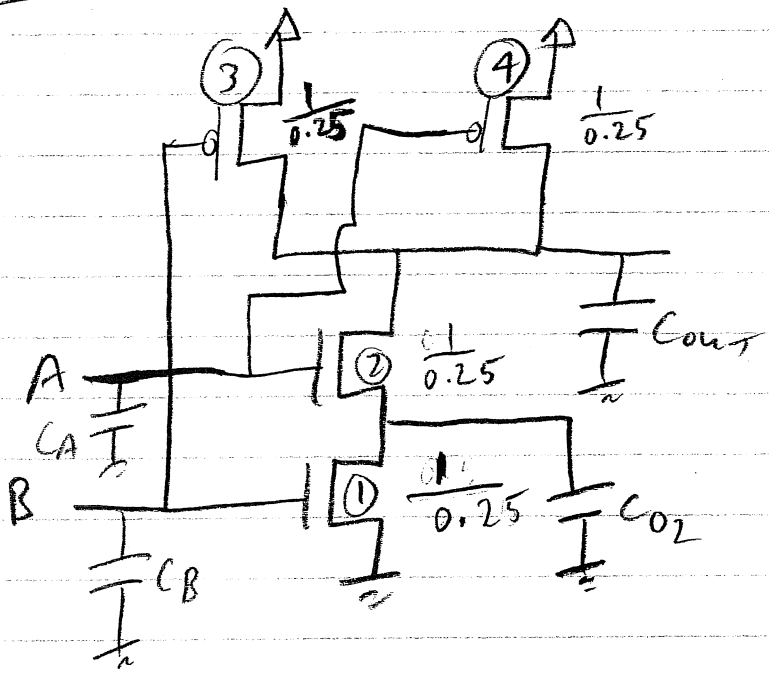
FIND C_{IN} & C_{OUT}.

$$C_{IN} = C_{gu} W_1 + C_{gu} W_2 = C_{gu}(W_1 + W_2)$$

$$= 2\,(fF/\mu m)[1.5\,\mu m] = \underline{3\,fF}$$

$$C_{OUT} = C_{du} W_1 + C_{du} W_2 = \underline{1.5\,fF}$$

EXAMPLE



$$C_A = C_B = C_{gn}(W_1 + W_3) = \underline{\underline{4\,fF}}$$

$$C_{OUT} = C_{dn}(W_2 + W_3 + W_4) = 3\,fF$$

$$C_{O2} = C_{dn}(W_1 + W_2) = 2\,fF$$

DETAILED CAPACITOR VALUES

C_{gs} & C_{gB} DEPEND ON ACTIVE, CUTOFF OR TRIODE REGION

	CUTOFF	TRIODE	ACTIVE
C_{gb}	C_o	0	0
C_{gs}	0	$C_o/2$	$\frac{2}{3}C_o$
C_{gd}	0	$C_o/2$	0

$$C_o = C_{ox} W L = C_{gm} W$$

$\frac{2}{3} C_o$ DUE TO CHANNEL SHAPE WHEN ACTIVE

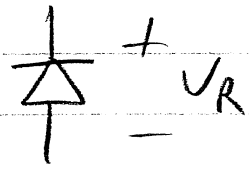
C_{gsov} & C_{gdov}

$$C_{gsov} = C_{gsOL} W$$

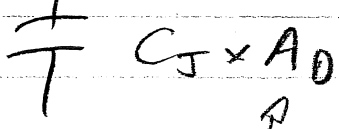
$$C_{gdov} = C_{gdOL} W$$

$C_{gsOL} = C_{gdOL}$ TYPICALLY

C_{SB} & C_{dB}



MODEL AS ⇒



REVERSE BIASED

AREA OF DIODE

$$C_J = \frac{C_{J0}}{\left(1 + \frac{V_R}{\phi_0}\right)^{M_J}}$$

WHERE C_{J0} IS CAPACITANCE/AREA AT $V_R = 0$

V_R IS REVERSE BIAS VOLTAGE

ϕ_0 IS BUILT IN POTENTIAL ($\phi_0 \approx 0.9V$)

M_J IS JUNCTION GRADING COEFF

0.3 → 0.5

$$C_{DB} = W L_D C_{jBS} + (W + 2L_D) C_{jBSw} + W C_{jBSwg}$$

$$C_{SB} = W L_S C_{jBS} + (W + 2L_S) C_{jBSw} + W C_{jBSwg}$$

$C_{jBS} \Rightarrow C_{j1}$ FOR BOTTOM OF DRAIN/SOURCE

$C_{jBSW} = C_{j2} \times h_D$ FOR SIDEWALL OF " NOT UNDER GATE

$C_{jBSWg} = C_{j3} \times h_D$ SIDEWALL UNDER GATE

C_{j1}, C_{j2}, C_{j3} NOT NECESSARILY SAME

DUE TO DIFFERENT GRADING AND/OR DOPING LEVELS