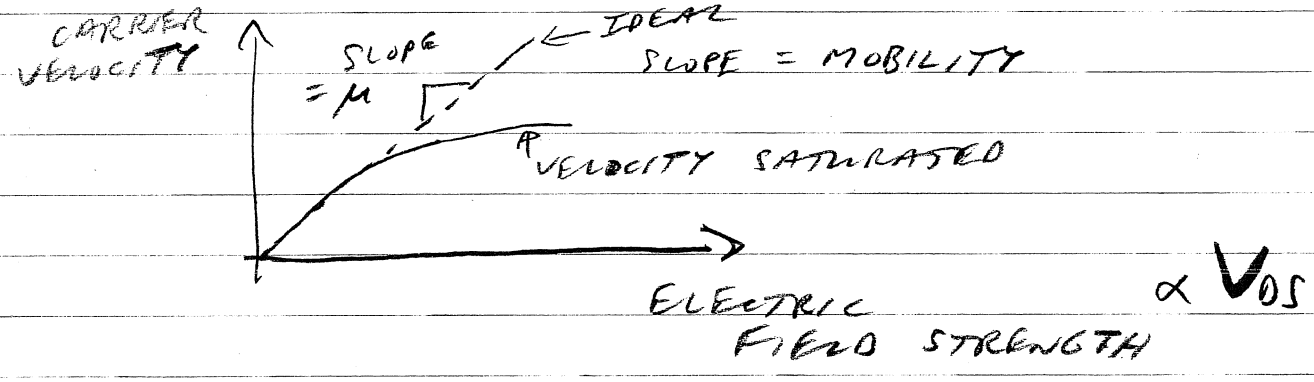
2.4 NON-IDEAL I-V EFFECTS

1) - VELOCITY SATURATION
2) - CHANNEL LENGTH MODULATION
3) - BODY EFFECT
4) - SUBTHRESHOLD CONDUCTION
5) - JUNCTION LEAKAGE
6) - TUNNELING
7) - TEMPERATURE DEPENDENCE
8) - GEOMETRY DEPENDENCE

1) VELOCITY SATURATION



IDEAL $I_D = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$ (ACTIVE REGION)

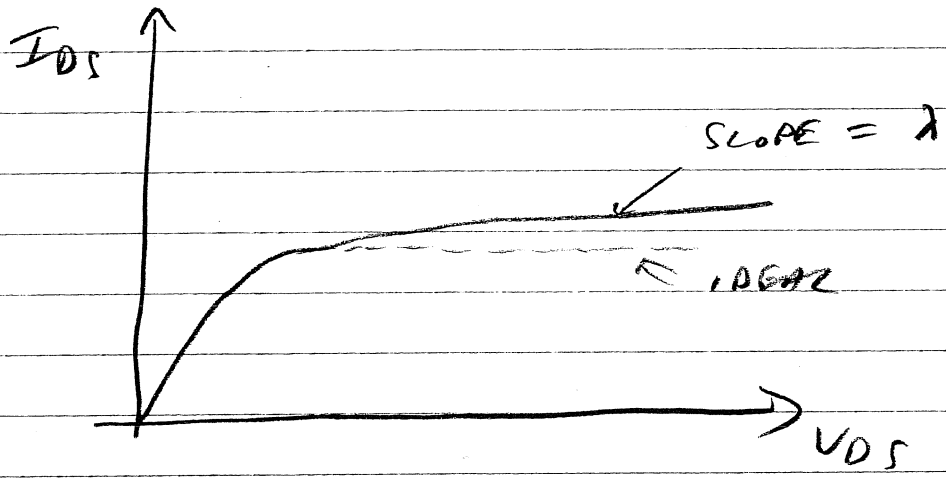
$I_D \propto (V_{GS}-V_t)^2$

VELOCITY SATURATED $I_D \propto (V_{GS}-V_t)$ NOT SQUARE LAW RELATED

(AS V_{DS} INCREASES)

2) CHANNEL-LENGTH MODULATION IN ACTIVE REGION

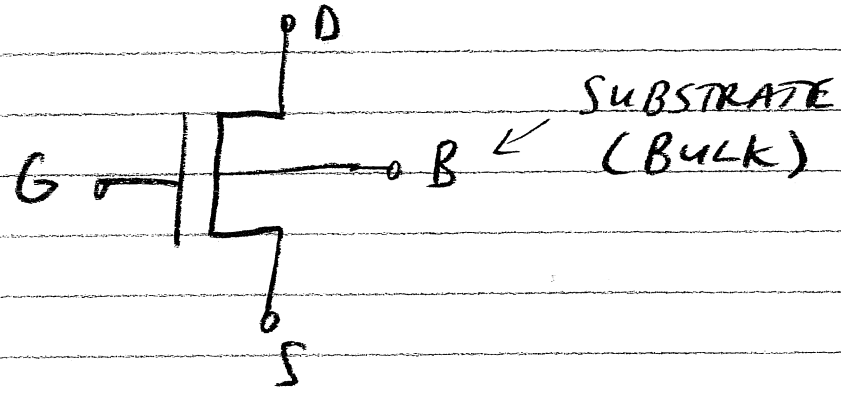
$$I_{DS} = \frac{\mu_N C_{ox}}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$



TYPICALLY NOT IMPORTANT FOR DIGITAL DESIGN

3) BODY EFFECT

V_{tN} IS A FUNTION OF V_{SB}



$$V_{tN} = V_{tN0} + \gamma\left(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s}\right)$$

V_{tN0} THRESHOLD VOLTAGE WITH $V_{SB} = 0$

V_{SB} SOURCE TO SUBSTRATE VOLTAGE

γ BODY EFFECT COEFFICIENT GIVEN FOR A DEVICE $\gamma \approx 0.4\ V^{\frac{1}{2}}$

ϕ_s SURFACE POTENTIAL GIVEN FOR A DEVICE $\phi_s \approx 0.9\ V$

EXAMPLE GIVEN $V_{tNO} = 0.4\ V$

$\gamma = 0.3\ \sqrt{V}$

$\phi_S = 0.9\ V$

FIND V_{tN} WHEN $V_{SB} = 1.5V$

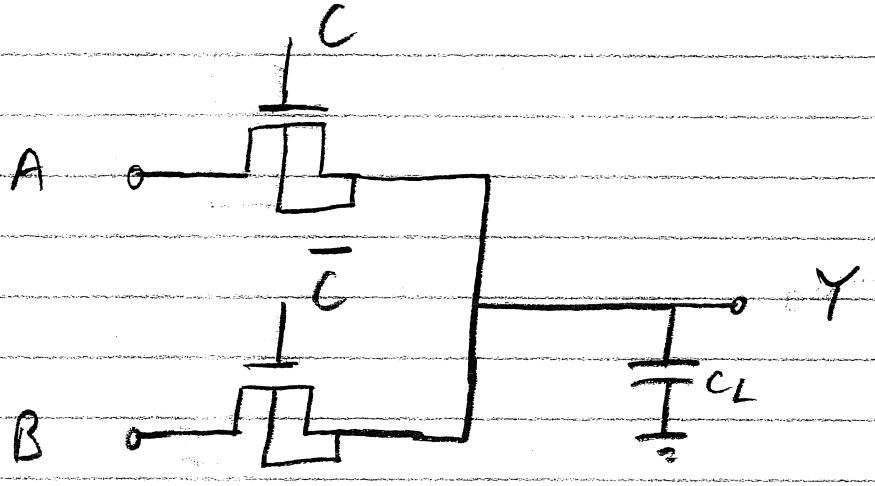
$$V_{tN} = 0.4 + 0.3\left(\sqrt{1.5 + 0.9} - \sqrt{0.9}\right)$$

$$= 0.4 + 0.18$$

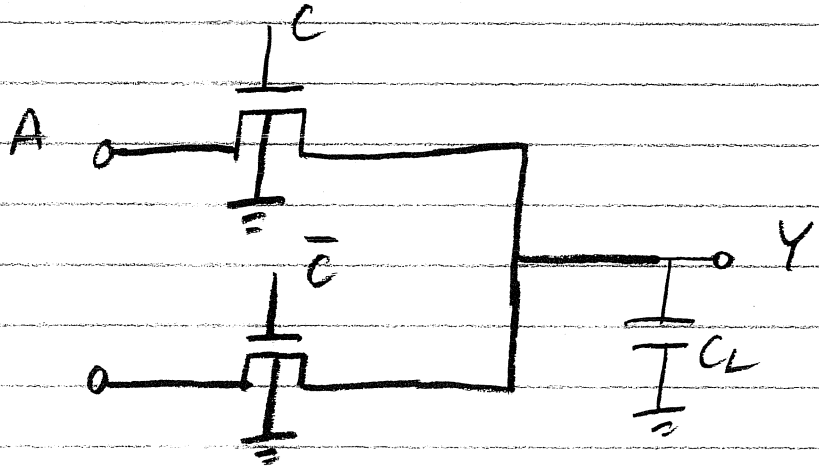
$$= 0.58\ V$$

V_{tN} INCREASES AS V_{SB} INCREASES

PASS TRANSISTOR LOGIC EXAMPLE



CASE I



CASE II

GIVEN $V_{DD} = 2\,V$ $\quad \phi_s = 0.9\,V$

$\gamma = 0.3\,\sqrt{V}$

$V_{tN_0} = 0.4\,V$

FIND V_y MAX FOR CASE I & II

CASE I $\quad C = V_{DD} = 2V$

$A = V_{DD} = 2V \quad V_{SB} = 0$

$V_{tN} = V_{tN_0} = 0.4\,V$

$V_{y\,(MAX)} = V_{DD} - V_{tN} = \underline{1.6\,V}$

CASE II $\quad C = V_{DD} = 2V \quad V_{SB} = V_y - 0 = V_y$

$A = V_{DD} = 2V$

$V_{tN} = V_{tN_0} + \gamma\left(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s}\right)$

$V_{tN} = 0.4 + 0.3\left(\sqrt{V_y + 0.9} - \sqrt{0.9}\right)$

$V_y = V_{DD} - V_{tN}$

$V_y = 2 - \left[0.4 + 0.3\left(\sqrt{V_y + 0.9} - \sqrt{0.9}\right)\right]$ (1)

NON-LINEAR EQUATION

SOLVE BY ITERATION

ESTIMATE $V_{Y1} = 1.6\,V$

FROM RHS OF (1)

$$V_{Y2} = 2 - \left[0.4 + 0.3\left(\sqrt{V_{Y1} + 0.9} - \sqrt{0.9}\right)\right]$$

$$V_{Y2} = 1.41$$

ESTIMATE $V_{Y2} = 1.41\,V$ & USE RHS OF (1) AGAIN

$$\Rightarrow V_{Y3} = 1.43$$

$$\Rightarrow V_{Y4} = 1.43 \quad \underline{\text{DONE}}$$

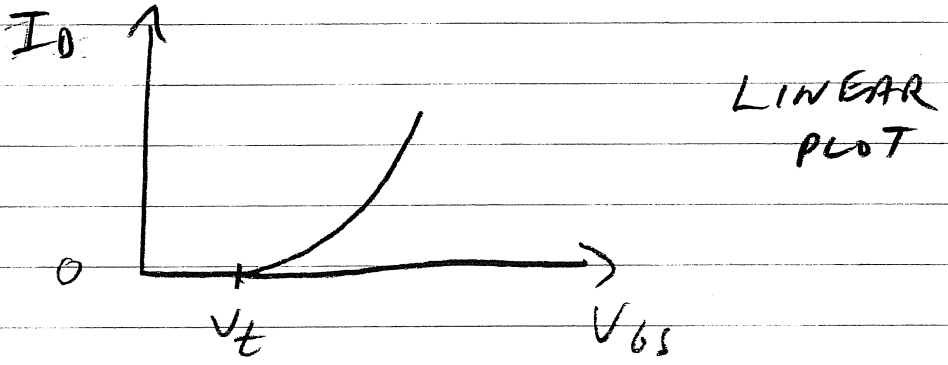
$$V_{Y(MAX)} = \underline{\underline{1.43\,V}}$$

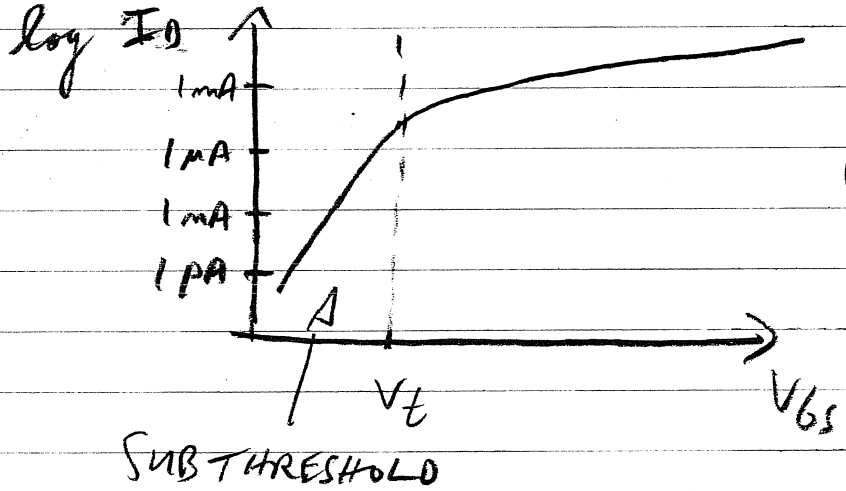
LOWER BY 0.17 V THAN CASE I

4) SUB THRESHOLD CONDUCTION

IDEALLY $I_D = 0$ FOR $V_{GS} < V_t$

(NMOS)





$$I_D = I_{D0} e^{\frac{V_{GS} - V_t}{nV_T}} \left[1 - e^{\frac{-V_{DS}}{V_T}} \right]$$

$I_D = I_{D0}$ WHEN $V_{GS} = V_t$

$$V_T = \frac{kT}{q} \approx 25\,mV \quad \text{AT ROOM TEMP}$$

$n \Rightarrow$ PROCESS DEPENDENT

THE TERM

$$\left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$$

ENSURES $I_D \to 0$ AS $V_{DS} \to 0$

BUT IT IS APPROX 1

WHEN $V_{DS} \gg V_T$ $V_T \approx 25\,mV$ AT ROOM TEMP

EXAMPLE

GIVEN $n = 1.5$ & 1 V CMOS PROCESS

FIND V_t (THRESHOLD) SO THAT

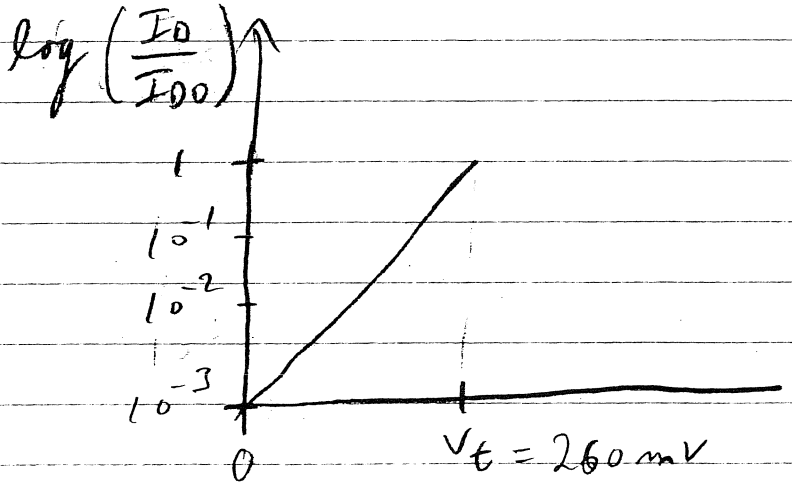
$$I_D @ V_{GS}=0 = \frac{I_D @ V_{GS}=V_t}{1000} \quad \text{WORST CASE}$$

$$I_D @ V_{GS}=0 = I_{D0} e^{\frac{V_{GS}-V_t}{nV_T}} \underbrace{\left(1 - e^{\left(\frac{-1}{25mV}\right)V_{DD}}\right)}_{\approx 1} = \frac{I_{D0}}{1000}$$

$$\frac{1}{1000} = e^{\frac{-V_t}{(1.5)(25mV)}}$$

$$V_t = -(1.5)(25\ mV)(\ln 10^{-3}) = 260\ mV$$

$$\frac{260}{3} \approx 90\ mV/\text{DECADE OF CURRENT}$$



5) JUNCTION LEAKAGE

REVERSE BIASED DIODES LEAK SOME CURRENT

SMALL $I_S \approx 0.1 \rightarrow 0.01\ fA/(\mu m)^2$

INCREASES EXPONENTIALLY WITH INCREASING TEMPERATURE

6) TUNNELING

GATE OXIDES SO THIN, ELECTRONS CAN "JUMP" THROUGH THIN OXIDE.

USED IN EPROM, EEPROM & FLASH MEMORY.

LIMITS GATE OXIDE THICKNESS IN MODERN TECHNOLOGIES

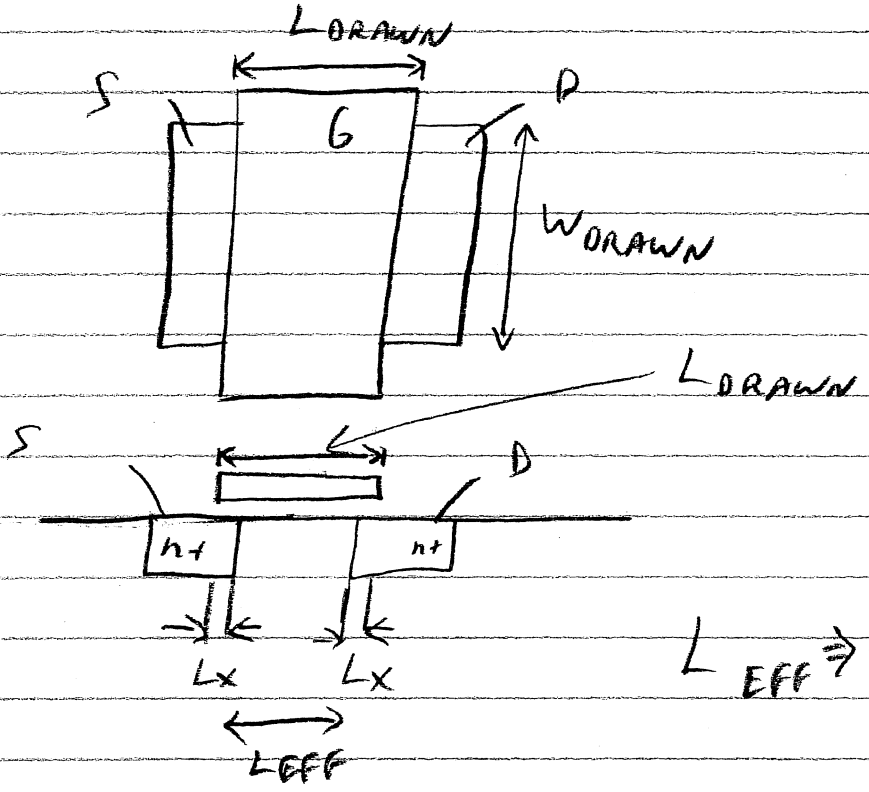
7) TEMPERATURE

- INCREASING TEMP DECREASES MOBILITY OF ELECTRONS & HOLES.
- INCREASING TEMP INCREASES TUNNELING & JUNCTION LEAKAGE
- INCREASING TEMP DECREASES V_t & THEREFORE INCREASES SUBTHRESHOLD CURRENT.
- INCREASED TEMP REDUCES LIFETIME OF DEVICES.
- INCREASE TEMP $\Rightarrow$ WORSE DIGITAL PERFORMANCE

  LIMIT OF $\approx$ 125 °C JUNCTION TEMP

  NEED HEAT SINKS OR FANS.

8) GEOMETRY DEPENDENCE



$L_{EFF} \Rightarrow$ L "EFFECTIVE"

L_{EFF} IS ACTUAL TRANSISTOR LENGTH

$$L_{EFF} = L_{DRAWN} - 2L_x$$

L_{DRAWN} IS WHAT IS SHOWN ON SCHEMATICS AND LAYOUT

L_{EFF} IS WHAT IS ACTUALLY IN TRANSISTORS

SIMILAR FOR W_{EFF}

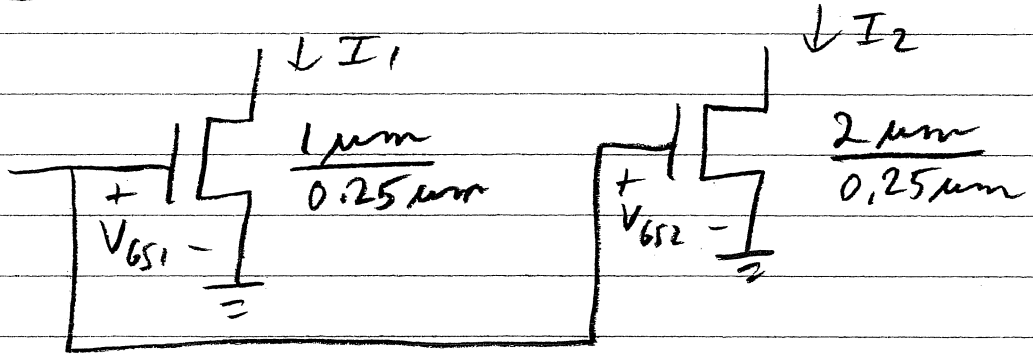
$$W_{EFF} = W_{DRAWN} - 2W_x$$

FOR EXAMPLE, SAY $W_x = 0.1\,\mu m$

$2L_x = 0.05\,\mu m$

AND WANT $I_2 = 2I_1$

FIRST TRY



$V_{GS1} = V_{GS2}$

$W_{EFF_1} = W_{DRAWN_1} - 2W_x$

$= 0.8\,\mu m$

$L_{EFF_1} = L_{DRAWN_1} - 2L_x$

$= 0.2\,\mu m$

$$\frac{W_{EFF1}}{L_{EFF1}} = \frac{0.8}{0.2} = 4$$

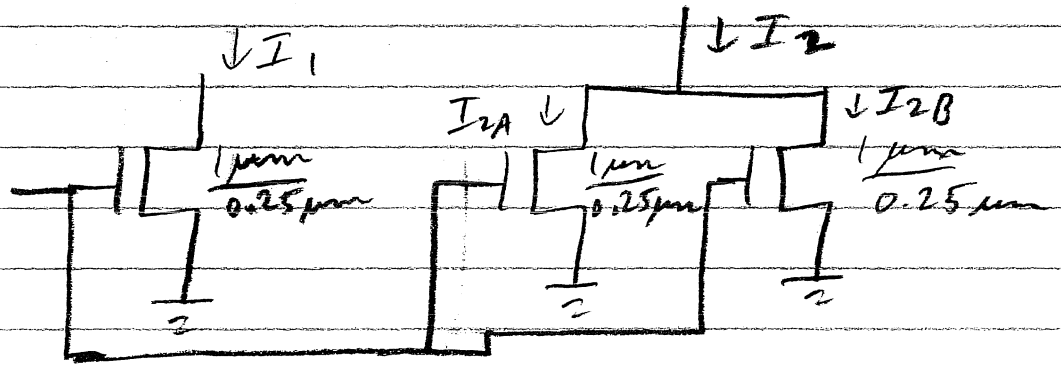
$W_{EFF_2} = W_{DRAWN_2} - 2W_L = 1.8\,\mu m$

$L_{EFF_2} = L_{DRAWN_2} - 2L_X = 0.2\,\mu m$

$$\frac{W_{EFF_2}}{L_{EFF_2}} = \frac{1.8}{0.2} = 9$$

$$\frac{W_{EFF_2}}{L_{EFF_2}} \neq 2\left(\frac{W_{EFF_1}}{L_{EFF_1}}\right) \quad SO \quad I_2 \neq 2I_1$$

BETTER APPROACH



$I_{2A} = I_{2B} = I_1$ SINCE ALL SAME W_{EFF} & L_{EFF}

$I_2 = I_{2A} + I_{2B}$

SO $I_2 = 2I_1$ ✓

THERE STILL EXISTS RANDOM VARIATIONS TO MAKE

$I_2 \neq 2I_1$

BUT SECOND APPROACH IS MUCH BETTER

IN ADDITION, SOME DESIGNS ARE OPTICALLY "SHRUNK" WHERE ALL LENGTHS AND/OR WIDTHS ARE SHRUNK BY FIXED AMOUNTS

THIS IS ANOTHER REASON TO USE SECOND APPROACH.