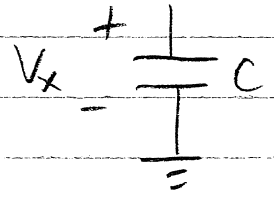
POWER DISSIPATION

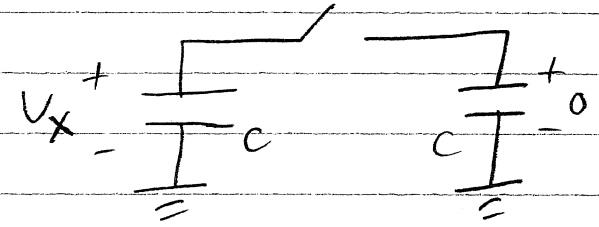
CAPACITORS DO NOT DISSIPATE ENERGY BUT...



ENERGY, $E = \frac{1}{2} C V_x^2$

CHARGE, $Q = C V_x$

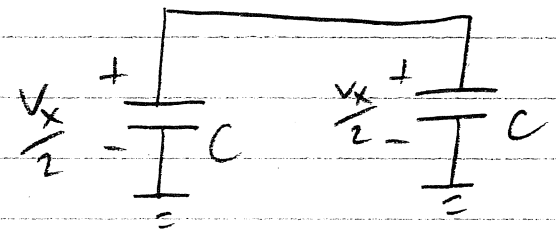
CONSIDER



$E_{TOTAL} = \frac{1}{2} C V_x^2$

$Q_{TOTAL} = C V_x$

CLOSE SWITCH



USING CHARGE CONSERVATION

$Q_{TOTAL} = C\frac{V_x}{2} + C\frac{V_x}{2}$

$= C V_x$ ✓

BUT NOW $E_{TOTAL} = \frac{1}{2}(2C)\left(\frac{V_x}{2}\right)^2 = \frac{1}{4} C V_x^2$

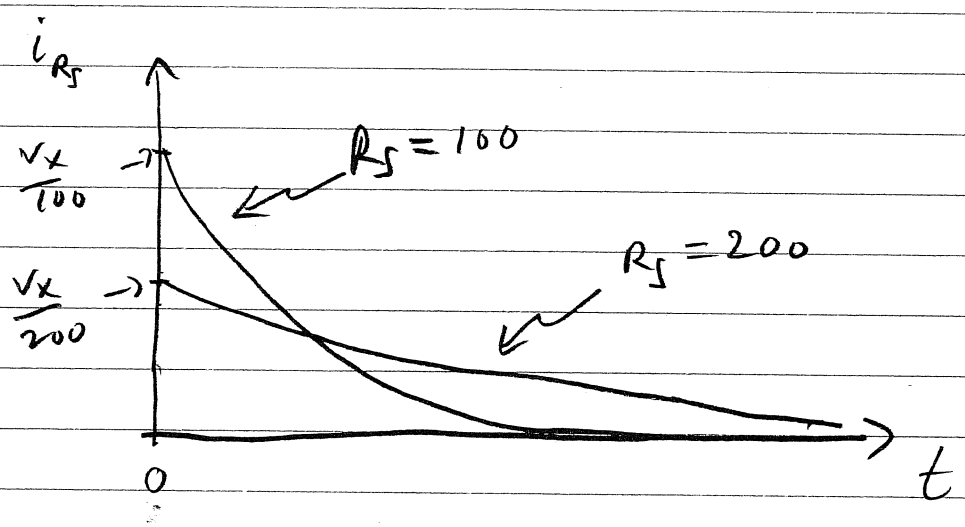
WHERE DID $\frac{1}{4} C V_x^2$ JOULES GO??

ENERGY IS DISSIPATED ACROSS SWITCH RESISTANCE, R_S

IF R_S SMALL THEN CURRENT IS LARGE

BUT FOR SHORT TIME, IF R_S LARGE

CURRENT IS SMALL BUT FOR LONG TIME.



SWITCH CLOSED AT $t = 0$

$$i_{R_S}(0) = \frac{V_x}{R_S} \qquad \tau = R_S \frac{C}{2}$$

SAME ENERGY DISSIPATED INDEPENDENT OF R_S (R_S CAN EVEN BE NON-LINEAR AS IN CASE OF A TRANSISTOR)

POWER DISSIPATION FOR A DIGITAL CHIP CONSISTS OF BOTH

- DYNAMIC POWER ← OCCURS ON TRANSITIONS
- STATIC POWER ← OCCURS EVEN IF HELD HIGH OR LOW

DYNAMIC POWER DISSIPATION

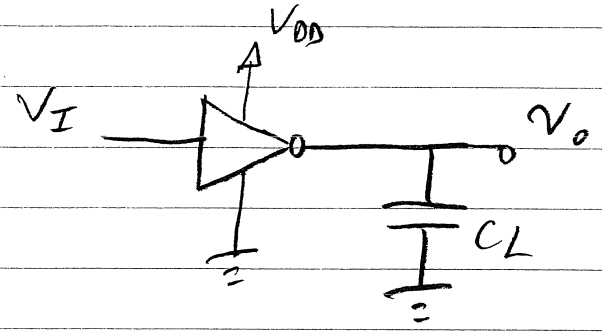
CONSISTS OF BOTH
- CAPACITOR CHARGE/DISCHARGE POWER
- DIRECT PATH POWER

TYPICALLY CAPACITIVE POWER ≈ 80%
DIRECT PATH ≈ 20%

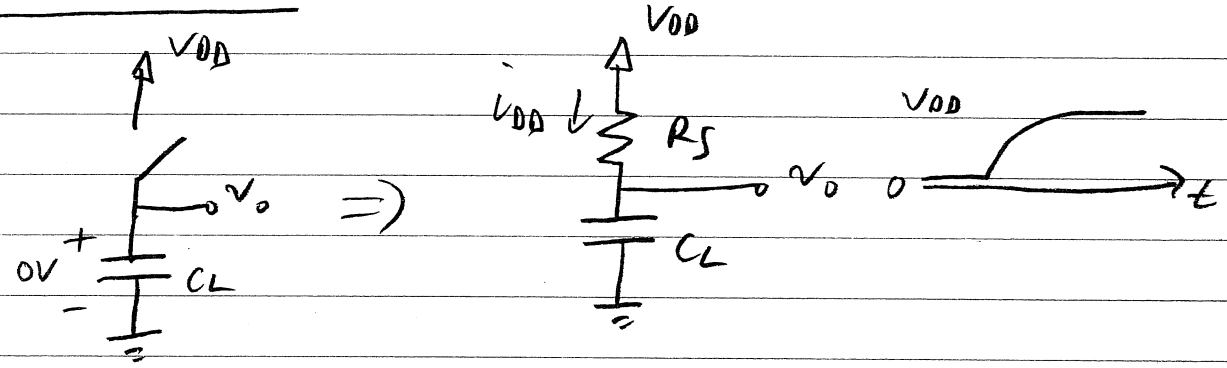
OF DYNAMIC POWER DISSIPATION
BUT SLOW CLOCK/DATA EDGES CAN

INCREASE DIRECT-PATH POWER DISSIPATION.

DYNAMIC CAPACITIVE POWER



LOW TO HIGH



ENERGY DELIVERED FROM V_{DD}, E_{DD}

$$E_{DD} = \int_0^\infty V_{DD}\, i_{DD}\, dt = V_{DD} \int_0^\infty i_{DD}\, dt \quad (1)$$

RECALL $q = CV$ AND $i = \frac{dq}{dt}$.

$$\Rightarrow q = \int i\, dt + \text{CONSTANT}$$

SO ① $\Rightarrow E_{DD} = V_{DD}\, q$

$= V_{DD}\, C_L\, V_{DD} = C_L V_{DD}^2$

SO ENERGY DELIVERED BY V_{DD} EQUALS $C_L V_{DD}^2$

BUT ENERGY STORED ON C_L, E_{CL}

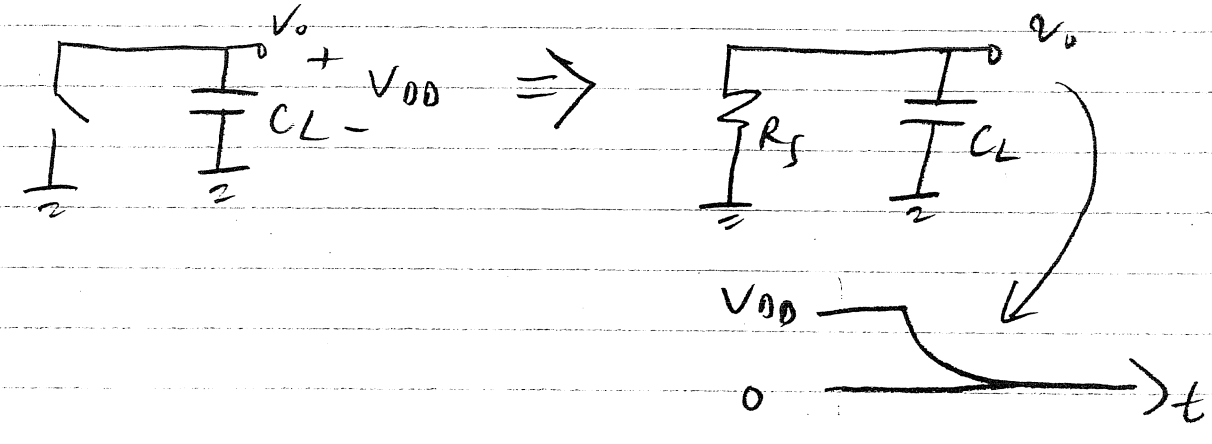
$$E_{CL} = \tfrac{1}{2} C_L V_{DD}^2$$

SO ENERGY DISSIPATED IN RESISTOR R_S

$$E_{DISS} = E_{DD} - E_{CL} = \underline{\underline{\tfrac{1}{2} C_L V_{DD}^2}}$$

INDEPENDENT OF R_S VALUE OR WHETHER IT IS LINEAR OR NOT.

HIGH TO LOW



ENERGY BEFORE IN CAP

$$E_{CL} = \frac{1}{2} C_L V_{DD}^2$$

AFTER $E_{CL} = 0$

$$\Rightarrow E_{DISS} = \frac{1}{2} C_L V_{DD}^2$$

THEREFORE OVER 1 COMPLETE CYCLE

$$E_{DISS} = C_L V_{DD}^2$$

IF f CYCLES PERFORMED EACH SECOND

$$\boxed{P_{DISS} = f C_L V_{DD}^2}$$

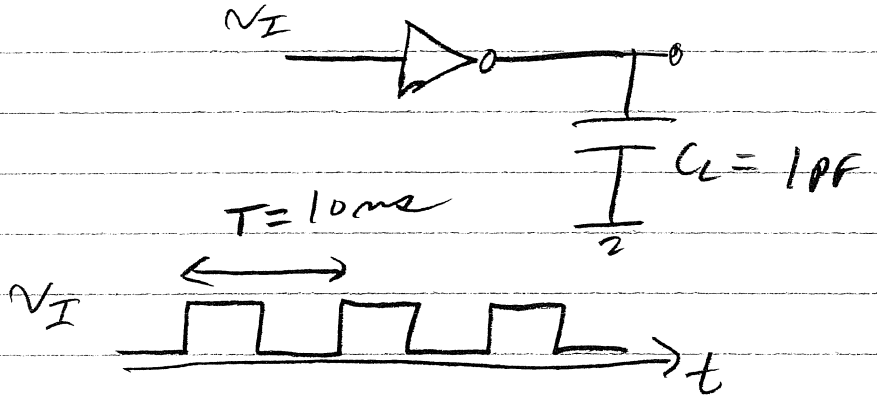
FOR A CLOCK SIGNAL OF FREQ f

HOWEVER FOR A DATA SIGNAL

$$\boxed{P_{DISS} = P_{1\to0} f C_L V_{DD}^2}$$

WHERE $P_{1\to0}$ IS PROBABILITY OF A 1->0 TRANSITION

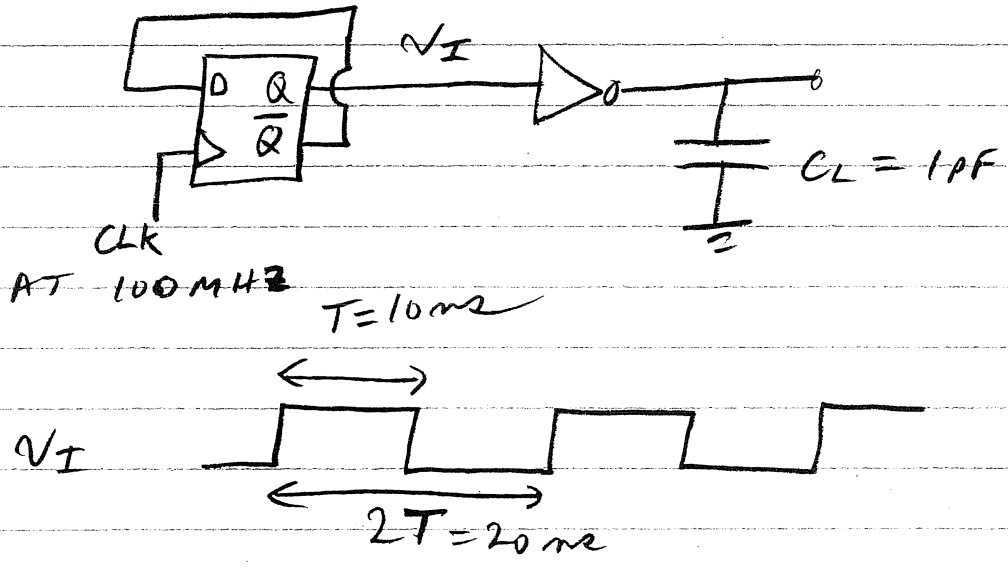
EXAMPLE 1



$$f = \frac{1}{T} = 100\,MHz$$

$$P_{DISS} = (100e6)(1e-12)(3.3^2) = 1.1\,mW$$

EXAMPLE 2



$P_{1\to0}$ AT EACH TRANSITION

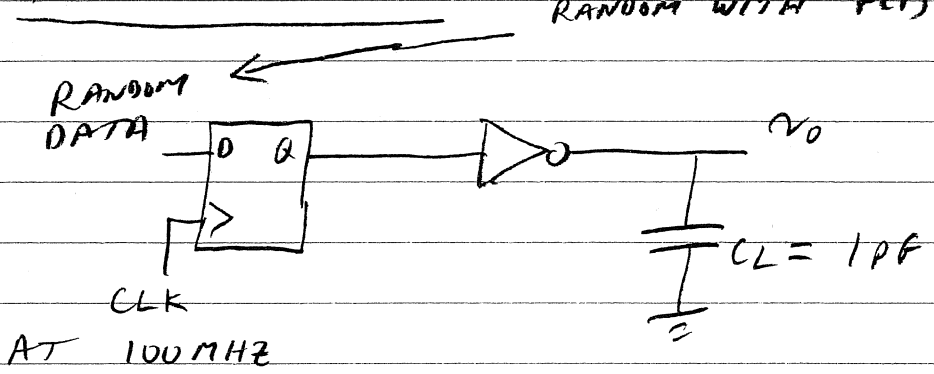
$$P_{1\to0} = 0.5$$

$$P_{DISS} = P_{1\to0}\, f\, C_L\, V_{DD}^2$$

$$= (0.5)(100e6)(1e\text{-}12)(3.3)^2$$

$$= 0.54 \text{ mW}$$

EXAMPLE 3

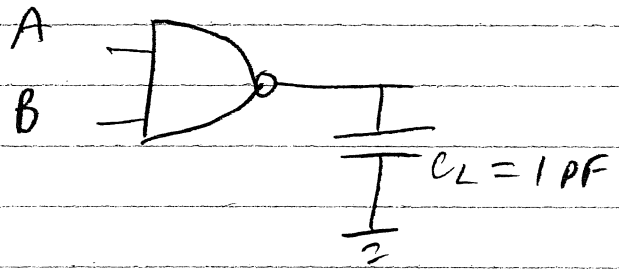


$$P_{1\to0} = P(1)\,P(0) = (0.5)(0.5) = \frac{1}{4}$$

$$P_{DISS} = P_{1\to0}\, f\, C_L\, V_{DD}^2 = \left(\frac{1}{4}\right)(100e6)(1e\text{-}12)(3.3^2)$$

$$= 0.27 \text{ mW}$$

EXAMPLE 4



A, B EACH RANDOM DATA CLOCKED AT 100 MHZ. EACH $P(1) = 0.5$

A	B	V_0
0	0	1
0	1	1
1	0	1
1	1	0

FOR V_0

$P(1) = \frac{3}{4}$

$P(0) = 1 - P(1) = \frac{1}{4}$

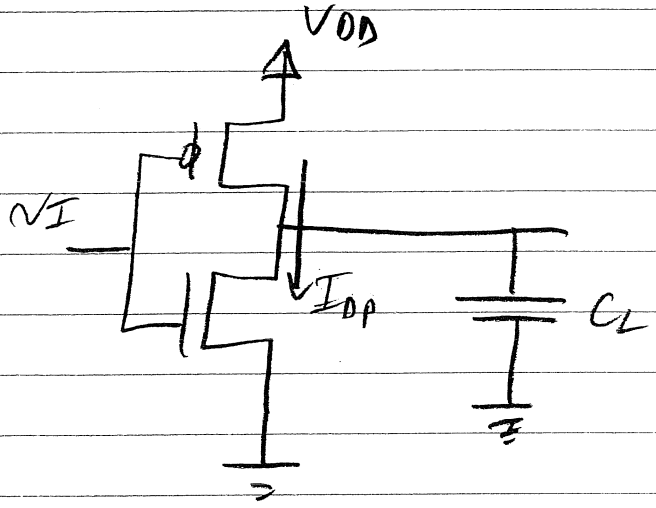
$$P_{1\to0} = P(1)\,P(0) = \left(\frac{3}{4}\right)\left(\frac{1}{4}\right) = \frac{3}{16}$$

$$P_{DISS} = P_{1\to0}\, f\, C_L V_{DD}^2 = \left(\frac{3}{16}\right)(100e6)(1e{-}12)(3.3)^2$$

$$= 0.20 \text{ mW}$$

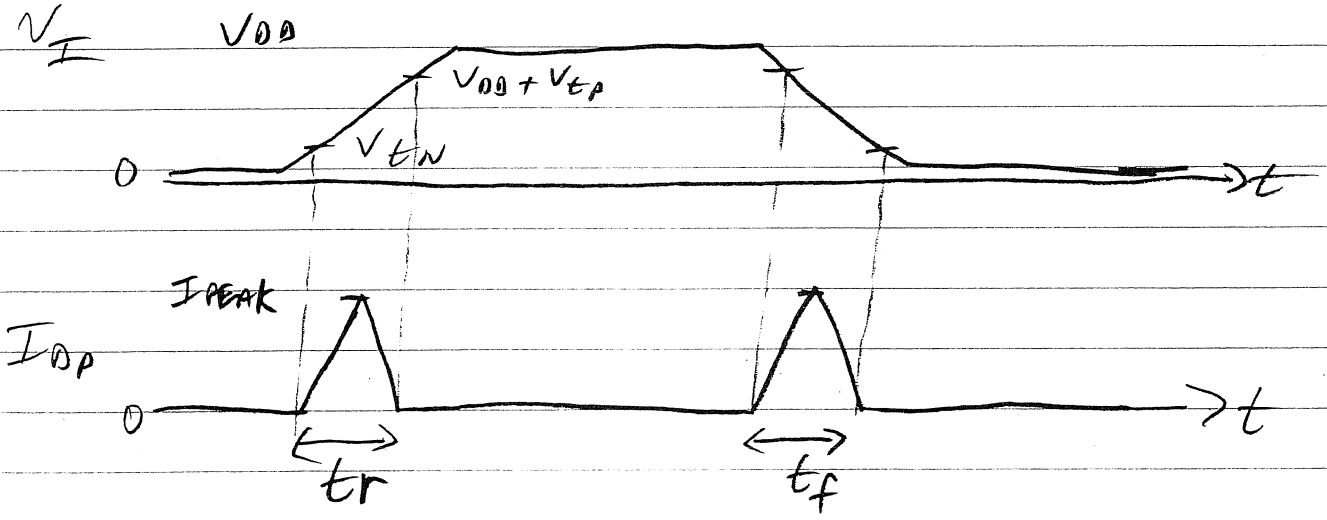
WE ONLY ACCOUND FOR 1->0 TRANSITIONS SINCE EVERY 1->0 TRANSITION IS FOLLOWED BY A 0->1 TRANSITION.

DYNAMIC DIRECT-PATH POWER



I_{DP} IS CURRENT THAT FLOWS DIRECTLY FROM V_{DD} TO GND WHEN BOTH NMOS & PMOS ON AS V_I IS SWITCHING

DOES NOT CHARGE/DISCHARGE C_L



ACTUALLY I_{DP} NOT TRIANGULAR BUT IT IS A GOOD APPROXIMATION.

RECALL V_{TH} IS INVERTER THRESHOLD

$$I_{PEAK} = \frac{\mu_N C_{ox}}{2}\left(\frac{W}{L}\right)_N \left[V_{TH} - V_{tN}\right]^2$$

ENERGY DIRECT PATH, E_{DP}

$$E_{DP} = V_{DD}\left(Q_r + Q_f\right)$$

Q_r / Q_f ARE CHARGE DELIVERED FOR RISING / FALLING EDGES

$$Q_r = I_{AVERGE} \times \Delta t = \frac{I_{PEAK}}{2} t_r$$

$$Q_f = \frac{I_{PEAK}}{2} t_f$$

SO

$$E_{DP} = V_{DD} \frac{I_{PEAK}}{2} \left(t_r + t_f\right)$$

DIRECT PATH POWER DISSIPATION, P_{DP}

$$P_{DP} = V_{DD} \frac{I_{PEAK}}{2} \left(t_r + t_f\right)(f)\left(P_{1\to 0}\right)$$

EXAMPLE

LET P_{DP} => DIRECT PATH POWER DISSIPATION
P_{DYN} => CAPACITIVE " "

$\mu_N C_{ox} = 190\ \mu A/V^2$ $\mu_P C_{ox} = 50\ \mu A/V^2$

$V_{tN} = 0.7V$ $V_{tP} = -0.8V$ $V_{DD} = 3.3V$

INVERTER WITH $\left(\frac{W}{L}\right)_N = \frac{0.7}{0.35}$ $\left(\frac{W}{L}\right)_P = \frac{1.4}{0.35}$

ASSUME $t_r \cong t_{dr}$ & $t_f \cong t_{df}$

FIND RATIO OF $\frac{P_{DP}}{P_{DYN}}$

$$\frac{P_{DP}}{P_{DYN}} = \frac{\left(V_{DD}\right)\left(\frac{I_{PEAK}}{2}\right)\left(t_r + t_f\right)\left(f\right)\left(P_{1\to 0}\right)}{P_{1\to 0}\, f\, C_L\, V_{DD}^2}$$

$$= \frac{\left(\frac{I_{PEAK}}{2}\right)\left(1.2\, C_L\right)\left(R_{EQN} + R_{EQP}\right)}{C_L\, V_{DD}}$$

TO FIND I_{PEAK}, FIRST FIND V_{TH}

$$V_{TH} = \frac{V_{DD} + V_{tp} + V_{tN}\, r}{1 + r} \qquad r = \sqrt{\frac{\mu_N \left(\frac{W}{L}\right)_N}{\mu_P \left(\frac{W}{L}\right)_P}}$$

$$= 1.46\ V$$

$$I_{PEAK} = \frac{\mu_N C_{ox}}{2} \left(\frac{W}{L}\right)_N \left(V_{TH} - V_{tN}\right)^2$$

$$= \left(\frac{190e\text{-}6}{2}\right)(2)\left(1.46 - 0.7\right)^2 = 109.7\,\mu A$$

$$R_{EQN} = \frac{2.5}{\mu_N C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{tN})} = 2.53k$$

$$R_{EQP} = \frac{2.5}{\mu_P C_{ox} \left(\frac{W}{L}\right)_P (V_{DD} + V_{tP})} = 5k$$

$$\frac{P_{DP}}{P_{DYN}} = \frac{\left(\frac{109.7e\text{-}6}{2}\right)(1.2)(2.53k + 5k)}{3.3}$$

$$= 0.15 \quad OR \quad \underline{\underline{15\%}}$$

STATIC POWER DISSIPATION

POWER DISSIPATION WHEN LOGIC IS NOT SWITCHING.

IN CMOS, DUE TO

1) SUBTHRESHOLD CURRENT

2) GATE LEAKAGE

3) REVERSE BIAS JUNCTION LEAKAGE

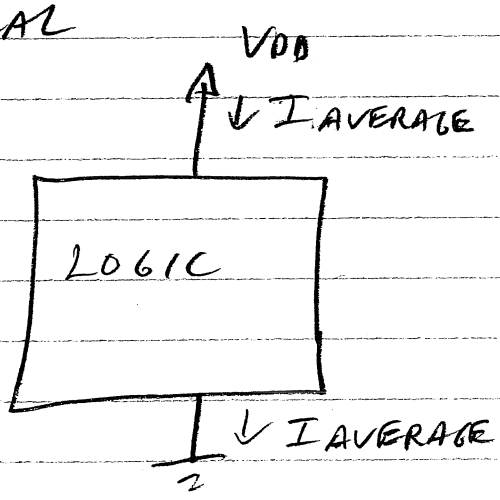
SUBTHRESHOLD CURRENT GENERALLY DOMINATES IN ADVANCED PROCESSES (130nm OR LESS)

GATE LEAKAGE IS NEXT WITH REVERSE BIAS JUNCTIONS BEING LOWEST AMOUNT

IN OLDER TECHNOLOGIES, REVERSE BIAS JUNCTIONS DOMINATE.

IN PSEUDO NMOS, STATIC POWER DISSIPATION IS HIGH WHEN OUTPUT IS LOW BUT NEAR ZERO WHEN OUTPUT IS HIGH

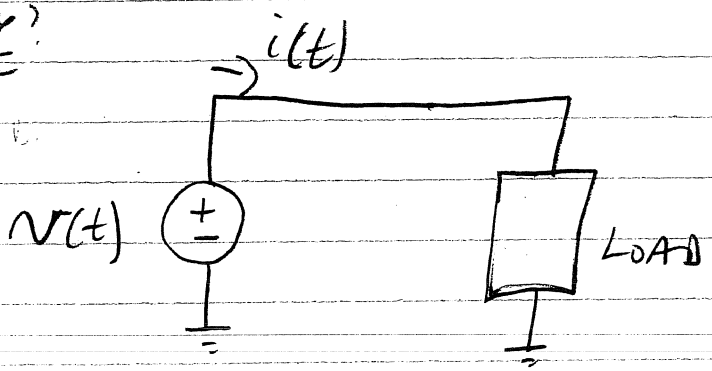
IN GENERAL



$$P_{DISS} = V_{DD}\ I_{AVERAGE}$$

(NOT I_{RMS})

WHY?



POWER DISSIPATED IN LOAD

$$P_{DISS} = \lim_{T\to\infty} \frac{1}{T} \int_0^T v(t)\, i(t)\, dt$$

IF $v(t) = V_{DD}$ (A FIXED DC VALUE)

$$P_{DISS} = \lim_{T\to\infty} \frac{1}{T} \int_0^T V_{DD}\, i(t)\, dt$$

$$P_{DISS} = V_{DD} \lim_{T\to\infty} \frac{1}{T} \int_0^T i(t)\,dt$$

$$P_{DISS} = V_{DD}\, I_{AVERAGE}$$

WHERE $$I_{AVERAGE} \equiv \lim_{T\to\infty} \frac{1}{T} \int_0^T i(t)\,dt$$

ASIDE

RMS IS USEFUL WHEN LOAD IS PURELY RESISTIVE $\Rightarrow$ LOAD = R

$$v(t) = i(t)\,R$$

$$P_{DISS} = \lim_{T\to\infty} \int_0^T R\, i^2(t)\,dt = R \lim_{T\to\infty} \int_0^T i^2(t)\,dt$$

$$= I_{RMS}^2\, R \quad \text{WHERE} \quad I_{RMS}^2 \equiv \lim_{T\to\infty} \int_0^T i^2(t)\,dt$$

SAME POWER AS A dc CURRENT OF I_{RMS} APPLIED TO RESISTOR

CAN ALSO USE RMS WITH POWER FACTORS FOR COMPLEX IMPEDANCE LOADS