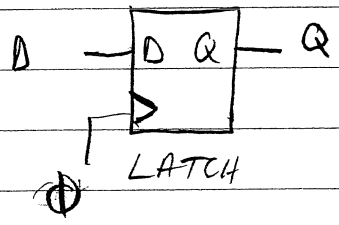
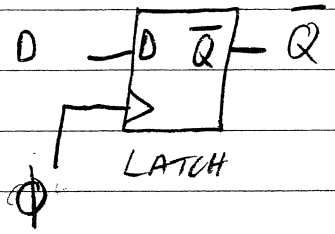
LATCH/REGISTER CIRCUITS

LATCHES

RECALL



OR



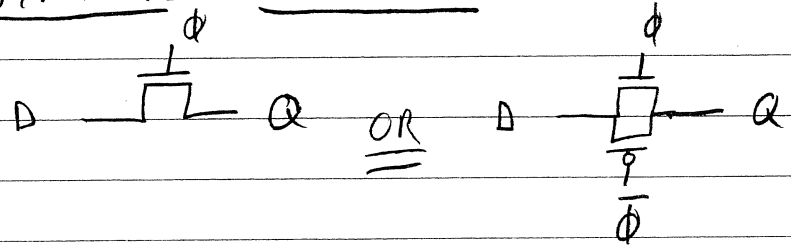
$\phi = 1 \quad Q = D$

$\phi = 0 \quad Q$ HELD

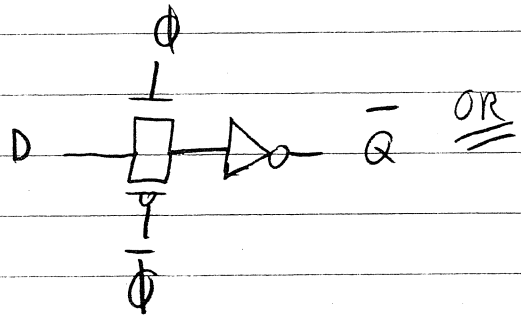
$\phi = 1 \quad \bar{Q} = \bar{D}$

$\phi = 0 \quad \bar{Q}$ HELD

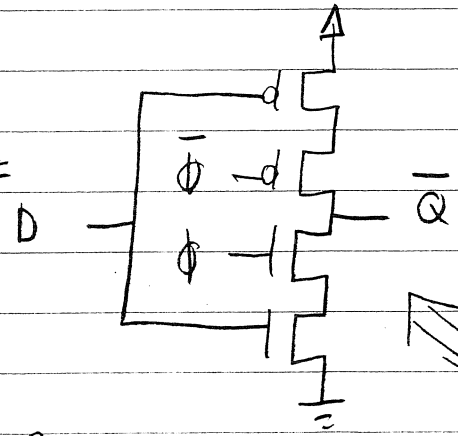
DYNAMIC LATCHES



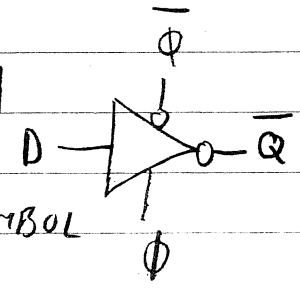
NON-INVERTING



OR



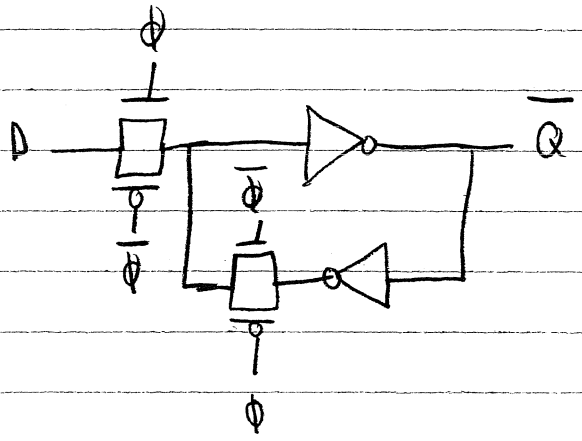
INVERTING



C^2MOS LATCH (CLOCKED CMOS)

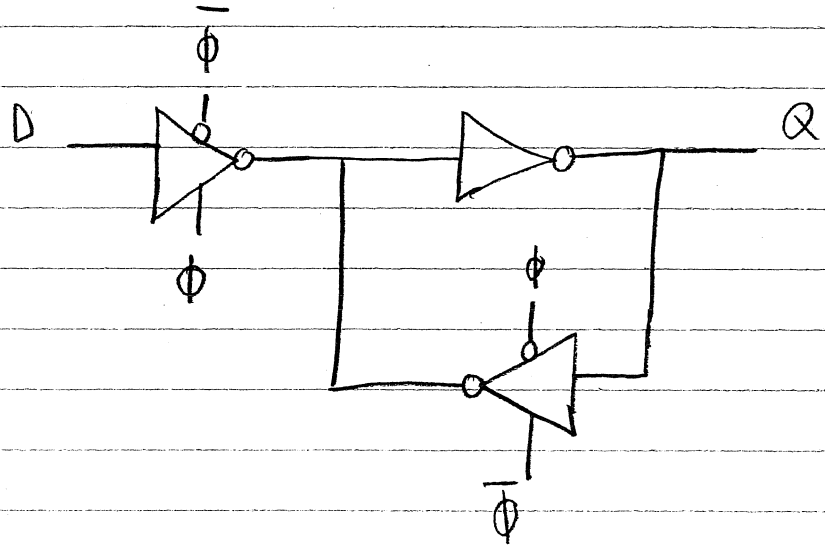
SYMBOL

STATIC LATCHES



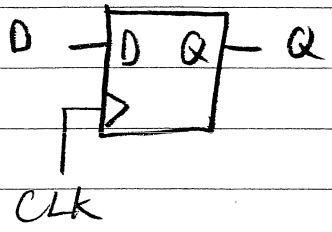
T-GATE LATCH

OR



C^2MOS STATIC LATCH

REGISTERS

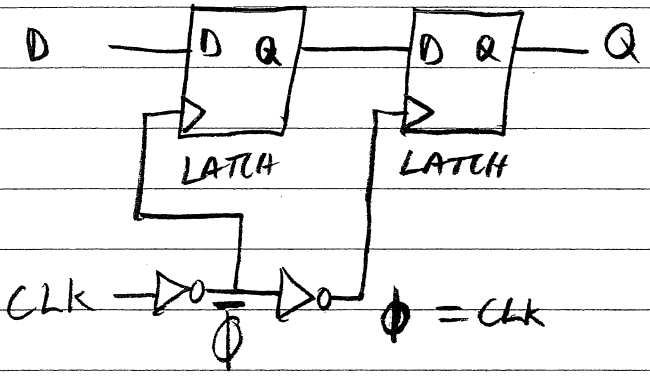


CLK ↑ Q = D

CLK = 0 Q HELD

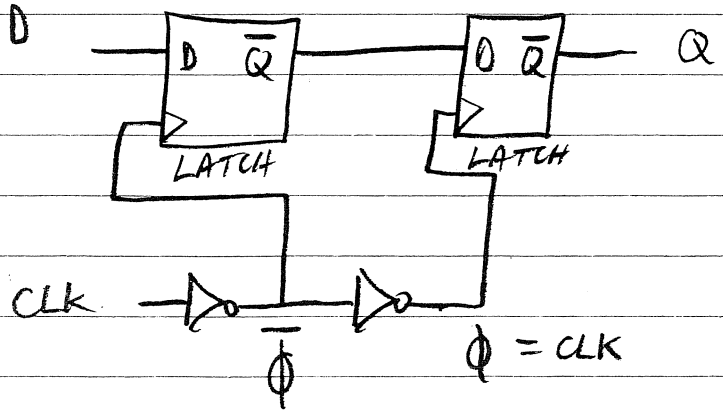
CLK = 1 Q HELD

CLK ⇒ ↓ Q HELD



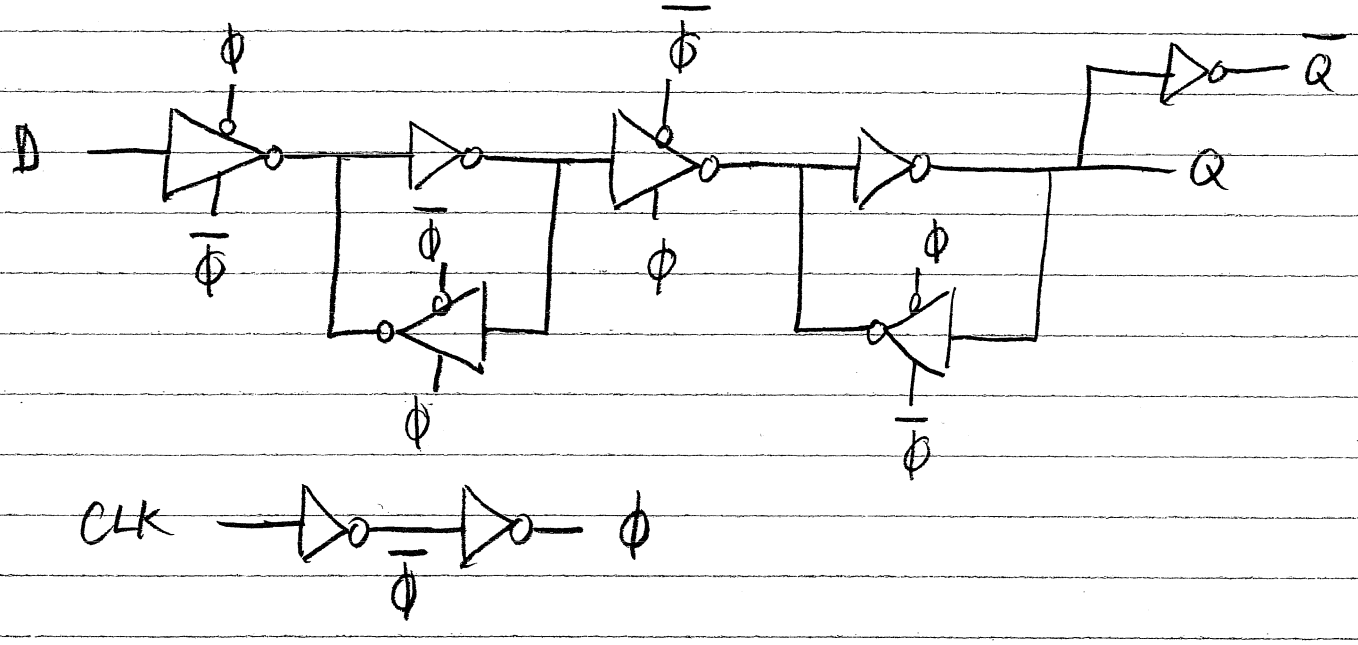
NON-INVERTING LATCHES

OR



INVERTING LATCHES

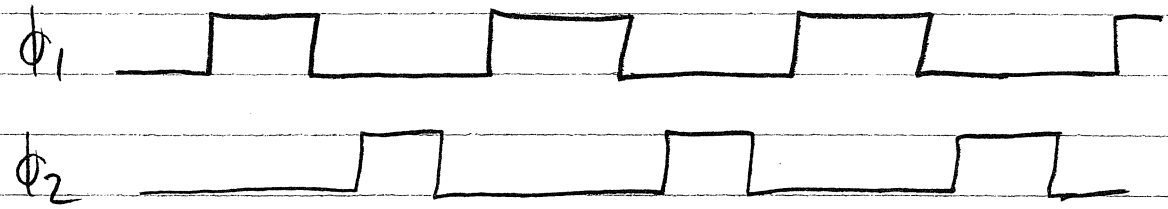
Ex REGISTER USING C^2MOS STATIC LATCHES



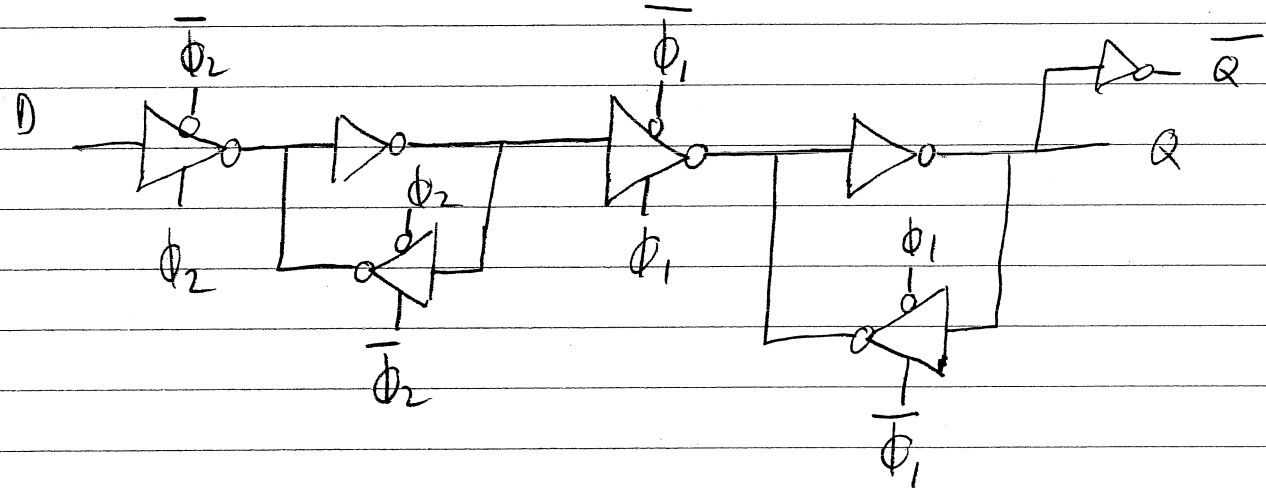
IF CONCERNS ABOUT RACE CONDITIONS

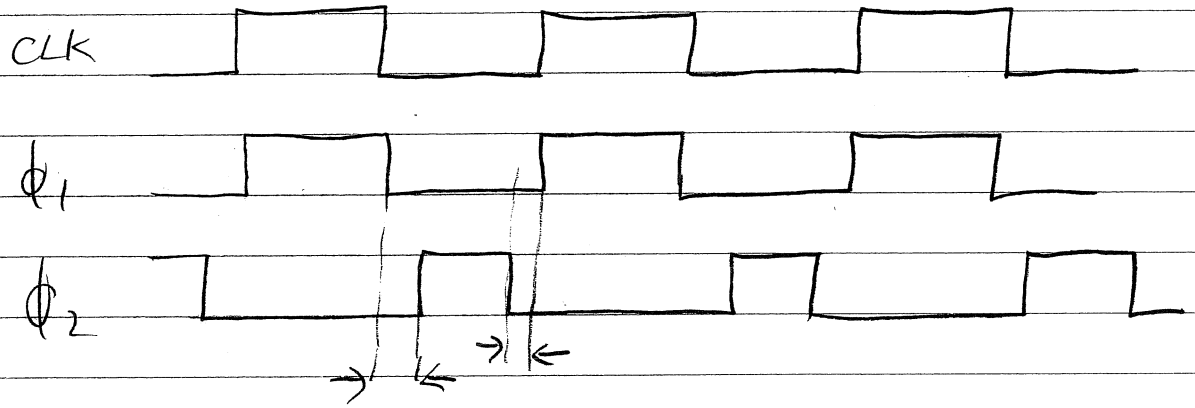
CAN USE NON-OVERLAPPING CLOCKS

ϕ_1, ϕ_2 (AND $\bar{\phi}_1, \bar{\phi}_2$)

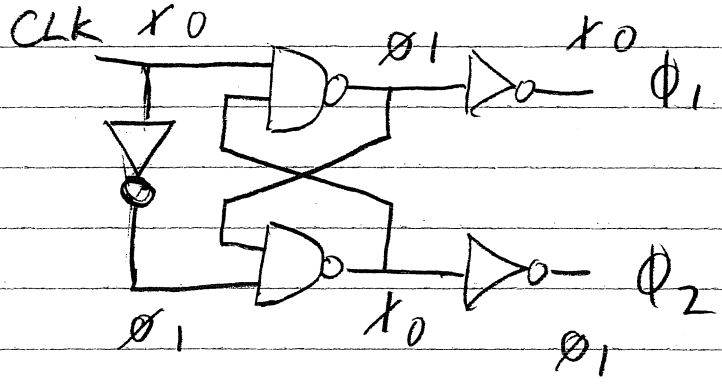


REGISTER WITH NON-OVERLAPPING CLOCKS





NON-OVERLAPPING CLOCK GENERATOR



RESETTABLE REGISTERS

- NORMALLY USE <u>CLOCKED</u> "RESETS" OR "SETS" SO NO ASYNCHRONOUS PROBLEMS TO DEAL WITH