University of Toronto

Final Exam

Date - Apr 15, 2010

Duration: 2.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet shown on last page.

2. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Student #: _____

Last Name: _____

First Name: _____

Question	Mark
1	
2	
3	
4	
5	
6	
7	
Total	

(max grade = 42)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T F Bitline twists in SRAM memory are used to increase the size of the differential signal seen at the sense amplifiers

T F In an SRAM memory, isolation transistors between the sense amplifier and BL and $\overline{BL}$ are used to amplify the read signal from the memory cell.

T F The PMOS transistors in SRAM memory cells are sometimes replaced by $1\,G\Omega$ resistors to reduce memory cell size without affecting speed.

T F To transmit an N-bit data word across 2 clock domains, N synchonizers are used to reduce metastability.

T F For a synchronous system, the minimum clock period is related to the setup time, the maximum clock-to-Q time and the maximum logic delay time.

T F For a synchronous system, the maximum clock period is related to the hold-time, the minimum clock-to-Q time and the minimum logic delay time.

T F The use of non-overlapping clocks within registers helps with meeting setup time constraints.

T F The use of non-overlapping clocks within registers helps with possible race conditions.

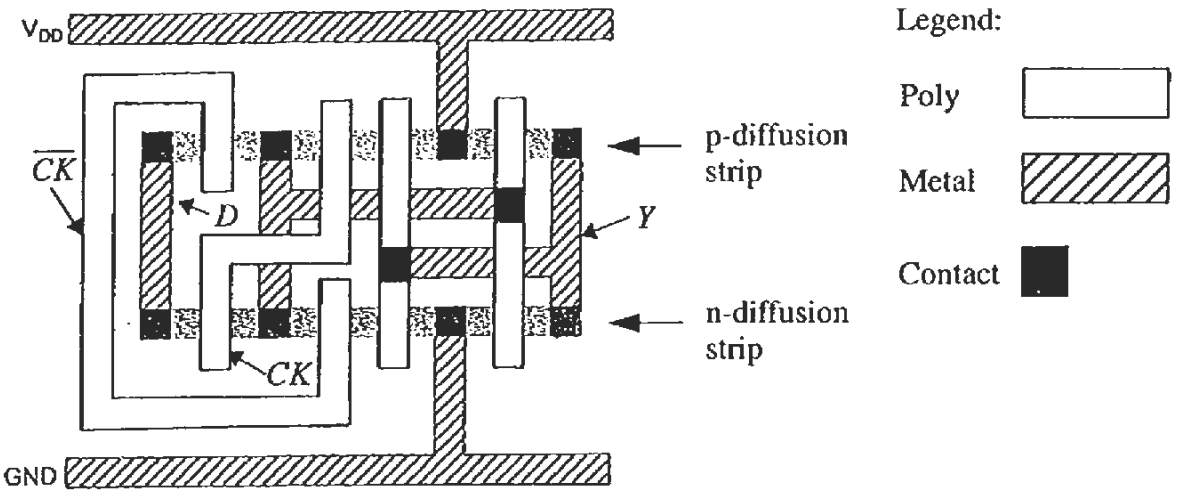
T F C^2MOS latches are built using transmission gates.

T F C^2MOS latches are built using clocked tri-state inverters.

T F For domino logic, unfooted gates must be used when the inputs come from CMOS logic.

T F CVSL (cascode voltage switch logic) built with ideal transistors does NOT have zero static power dissipation.

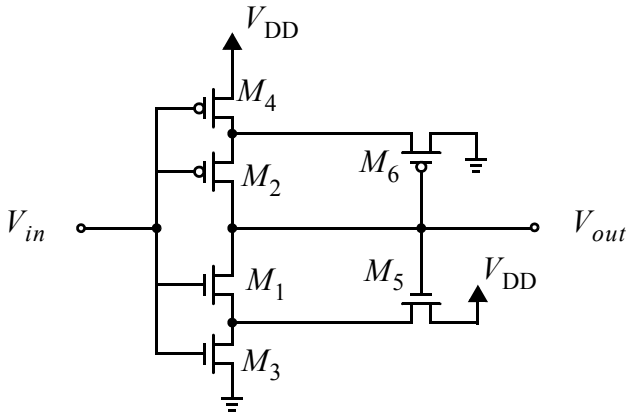
[6] Question 2: In the layout diagram shown below, Y is the output node while D, CK and $\overline{CK}$ are inputs.



a) Draw a schematic for the above layout. What function does this circuit perform?.

b) When connecting to p- substrate, p+ is inserted between the metal and p-. Explain why this is done and what would happen if metal were directly connected to p-.

[6] Question 3: Consider the Schmitt trigger below. All transistors have minimum channel length and transistor relative widths are shown. Derive an expression for the switching threshold as V_{in} is increased from 0V. Ignore the body effect.



$$W_1 = W_3 = 4W_5$$
$$W_2 = W_4 = 4W_6$$

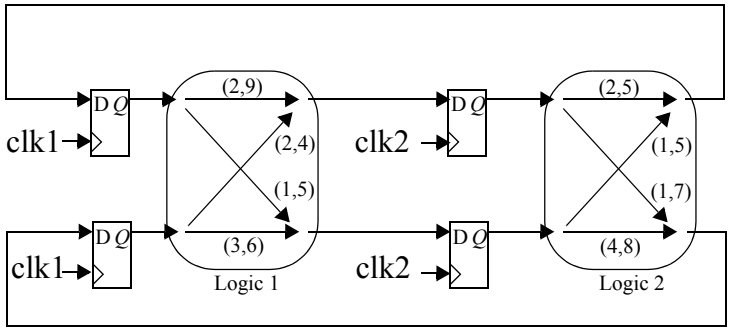
[6] Question 4: Without showing transistor sizes, show transistor schematics for the following circuits:

a) A 3 input nand gate in dual-rail footed domino logic.

b) An inverting 1V to 3V level translator where both low voltage and high voltage transistors are available. Indicate which transistors are high voltage and which are low voltage.

c) An inverting 3V to 1V level translator where both low voltage and high voltage transistors are available. Indicate which transistors are high voltage and which are low voltage.

[6] Question 5: In Logic Block 1 and Logic Block 2, the notation for the total gate delay in each logic path is (min-delay, max-delay). The delay time is in units of nano-seconds.



The above synchonous system has the following register specs: $(t_{ccq}, t_{pcq}) = (0.5, 2)$ and $t_{setup} = 1$, $t_{hold} = 1$.

a) Assuming clk1 and clk2 have the same exact frequency and phase, determine the minimum T_{cycle} for this system ($T_{cycle} = 1/\text{clock freq}$)

b) Determine the maximum clock skew, $|T_{skew}|$, between clk1 and clk2 that can be tolerated so that a race condition does not occur.

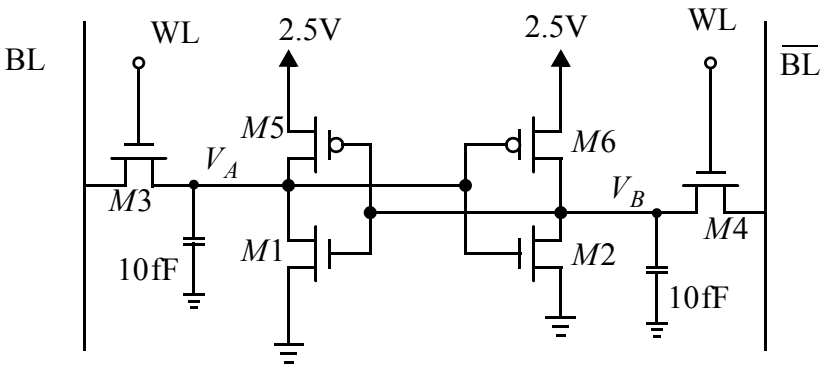
[6] Question 6: Consider the case where a logic signal needs to cross from clock domain 1 to clock domain 2 asynchronously.

a) Explain the error that can occur if a register is NOT used as the final stage of clock domain 1

b) What is the equation for the MTBF if only a single register is used as the synchonizer in clock domain 2.

c) Due to the challenges of asychronous signals, it is desirable to have registers with synchronous resets. Show how to modify a simple register so that it has a synchronous reset.

[6] Question 7: Consider an SRAM cell shown below where BL and $\overline{\text{BL}}$ are both precharged to $V_{DD} = 2.5\text{V}$ during a read operation.



all lengths = 0.25um

$W_1 = 1.0\text{um}$

$W_3 = 0.5\text{um}$

$W_5 = 0.5\text{um}$

$\mu_n C_{ox} = 120\ \mu A/V^2$

$\mu_p C_{ox} = 30\ \mu A/V^2$

$V_{tn} = -V_{tp} = 0.4\ \text{V}$

$C_{ox} = 6\ \text{fF}/\mu\text{m}^2$

a) Estimate the peak voltage at V_A during a read operation when the cell stores a "one" at V_B.

b) Assuming this SRAM cell is one of 512 x 512 array, estimate the word line capacitance for a single row. Ignore any wiring capacitance.

(blank sheet for scratch calculations)

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}\,\mathrm{JK}^{-1}$; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26\,\mathrm{mV}$ at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0} e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to 0} f C_L V_{DD}^2$; $P_{dp} = 0.5 P_{1\to 0} f V_{DD} I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_{\square} = \rho/t$; $C = (\varepsilon_{ox} wl)/t$; $C = \varepsilon_{ox} l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;

Max delay constraint: $T_c \geq t_{pcq} + t_{pd} + t_{setup}$ **Min Delay constraint:** $t_{hold} \leq t_{ccq} + t_{cd}$ **Metastability:** $\mathrm{MTBF} = e^{T/\tau_s}/(t_{rd} F_D F_{CLK})$

SRAM: M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,

SRAM read: $W_1/W_3 \geq (V_{DD} - V_A - V_{tn})^2/(2((V_{DD} - V_{tn})V_A - V_A^2/2))$; $I_{cell} = ((\mu_n C_{ox})/2)(W_3/L)(V_{DD} - 2V_{tn})^2$
$\Delta V_{BL} = (I_{cell}\Delta t)/C_{BL}$

SRAM write: $W_3/W_5 \geq (\mu_p(V_{DD} + V_{tp})^2)/(2\mu_n((V_{DD} - V_{tn})V_A - V_A^2/2))$