University of Toronto

Final Exam

Date - Apr 18, 2011

Duration: 2.5 hrs

ECE334 — Digital Electronics
Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Calculator type unrestricted
3. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
6	
Total	

(max grade = 36)

Last Name: ______________________

First Name: ______________________

Student #: ______________________

[6] Question 1: Each correct answer is worth 0.5 marks.

For the questions below, circle one of True [T] or False [F].

T F In the 1970's and 1980's, CMOS digital circuits became more popular than bipolar digital circuits due to their higher speed.

T F Two ways to add dopants to a silicon substrate are ion implantation and injection.

T F For the detailed MOS gate capacitance model, the gate-bulk capacitance is 0 when the transistor is in triode.

T F Channel length modulation of digital circuits is important as it reduces the speed of digital circuits.

T F Elmore delay is not necessarily accurate in absolute prediction of an RC tree delay but if one minimizes the Elmore delay, generally, the RC tree delay is also minimized.

T F Since dynamic gates precharge high then fall low during evaluation, a dynamic bus will never see twice the crosstalk capacitance due opposite switching during evaluation.

T F It is not possible to make a symmetric CMOS 3-input nand gate.

T F Most flash memory is built as NOR memory architecture.

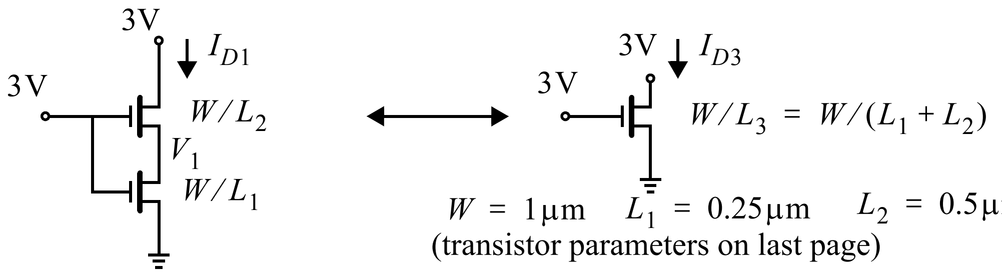
T F Hot carrier injection is a self-limiting mechanism when putting electrons on a floating gate.

T F A DRAM memory cell should be refreshed after every read of that cell.

T F The pmos transistors in a SRAM memory cell generally do not affect read or write speed.

T F Bitline twists are used in SRAM memory to reduce capacitance coupling and therefore increase memory speed.

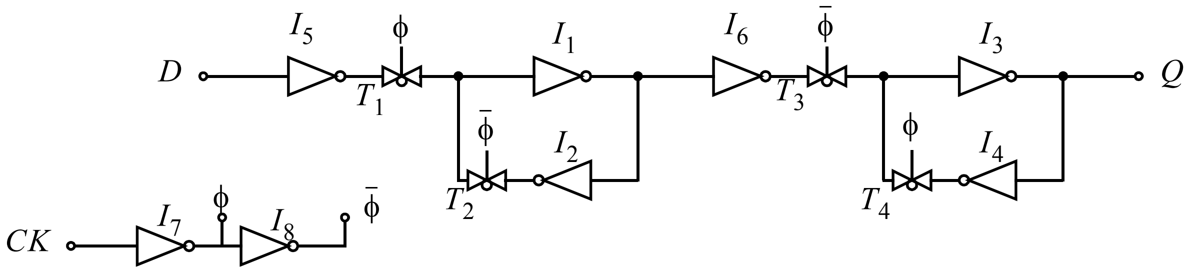
[6] Question 2: Transistor equivalency says that that 2 transistors in series having the same width is equivalent to a single transistor with that width and the lengths added together as shown below. For the case below (voltage, width and lengths shown), show that this is indeed true (**not using transistor equivalency**) by finding I_{D1} and I_{D3} and also find V_1. (Ignore body effect and finite output impedance).



$W = 1\mu m \quad L_1 = 0.25\mu m \quad L_2 = 0.5\mu m$

(transistor parameters on last page)

[6] Question 3: Consider the "d" register shown below.



Assuming that each T-gate turns on/off according to it controlling signal edge, and defining the following delays:

T_{I_i} is the delay through the i 'th inverter

T_{G_i} is the delay through the i 'thT-gate from its control input to its output

T_{T_i} is the delay through the i 'thT-gate from its "data" input to its output

a) Find T_{setup} in terms of T_{I_i}, T_{G_i} and T_{T_i} (be specific in terms of i).

b) Find T_{pcq} in terms of T_{I_i}, T_{G_i} and T_{T_i} (be specific in terms of i).

[6] Question 4:

a) Explain why when a single logic signal is crossing from clock domain 1 to clock domain 2, the last logic element in clock domain 1 should be a register. Give an example where an error occurs if the last element is NOT a register. (Show a timing diagram in your example).

b) A 3-register synchronizer (1 register in clock domain 1 and 3 registers in clock domain 2) uses registers with $\tau_s = 500\text{ps}$ and $t_{\text{rd}} = 200\text{ps}$. Assuming the input toggles at 10MHz, what is the minium clock period for which the mean time between failures is 1000 years? (Your clock period answer only needs to be accurate to 20%).

[6] Question 5: A single CMOS inverter is sized with minimum transistor lengths of 0.25um, NMOS width of 1um and PMOS width of 2um. This inverter is driving a fixed capacitive load of 50fF. However, the output wire of the inverter also has 50fF capacitive coupling to another signalling wire which may or may not switch when the inverter switches. Estimate the fastest delay (either t_{dr} or t_{df}) and slowest delay (either t_{dr} or t_{df}) through the inverter taking into account the adjacent signalling wire. Use parameters on last page.

[6] Question 6:

a) An embedded SRAM contains 8192 8-bit words. If it is physically arranged in a square fashion, how many bits will be used in the row decode and how many bits will be used in the column decode? (assume the cell aspect ratio is square).

b) A dynamic memory cell has a worst case leakage current of 2nA (independent of voltage) and is refreshed every $100\mu s$. If the power supply is 3V and the cell voltage should not leak lower than 1.8V, find the required cell capacitance value.

c) In a DRAM memory, the sense amps are connected directly to the bit lines. In a SRAM memory, the sense amps are connected to the bit lines through 2 isolation PMOS transistors. Explain why the isolation transistors are needed in an SRAM. Also, explain why the isolation transistors should NOT be used in a DRAM.

(blank sheet for scratch calculations)

Last Name: ________________

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}$ JK^{-1} ; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26$mV at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0}e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min}; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to0}fC_L V_{DD}^2$; $P_{dp} = 0.5P_{1\to0}fV_{DD}I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_\square = \rho/t$; $C = (\varepsilon_{ox}wl)/t$; $C = \varepsilon_{ox}l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;

Max delay constraint: $T_c \geq t_{pcq} + t_{pd} + t_{setup}$ **Min Delay constraint:** $t_{hold} \leq t_{ccq} + t_{cd}$ **Metastability:** $\text{MTBF} = e^{T/\tau_s}/(t_{rd}F_D F_{CLK})$

SRAM: M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,

SRAM read: $W_1/W_3 \geq (V_{DD} - V_A - V_{tn})^2/(2((V_{DD} - V_{tn})V_A - V_A^2/2))$; $I_{cell} = ((\mu_n C_{ox})/2)(W_3/L)(V_{DD} - 2V_{tn})^2$
$\Delta V_{BL} = (I_{cell}\Delta t)/C_{BL}$

SRAM write: $W_3/W_5 \geq (\mu_p(V_{DD} + V_{tp})^2)/(2\mu_n((V_{DD} - V_{tn})V_A - V_A^2/2))$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9$V

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	0.3
PMOS	-0.4	0.4	30	0.1	6	0.3	2	0.3

V_{T0} is the threshold voltage with zero bulk-source voltage; γ is used to account for non-zero bulk-source voltage; μC_{ox} is the transistor current gain parameter; λ is to account for the transistor finite output impedance (channel length modulation); C_{ox} is the gate capacitance per unit area; C_o is the gate overlap capacitance per unit length; C_j is the drain/source junction capacitance per unit area; C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters