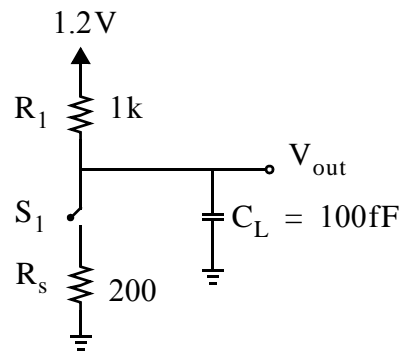


2.9 An nMOS transistor has a threshold voltage of 0.4 V and a supply voltage of  $V_{DD} = 1.2$  V. A circuit designer is evaluating a proposal to reduce  $V_t$  by 100 mV to obtain faster transistors.

- By what factor would the saturation current increase (at  $V_{gs} = V_{ds} = V_{DD}$ ) if the transistor were ideal?
- By what factor would the subthreshold leakage current increase at room temperature at  $V_{gs} = 0$ ? Assume  $n = 1.4$ .
- By what factor would the subthreshold leakage current increase at 120° C? Assume the threshold voltage is independent of temperature.

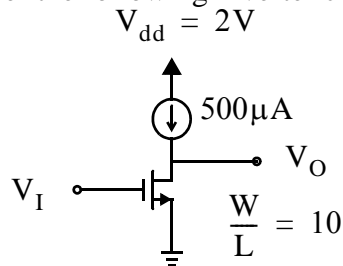
2.10 As temperature rises, does the current through an ON transistor increase or decrease? Does current through an OFF transistor increase or decrease? Will a chip operate faster at high temperature or low temperature? Explain.

- Consider the following resistor transistor logic (RTL) inverter where switch S1 represents the transistor and  $R_s$  represents the switch on resistance (it's off resistance is infinite).



- Sketch the output waveform for the switch toggling from open to closed. What is the time-constant in this case?
- Sketch the output waveform for the switch toggling from closed to open. What is the time-constant in this case?

- Consider the following inverter circuit.



$$\mu_n = 3\mu_p = 0.06 \text{ m}^2/\text{Vs}$$

$$C_{ox} = 8\text{fF}/\mu\text{m}^2$$

$$V_{tn} = 0.3\text{V}$$

- Sketch the input/output transfer curve.
- Find the threshold,  $V_{th}$ , of this inverter.

c) Find the output logic high and output logic low levels (assume the current source cannot drive the output above  $V_{dd}$ ).

**For questions 3-4 below, assume  $\mu_n = 3\mu_p = 0.06 \text{ m}^2/\text{Vs}$ ,  $V_{tn} = -V_{tp} = 0.3 \text{ V}$ ,  $C_{ox} = 8 \text{ fF}/\mu\text{m}^2$ , and  $V_{dd} = 2 \text{ V}$ .**

3) Given a CMOS inverter with  $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$ , where the input is at  $V_{dd}$ , find the maximum current that the output can sink before the output rises above  $0.2 \text{ V}$ .

4) Given a CMOS inverter with  $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 10$ , where the input is at  $0$ , find the maximum current that the output can source before the output falls below  $1.8 \text{ V}$ .