2.5 The minimum size diffusion contact is 4 x 5 λ, or 1.2 x 1.5 μm. The area is 1.8 μm^2 and perimeter is 5.4 μm. Hence the total capacitance is

$$C_{db}(0V) = (1.8)(0.42) + (5.4)(0.33) = 2.54\,fF$$

At a drain voltage of VDD, the capacitance reduces to

$$C_{db}(5V) = (1.8)(0.42)\left(1+\frac{5}{0.98}\right)^{-0.44} + (5.4)(0.33)\left(1+\frac{5}{0.98}\right)^{-0.12} = 1.78\,fF$$

2.6 The new threshold voltage is found as

$$f_s = 2(0.026)\ln\frac{2\bullet 10^{17}}{1.45\bullet 10^{10}} = 0.85V$$

$$g = \frac{100\bullet 10^{-8}}{3.9\bullet 8.85\bullet 10^{-14}}\sqrt{2\left(1.6\bullet 10^{-19}\right)\left(11.7\bullet 8.85\bullet 10^{-14}\right)\left(2\bullet 10^{17}\right)} = 0.75V^{1/2}$$

$$V_t = 0.7 + g\left(\sqrt{f_s+4} - \sqrt{f_s}\right) = 1.66V$$

The threshold increases by 0.96 V.

2.7 No. Any number of transistors may be placed in series, although the delay increases with the square of the number of series transistors.

2.8 The threshold is increased by applying a negative body voltage so $V_{sb} > 0$.

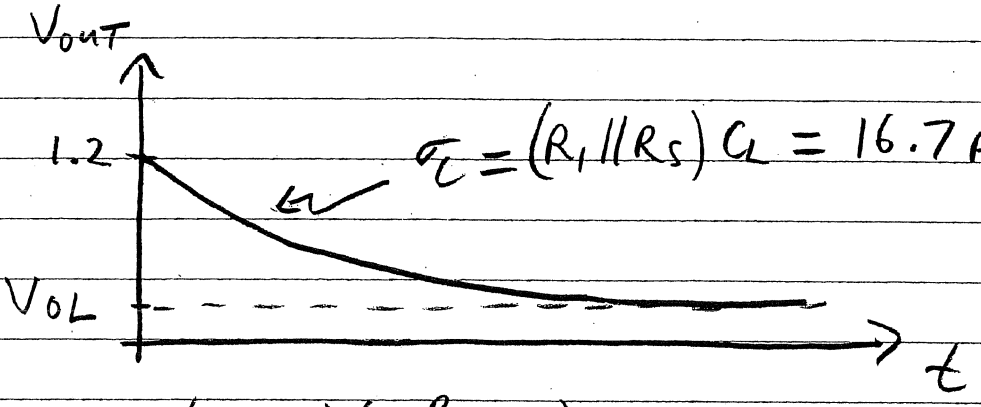
2.9 (a) (1.2 - 0.3)2 / (1.2 - 0.4)2 = 1.26 (26%)

(b) $\dfrac{e^{\frac{-0.3}{\sqrt{1.4\bullet 0.026}}}}{e^{\frac{-0.4}{\sqrt{1.4\bullet 0.026}}}} = 15.6$

(c) $v_T = kT/q$ = 34 mV; $\dfrac{e^{\frac{-0.3}{\sqrt{1.4\bullet 0.034}}}}{e^{\frac{-0.4}{\sqrt{1.4\bullet 0.034}}}} = 8.2$; note, however, that the total leakage will normally be higher for both threshold voltages at high temperature.

2.10 The current through an ON transistor tends to decrease because the mobility goes down. The current through an OFF transistor increases because V_t decreases. A chip will operate faster at low temperature.

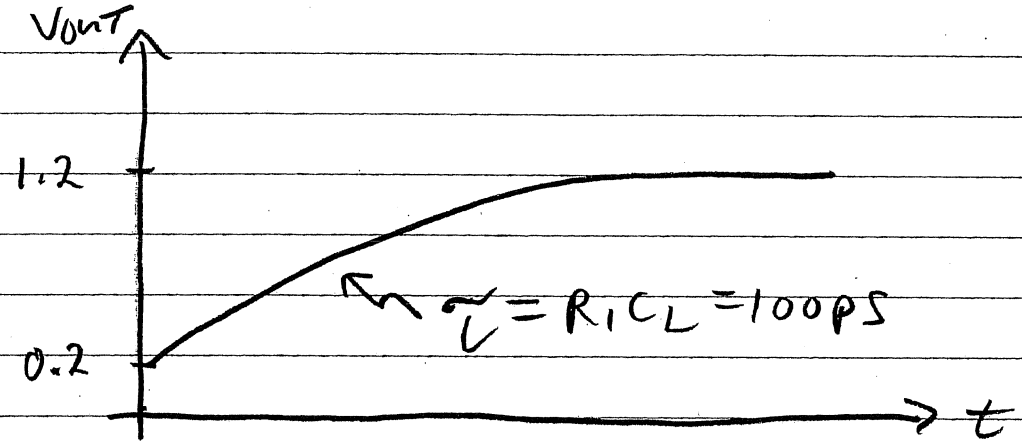
1) a)



$\tau_L = (R_1 \| R_S) C_L = 16.7\,ps$

$$V_{OL} = (1.2V)\left(\frac{R_S}{R_S + R_1}\right) = 0.2V$$

b)



2) b) V_{TH} occurs for $V_o = V_I$ therefore NMOS in saturation region (since $V_{GS} = V_{DS}$)

$\mu_N C_{ox} = (0.06\ m^2/Vs)(8\times10^{-3}\ F/m^2) = 480\ \mu A/V^2$

$$I_{DN} = \frac{\mu_N C_{ox}}{2}\left(\frac{W}{L}\right)\left[V_{TH} - V_{tN}\right]^2$$

$$500\,\mu A = \frac{(480e\text{-}6)}{2}(10)\left[V_{TH} - 0.3\right]^2$$

$$V_{TH} = \underline{\underline{0.756\ V}}$$

2 c) FOR $V_I = 0 \Rightarrow V_{OH} = V_{DD}$

FOR $V_I = V_{DD} \Rightarrow$ NMOS IN TRIODE

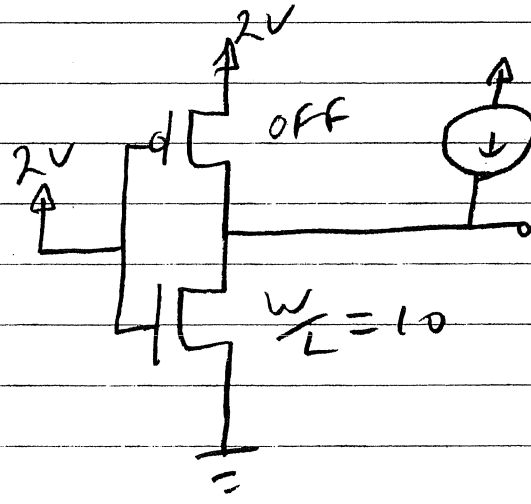
$$I_{DN} = \mu_N C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_{tN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

HERE $I_{DN} = 500\,\mu A$, $V_{GS} = V_{DD}$, $V_{DS} = V_{OL}$

$$500e\text{-}6 = (480e\text{-}6)(10)\left[(2 - 0.3)V_{OL} - \frac{V_{OL}^2}{2}\right]$$

$V_{OL} = 0.062$ V OR ~~3.34 V~~ NOT POSSIBLE SINCE OUT OF TRIODE

3)



$$I_{SOURCE} = (480e\text{-}6)(10)\left[(2 - 0.3)\,0.2 - \frac{0.2^2}{2}\right]$$

$$= 1.536\ mA$$

4) SIMILAR TO 3)

$$I_{SINK} = (160e\text{-}6)(10)\left[(-2+0.3)(-0.2) + \frac{(-0.2)^2}{2}\right]$$

$$= \underline{\underline{512\ \mu A}}$$

5) $C_{IN} = C_{gsN} + C_{gsP}$

$= C_{ox} W_N L_N + C_{ox} W_P L_P$

$= (8)(3)(0.3) + (8)(3)(0.3)$

$= 14.4\ fF$

6) SINCE LENGTH & WIDTH ARE 2 TIMES SIZES OF 5), THEN C_{IN} IS 4 TIMES

$C_{IN} = 4 \times 14.4\ fF = 57.6\ fF$