University of Toronto

Term Test 1

Date - Feb 10, 2010

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Only tests written in pen will be considered for a re-mark.
3. Calculator type unrestricted
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: SOLUTIONS

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T (F) In a rising clock edge register, when the clock is high, the first (input) latch is in track mode while the second (output) latch is in hold mode.

T (F) For a CMOS gate, the pull-up network is always the dual of the pull-down network.

T (F) Given a chain of identical CMOS inverters, the gate delay will DECREASE when C_{ox} is increased by 10%.

T (F) Given a chain of identical CMOS inverters, the gate delay will DECREASE when $|V_{tn}|$ and $|V_{tp}|$ are both increased by 10%.

T (F) Given a chain of identical CMOS inverters, the gate delay will DECREASE when the widths of all transistors are increased by 10%

(T) F For a CMOS gate, a large unwanted current will occur if both the pull-up network and pull-down network are on at the same time.

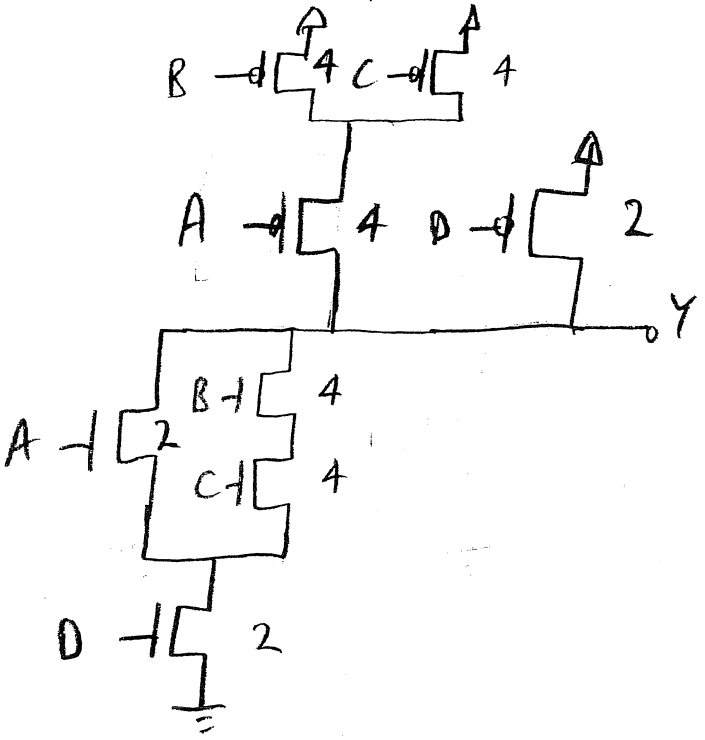
T (F) For pass transistor logic and where "1" equals Vdd and "0" equals ground, an NMOS transistor passes a "1" well but does not pass "0" well.

(T) F Restoring logic uses negative gain circuits where the output saturates towards the logic levels.

T (F) Moore's "law" states that "computer performance will double every 18 months".

T (F) For detailed estimation of drain-bulk junction capacitance, the gate-source voltage is required.

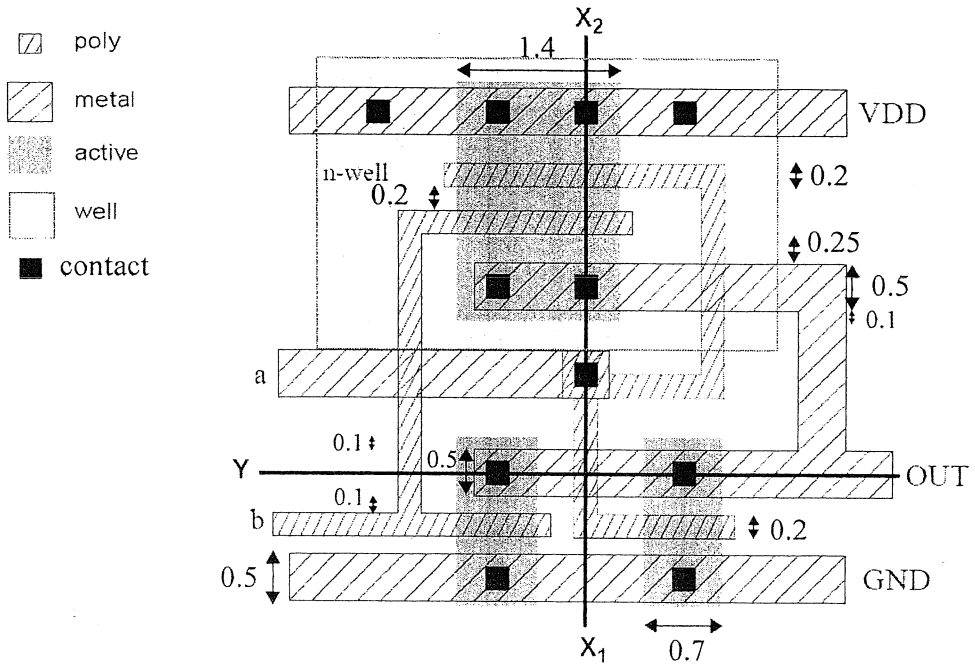
[6] Question 2: Show a CMOS gate that realizes the function $Y = \overline{(A + BC)D}$. Also, determine transistor sizes so that the worst case pull-down and pull-up is equivalent to a single inverter with $W_n = 1\mu m$ and $W_p = 2\mu m$. All transistor lengths are $0.25\mu m$.



W SHOWN BESIDE TRANSISTORS

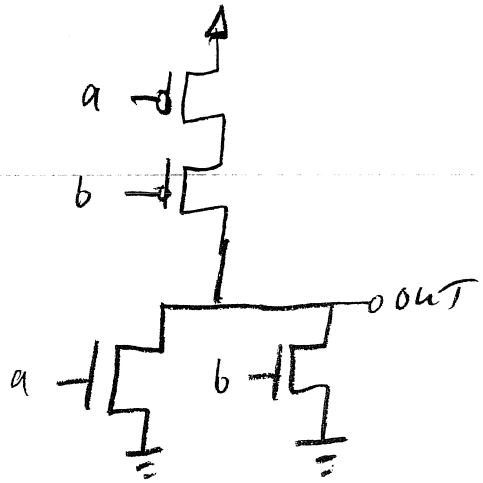
SOLUTION IS NOT UNIQUE.

[6] Question 3:



a) For the layout shown above, draw the schematic. Show the sizes of the NMOS and PMOS transistors. Also show the TOTAL drain area, A_D, and TOTAL drain perimeter, P_D, attached to the OUT node.

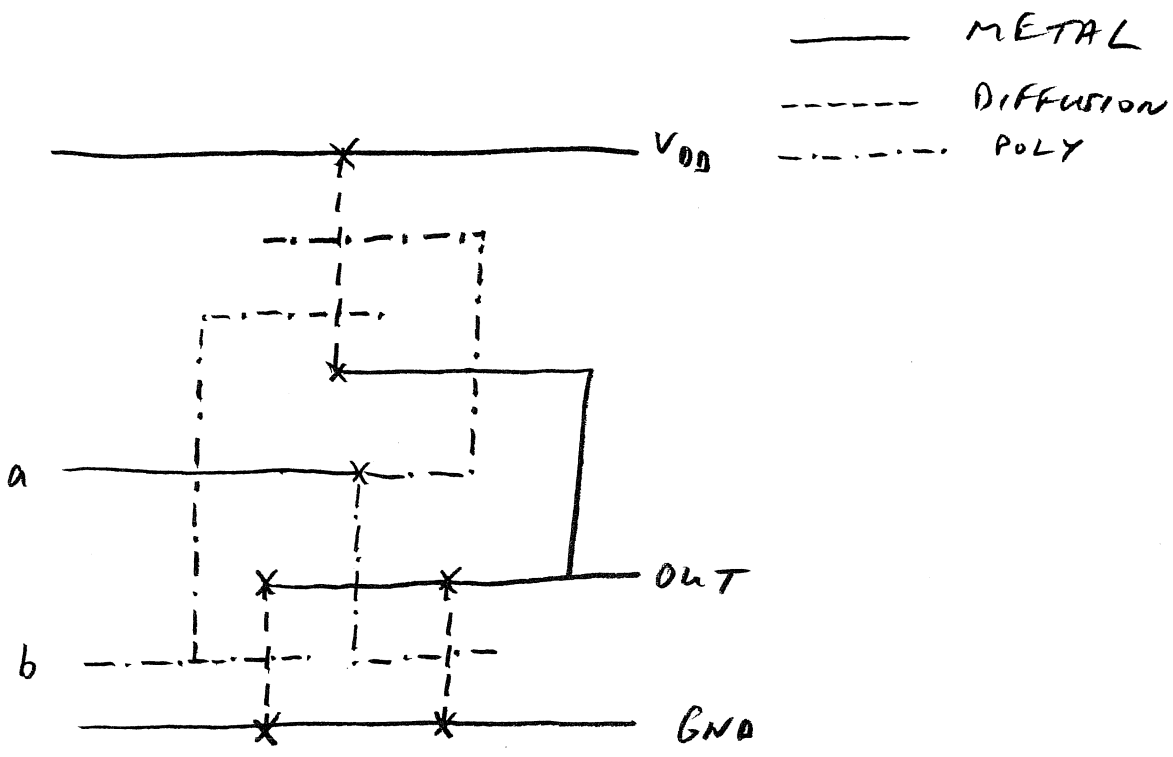
A_D =
P_D =



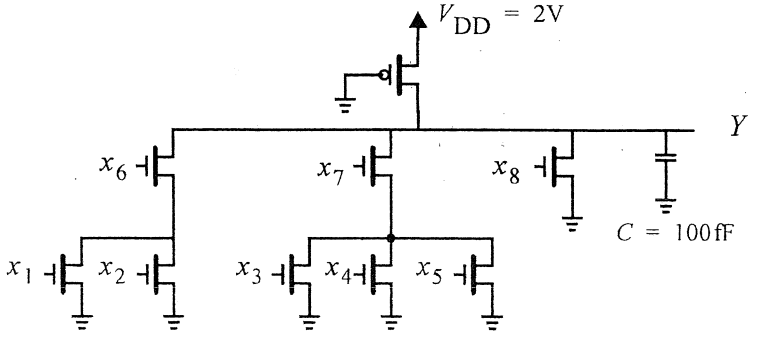
$A_D = 2(0.7)(0.7) + (0.85)(1.4) = 2.17\ (\mu m)^2$

$P_D = 4(0.7+0.7) + 2(0.85+1.4) = 10.1\ \mu m$

b) For the layout shown above, draw a stick diagram. Show your stick diagram legend that indicates which lines are poly, metal and active. Use "X" for contacts.



[6] Question 4: Consider the following ratioed logic gate



$\mu_n C_{ox} = 200\mu A/V^2$

$V_{tn} = 0.3V$
$W_p = 0.5\mu m$
$L_p = 1\mu m$

all $W_n = 1\mu m$
all $L_n = 0.25\mu m$

a) Using the RC delay estimate, find t_{df_min} and t_{df_max} (ignore effect of PMOS transistor).

$t_{df\_MAX} \Rightarrow X_1X_6,\ X_2X_6,\ X_3X_7,\ X_3X_7,\ X_5X_7$

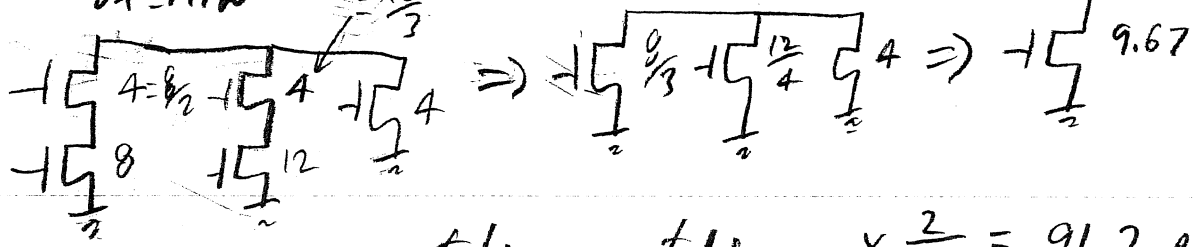
$\left(\frac{W}{L}\right)_{EQ} = \left(\frac{1}{0.5}\right) \Rightarrow R_{EQN} = \frac{2.5}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{DD}-V_{tN})}$

$= 2$

$= 3.68\,k$

$t_{df\_MAX} = 1.2\, R_{EQN} C = \underline{441\ ps}$

$t_{df\_MIN} \Rightarrow$ ALL HIGH



W/L SHOWN

$t_{df\_MIN} = t_{df\_MAX} \times \frac{2}{9.67} = \underline{91.2\ ps}$

b) If the effect of the PMOS transistor is taken into account, would the delay estimate for both t_{df_min} and t_{df_max} decrease, increase or stay the same? Explain.

IT WOULD DECREASE DELAY TIMES AS IT IS EQUIVALENT TO A RESISTANCE IN PARALLEL TO R_{EQN} OF NMOS TRANSISTORS.

[6] Question 5: A CMOS process has a supply voltage of 2V and an NMOS threshold voltage of 0.3V. A circuit designer is evaluating a proposal to reduce V_{tn} by 100mV to reduce delay times for falling edges.

a) By what factor would the delay for falling edges decrease?

$\frac{2-0.2}{2-0.3} = 1.059$ OR 5.9% DECREASE

b) By what factor would the subthreshold leakage current increase at room temperature at $V_{GS} = 0$? Assume $n = 1.4$. $V_t = 26\,mV$

$$\frac{e^{\frac{-0.2}{(1.4)(26mV)}}}{e^{\frac{-0.3}{(1.4)(26mV)}}} = e^{\frac{0.1}{(1.4)(26mV)}} = 15.6$$

c) Assuming the threshold voltage remains fixed at $V_{tn} = 0.3\,V$, does the delay for falling edges decrease or increase as the temperature is lowered? Explain your reasoning.

DELAY DECREASES SINCE MOBILITY INCREASES AS TEMP IS LOWERED.

(blank sheet for scratch calculations)

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}\,\mathrm{JK}^{-1}$; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26\,\mathrm{mV}$ at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0}e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;