

**University of Toronto**

**Term Test 1**

Date - Feb 9, 2011

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

**ANSWER QUESTIONS ON THESE SHEETS USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
  2. Only tests written in pen will be considered for a re-mark.
  3. Calculator type unrestricted
  4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.
- 

**Last Name:** SOLUTIONS

**First Name:** \_\_\_\_\_

**Student #:** \_\_\_\_\_

Question	Mark
1	
2	
3	
4	
5	
Total	

**(max grade = 29)**

[5] Question 1: Each correct answer is worth 0.5 marks.

For the questions below, circle one of True [T] or False [F].

T  F The capacitance of a reverse biased junction increases as the reverse bias voltage is increased.

T  F The output of a CMOS tri-state inverter is one of  $V_{DD}$ ,  $V_{DD}/2$ , or 0.

T F  $C_{ox}$  is inversely proportional to the gate oxide thickness.

T F Channel length modulation is generally important in analog circuits but not usually important in digital circuits.

For the questions below, consider the gate delay for a chain of identical CMOS inverters and only one parameter is changed. Circle one of "increase", "unchanged" or "decrease" that corresponds to the new gate delay

increase  unchanged decrease  $C_{ox}$  is increased by 10%

increase unchanged  decrease  $V_{DD}$  is increased by 10%

increase  unchanged decrease The widths of all transistors are increased by 10%

increase unchanged decrease  $|V_{tn}|$  and  $|V_{tp}|$  are both increased by 10%

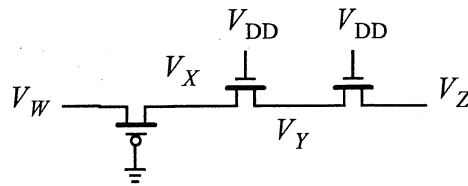
increase unchanged decrease Temperature is increased by 10%

increase unchanged  decrease Electron and hole mobility are both increased by 10%



[6] Question 3: Consider the pass transistor logic shown below where  $V_W$  is the input and  $V_Z$  is the output. Use CMOS parameters on equation sheet (last page).

IGNORE BODY EFFECT



for all transistors  $V_{DD} = 2.5$   
 $W = 1\mu m$   
 $L = 0.25\mu m$

a) When  $V_W$  is initially 0V and then goes to  $V_{DD}$ , find the final voltage values at  $V_X$ ,  $V_Y$ , and  $V_Z$ .

$$V_X = V_{DD} = \underline{\underline{2.5V}}$$

$$V_Y = V_{DD} - V_{tN} = 2.5 - 0.4 = \underline{\underline{2.1V}}$$

$$V_Z = V_{DD} - V_{tN} = \underline{\underline{2.1V}}$$

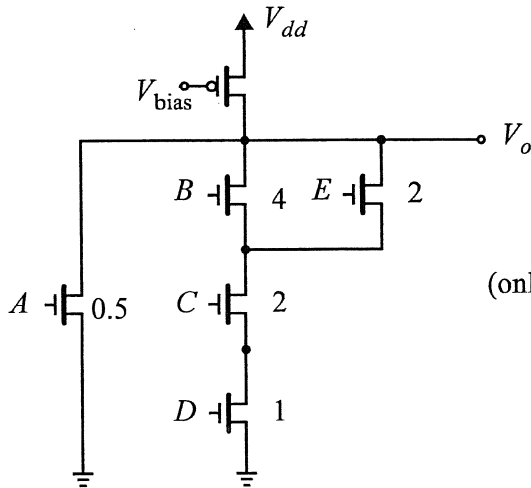
b) When  $V_W$  is initially  $V_{DD}$  and then goes to 0V, find the final voltage values at  $V_X$ ,  $V_Y$ , and  $V_Z$ .

$$V_X = 0 - V_{tP} = \underline{\underline{0.4V}}$$

$$V_Y = V_X = \underline{\underline{0.4V}}$$

$$V_Z = V_Y = \underline{\underline{0.4V}}$$

[6] **Question 4:** Using the concept of equivalent transistors, simplify the n-channel driver network shown below to a single pull-down transistor with a width of  $W_n$  (all lengths are same and minimum). Find this equivalent transistor for 2 cases:  $W_{n(\text{fast})}$  representing the input pattern with the fastest pull-down and  $W_{n(\text{slow})}$  for the slowest pull-down input case.

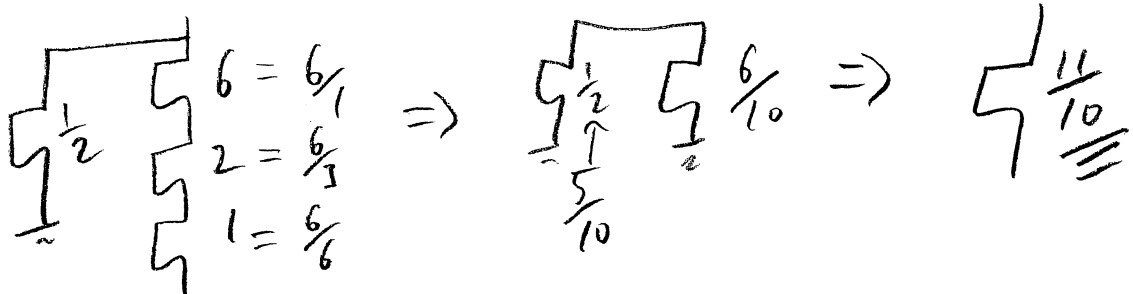


$$W_{n(\text{fast})} = \frac{11}{10} = 1.1$$

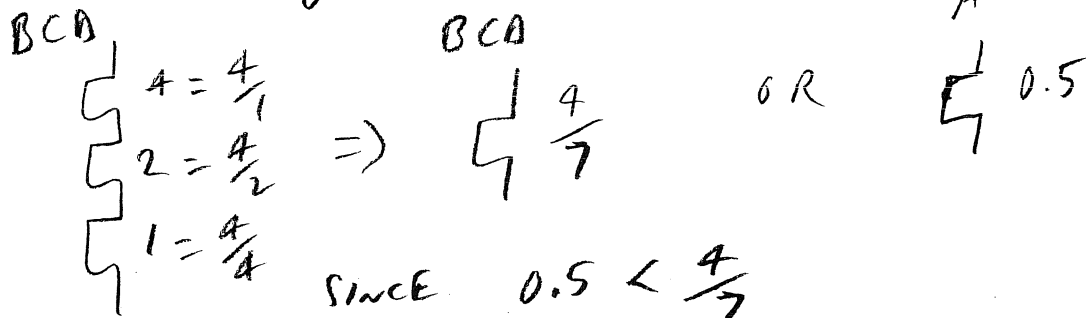
$$W_{n(\text{slow})} = 0.5$$

(only widths shown, all length are minimum)

$W_N(\text{FAST})$  ALL A-E HIGH



$W_N(\text{SLOW})$  EITHER A HIGH OR B C A HIGH

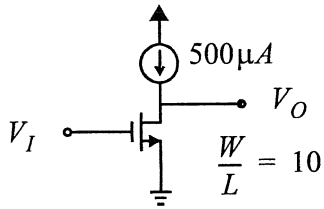


SINCE  $0.5 < \frac{4}{7}$

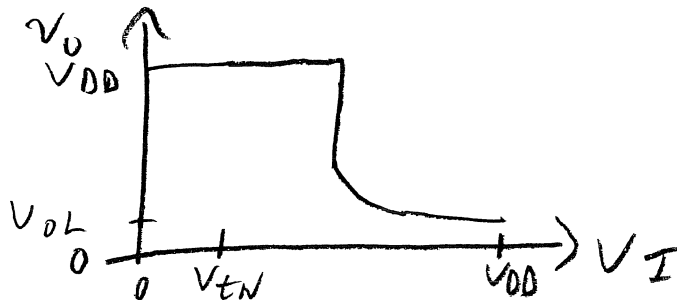
$$W_{N(\text{SLOW})} = 0.5$$

[6] Question 5: Consider the following inverter circuit. Assume the current source is ideal until the voltage across it is 1mV at which point it linearly drops to 0mA at 0V across it. Use CMOS parameters on equation sheet (last page).

$$V_{DD} = 2V$$



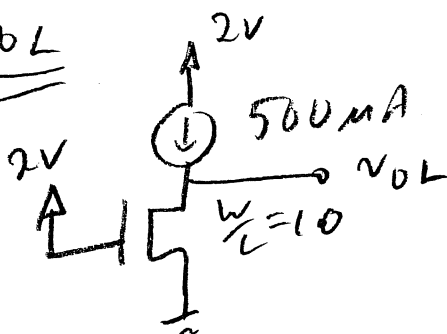
a) Sketch the input/output transfer curve for  $V_I$  from zero to  $V_{DD}$ .



b) Find the output logic high and output logic low levels assuming  $V_I$  goes from 0 to  $V_{DD}$ .

$$V_{OH} = V_{DD} = \underline{\underline{2V}}$$

$$\underline{\underline{V_{OL}}}$$



$$I_{DN} = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[ (V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_{DN} = 500 \mu A$$

$$V_{GS} = V_{DD} = 2V$$

$$V_{DS} = V_{OL}$$

$$500 \mu A = (120 \times 10^{-6}) (10) \left[ (2 - 0.4) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

$$0.4167 = 1.6 V_{OL} - \frac{V_{OL}^2}{2}$$

$$V_{OL}^2 - 3.2 V_{OL} + 0.833 = 0$$

$$V_{OL} = 2.91 \text{ or } \underline{\underline{0.286 V}}$$

$$\underline{\underline{V_{OL} = 0.29 V}}$$

**ECE334**

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**Equation Sheet**

**Constants:**  $k = 1.38 \times 10^{-23} \text{ JK}^{-1}$ ;  $q = 1.602 \times 10^{-19} \text{ C}$ ;  $V_T = kT/q \approx 26 \text{ mV}$  at 300 °K ;  
 $\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$ ;  $k_{ox} = 3.9$ ; **caps:**  $C_{ox} = (k_{ox}\epsilon_0)/t_{ox}$ ;  $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$  ;  
**NMOS:**  $\beta_n = \mu_n C_{ox}(W/L)$ ;  $V_{in} > 0$ ;  $V_{DS} \geq 0$ ; (triode)  $I_D = \beta_n((V_{GS} - V_{in})V_{DS} - (V_{DS}^2/2))$ ; (active)  $I_D = 0.5\beta_n(V_{GS} - V_{in})^2$ ;  
 (triode)  $V_{DS} \leq (V_{GS} - V_{in})$ ; (active)  $V_{DS} \geq (V_{GS} - V_{in})$ ;  $V_{in} = V_{in0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$ ;  
 (subthreshold)  $I_D = I_{D0}e^{((V_{GS} - V_{in})/(nV_T))} (1 - e^{-V_{DS}/V_T})$  ;  
**PMOS:**  $\beta_p = \mu_p C_{ox}(W/L)$ ;  $V_{ip} < 0$ ;  $V_{DS} \leq 0$ ; (triode)  $I_D = \beta_p((V_{GS} - V_{ip})V_{DS} - (V_{DS}^2/2))$ ; (active)  $I_D = 0.5\beta_p(V_{GS} - V_{ip})^2$ ;  
 (triode)  $V_{DS} \geq (V_{GS} - V_{ip})$ ; (active)  $V_{DS} \leq (V_{GS} - V_{ip})$ ;  
**Simple cap model:**  $C_g = C_{ox}WL$ ; if  $L_{min}$ ;  $C_{gu} \equiv C_{ox}L_{min}$ ;  $C_g = C_{gu}W$ ;  $C_d = C_s = C_{du}W$  ;  
**CMOS inverter:**  $V_{TH} = (V_{DD} + V_{ip} + V_{in}r)/(1+r)$ ;  $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$  ;  
**RC delay est:**  $t_{dr} = t_{df} = 1.2\tau$ ;  $\tau = R_{eq}C$ ;  $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{in}))$ ;  $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{ip}))$  ;  
 $(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$  **Unit delay est:**  $t_{d\Omega}/t_{d\Gamma} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$   
**Min delay:**  $t_{delay} = \tau_{inv}(C_{out}/C_{in})$ ; **total delay** =  $Nf\tau_{inv}$ ;  $f^N = C_{out}/C_{in}$ ; usually  $f = 4$   
**Power diss:**  $P_{dyn} = P_1 \rightarrow 0 f C_L V_{DD}^2$ ;  $P_{dp} = 0.5P_1 \rightarrow 0 f V_{DD} I_{peak}(t_r + t_f)$ ;  $I_{peak} = 0.5\beta_n(V_{TH} - V_{in})^2$  ;  
**Elmore Delay:**  $\tau_i \equiv \sum C_k R_{ik}$ ; dist RC,  $\tau \equiv RC/2$  ;  
**Interconnect:**  $R = (\rho l)/(tw)$ ;  $R_{\square} = \rho/t$ ;  $C = (\epsilon_{ox}wl)/t$ ;  $C = \epsilon_{ox}l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$  ;  
**Max delay constraint:**  $T_c \geq t_{pcq} + t_{pd} + t_{setup}$  **Min Delay constraint:**  $t_{hold} \leq t_{ccq} + t_{cd}$  **Metastability:**  $MTBF = e^{T/\tau_s}/(t_{rd}F_D F_{CLK})$   
**SRAM:** M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,  
**SRAM read:**  $W_1/W_3 \geq (V_{DD} - V_A - V_{in})^2 / (2((V_{DD} - V_{in})V_A - V_A^2/2))$  ;  $I_{cell} = ((\mu_n C_{ox})/2)(W_3/L)(V_{DD} - 2V_{in})^2$   
 $\Delta V_{BL} = (I_{cell}\Delta t)/C_{BL}$   
**SRAM write:**  $W_3/W_5 \geq (\mu_p(V_{DD} + V_{ip})^2) / (2\mu_n((V_{DD} - V_{in})V_A - V_A^2/2))$

**MOS Transistor;** CMOS basic parameters. Channel length =  $0.25\mu m$ ,  $m_j = 0.5$ ,  $\phi_0 = 0.9V$

	$V_{T0}$ (V)	$\gamma$ ( $V^{0.5}$ )	$\mu C_{ox}$ ( $\mu A/V^2$ )	$\lambda$ ( $V^{-1}$ )	$C_{ox}$ ( $fF/\mu m^2$ )	$C_o$ ( $fF/\mu m$ )	$C_j$ ( $fF/\mu m^2$ )	$C_{jsw}$ ( $fF/\mu m$ )
NMOS	0.4	0.4	120	0.06	6	0.3	2	0.3
PMOS	-0.4	0.4	30	0.1	6	0.3	2	0.3

$V_{T0}$  is the threshold voltage with zero bulk-source voltage;  $\gamma$  is used to account for non-zero bulk-source voltage;  $\mu C_{ox}$  is the transistor current gain parameter;  $\lambda$  is to account for the transistor finite output impedance (channel length modulation);  $C_{ox}$  is the gate capacitance per unit area;  $C_o$  is the gate overlap capacitance per unit length;  $C_j$  is the drain/source junction capacitance per unit area;  $C_{jsw}$  is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters