University of Toronto

Term Test 2

Date - Mar 17, 2010

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Only tests written in pen will be considered for a re-mark.
3. Calculator type unrestricted
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: SOLUTIONS

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T (F) When creating metal wires on a chip, first silicon dioxide is grown and photoresist is used to etch where wires should exist. Next, aluminum is sprayed on using silicon dioxide as a mask.

(T) F When creating metal wires on a chip, first aluminum is sprayed on the entire micro-chip, then photoresist and silicon oxide is used to mask where wires should exist and the rest is etched off.

T (F) In a self-aligned process, the drain/source junctions are first formed and then the gate is formed above the drain/source junctions so that it is self-aligned.

T (F) The silicon dioxide layer formed under the gate region is grown using wet oxidation instead of dry oxidation.

T (F) Tungsten is used in via and contact holes due to its low resistance.

(T) F P-type silicon is made by doping pure silicon with boron.

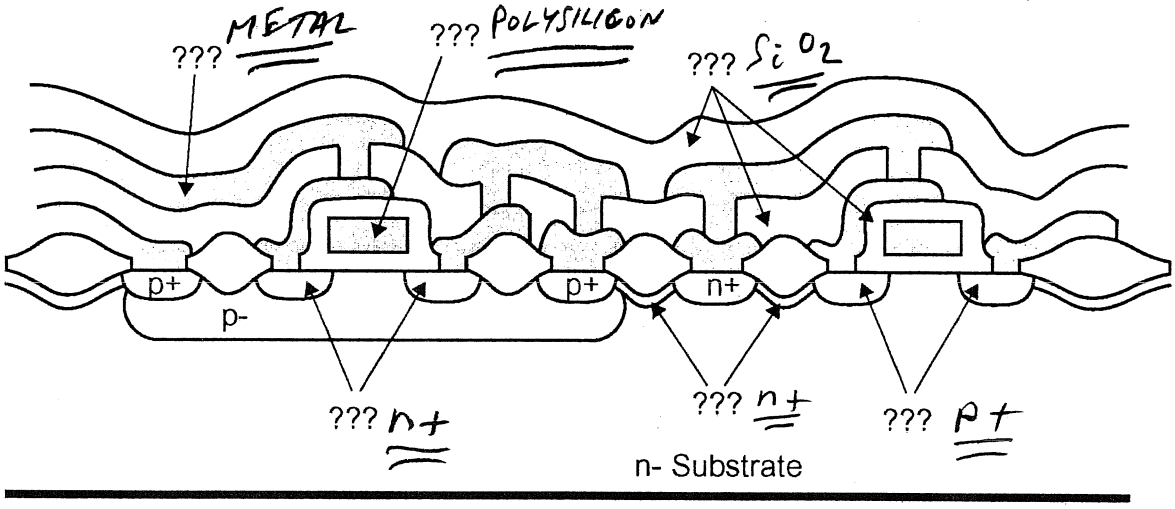
T (F) The dynamic power of a digital chip is due to the energy being dissipated across capacitors in the chip.

T (F) In CMOS circuits, to keep all the drain/source diodes reverse biased, the substrate (or bulk) of all NMOS transistors should be tied to V_{dd} while the substrate (or bulk) of all PMOS transistors should be tied to ground.

(T) F A pseudo-NMOS gate with power supplies 0 and V_{dd} has it's output high level equal to V_{dd} while it's output low level is a value greater than 0.

T (F) V_{TH} for an inverter is defined to be the input voltage where the inverter's gain is largest.

[6] Question 2: Consider the following cross-section of a p-well process (not n-well)



a) On the above diagram, label all the "???" signs with the material name (i.e. polysilicon, silicon dioxide, metal, p+, n+, p-, n-, etc.).

b) What is the purpose of the p+ in the p-well and the n+ in the n- substrate?

THESE ARE SUBSTRATE CONTACTS TO BIAS THE P-WELL AND N- SUBSTRATE. IF METAL DIRECTLY CONNECTED TO LIGHTLY DOPED MATERIAL SCHOTTKEY DIODE IS FORMED SO HEAVILY DOPED MATERIAL IS USED.

c) What is the purpose of field-implants?

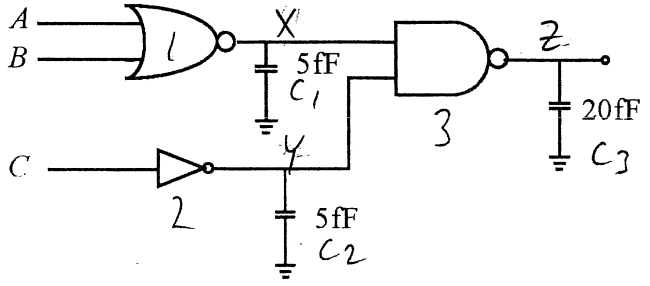
SO THAT THE SUBSTRATE DOES NOT INVERT DUE TO VOLTAGES ABOVE IT.

d) Explain clearly why metal is not used as the gate material in a self-aligned process.

IT WOULD MELT DURING ANNEALING PROCESS STEP. POLYSILICON CAN WITHSTAND HIGHER TEMPERATURES.

[6] Question 3: Find the dynamic power dissipation, P_{dyn}, for the following CMOS circuit assuming the clock is 1GHz, V_{DD} = 2.5V and the inputs have the following probability values that change on the rising edge of the clock.

$P(A=1) = 0.5$, $P(B=1) = 0.4$, $P(C=1) = 0.7$



P_{dyn} = 23.4 μW

$P_{DYN\_1} = P_{1\to0} f C_1 V_{DD}^2$

$P_{X=1} = P_{A=0} P_{B=0} = (0.5)(0.6) = 0.3$

$P_{X=0} = 1 - P_{X=1} = 0.7$

$P_{X(1\to0)} = (0.3)(0.7) = 0.21$

$P_{DYN\_1} = (0.21)(1e9)(5e-15)(2.5)^2 = 6.6\,\mu W$

$P_{DYN\_2} = P_{1\to0} f C_2 V_{DD}^2 = (0.3)(0.7)(1e9)(5e-15)(2.5^2)$

$= 6.6\,\mu W$

$P_{DYN\_3} = P_{1\to0} f C_3 V_{DD}^2$

$P_{Z=0} = P_{X=1} P_{Y=1} = (0.3)(0.3) = 0.09$

$P_{Z=1} = 1 - P_{Z=0} = 0.91$

$P_{DYN\_3} = (0.91)(0.09)(1e9)(20e-15)(2.5^2)$

$= 10.2\,\mu W$

$P_{DYN} = P_{DYN\_1} + P_{DYN\_2} + P_{DYN\_3} = 6.6 + 6.6 + 10.2$

$= 23.4\,\mu W$

[6] Question 4: Consider a metal 1 (first layer of metal) aluminum wire that is 0.8μm above the substrate, is 0.5μm in height and has a width of 0.25μm and has a length of 5 mm .Recall that the resistivity of aluminum is 2.8 μΩ • cm

a) Find the resistance per μm , R_w and the capacitance per μm , C_w.

$R_\square = \frac{\sigma}{t} = \frac{2.8e-8\ \Omega\cdot m}{0.5e-6\ m} = 0.056\ \Omega/\square$

$R_w = R_\square \frac{1mm}{0.25\mu m} = 4R_\square = 0.224\ \Omega/\mu m$

$C_w = \varepsilon_{ox}\left[\left(\frac{w}{h}\right)+0.77+1.06\left(\frac{w}{h}\right)^{0.25}+1.06\left(\frac{t}{h}\right)^{0.5}\right]$

$= 3.9\times 8.854e-12\,[2.71]$

$= 93.7\ pF/m = 0.094\ fF/\mu m$

$R_w = 0.224\ \Omega/\mu m$

$C_w = 0.094\ fF/\mu m$

a) Estimate the delay, t_d, of this wire assuming the delay is 1.2τ.

$\tau = \frac{RC}{2} = \frac{(0.224)(5000)(0.094)(5000)}{2}$

$= \frac{(1120)(470\ fF)}{2} = 263\ ps$

$t_d = 1.2\tau = 316\ ps$

$t_d = 316\ ps$

b) Estimate the delay of this wire if the width is increased to 1μm and other parameters are unchanged.

$w_2 = 4w \Rightarrow R_2 = \frac{R}{4} = 280\ \Omega$

$C_{w_2} = \varepsilon_{ox}\left[\left(\frac{w_2}{h}\right)+0.77+1.06\left(\frac{w_2}{h}\right)^{0.25}+1.06\left(\frac{t}{h}\right)^{0.5}\right]$

$= \varepsilon_{ox}\,[3.98] = 0.138\ fF/\mu m$

$C_2 = C_{w_2}(5000) = 690\ fF$

$t_{d_2} = 1.2\frac{R_2 C_2}{2} = 116\ ps$

$t_d = 116\ ps$

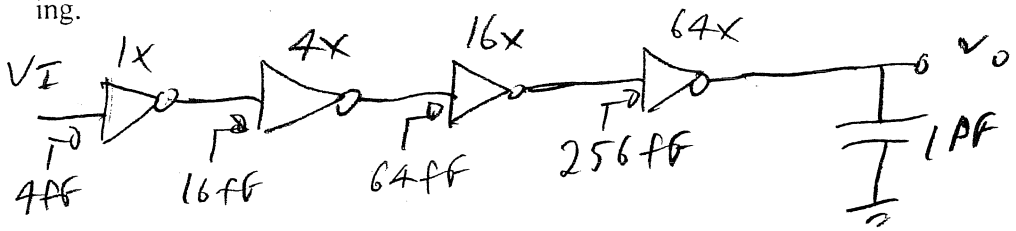
[6] Question 5: It is desired to drive a 1pF capacitive load given that a minimum size inverter has a gate capacitance of 4fF and it's inherent delay is 15ps.

a) Find the delay if a single inverter is used.

$$t_d = \tau_{INV} \frac{C_{OUT}}{C_{IN}} = (15\,ps)\left(\frac{1\,pF}{4\,fF}\right)$$

$$= 3.75\,ns$$

b) Find the delay if an inverter chain is used where a fanout factor of 4 is used for inverter sizing.



$$t_d = 3\tau_{INV}(4) + \tau_{INV}\left(\frac{1\,pF}{256\,fF}\right) = 12\tau_{INV} + 3.9\tau_{INV}$$

$$= 15.9\tau_{INV} = (15.9)(15\,ps) = 238\,ps$$

c) Explain why a fanout factor of 4 is generally used for inverter sizing in an inverter chain instead of a factor of *e* which was derived in class to be optimum. (hint: what was overlooked in the class derivation?)

CLASS DERIVATION DID NOT ACCOUNT FOR OUTPUT CAPACITANCE OF AN INVERTER WHICH ROUGHLY SCALES WITH SIZE OF INVERTER. ALSO FACTOR OF 4 IS SIMPLE TO DO.

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}$ JK^{-1} ; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26$mV at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$;(triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$;(active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0} e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$;(triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$;(active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to 0} f C_L V_{DD}^2$; $P_{dp} = 0.5 P_{1\to 0} f V_{DD} I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_\square = \rho/t$; $C = (\varepsilon_{ox} w l)/t$; $C = \varepsilon_{ox} l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;