University of Toronto

Term Test 1

Date - Feb 9, 2011

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Only tests written in pen will be considered for a re-mark.
3. Calculator type unrestricted
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Each correct answer is worth 0.5 marks.

For the questions below, circle one of True [T] or False [F].

T F The capacitance of a reverse biased junction increases as the reverse bias voltage is increased.

T F The output of a CMOS tri-state inverter is one of V_{DD}, $V_{DD}/2$, or 0.

T F C_{ox} is inversely proportional to the gate oxide thickness.

T F Channel length modulation is generally important in analog circuits but not usually important in digital circuits.

For the questions below, consider the gate delay for a chain of indentical CMOS inverters and only one parameter is changed. Circle one of "increase", "unchanged" or "decrease" that corresponds to the new gate delay

increase unchanged decrease C_{ox} is increased by 10%

increase unchanged decrease V_{DD} is increased by 10%

increase unchanged decrease The widths of all transistors are increased by 10%

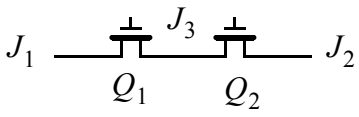
increase unchanged decrease $|V_{tn}|$ and $|V_{tp}|$ are both increased by 10%

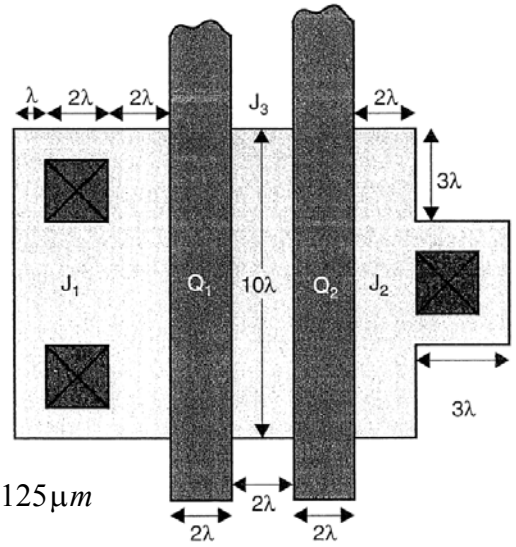
increase unchanged decrease Temperature is increased by 10%

increase unchanged decrease Electron and hole mobility are both increased by 10%

Last Name: _____

[6] Question 2: Consider the layout of 2 nmos transistors as shown below and use CMOS parameters on the equation sheet (last page).





$\lambda = 0.125\mu m$

a) Find the input capacitance for the gate of a single transistor (ignore overlap capacitance).

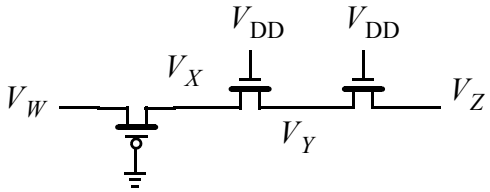
b) Find the overlap capacitance for the gate of Q_2 to junction J_2

c) Find the drain-bulk capacitance at J_3 (using both area and sidewall capacitance).

d) Find the drain-bulk capacitance at J_2 (using both area and sidewall capacitance).

Last Name: _____

[6] Question 3: Consider the pass transistor logic shown below where V_W is the input and V_Z is the output. Use CMOS parameters on equation sheet (last page) and IGNORE body effect.

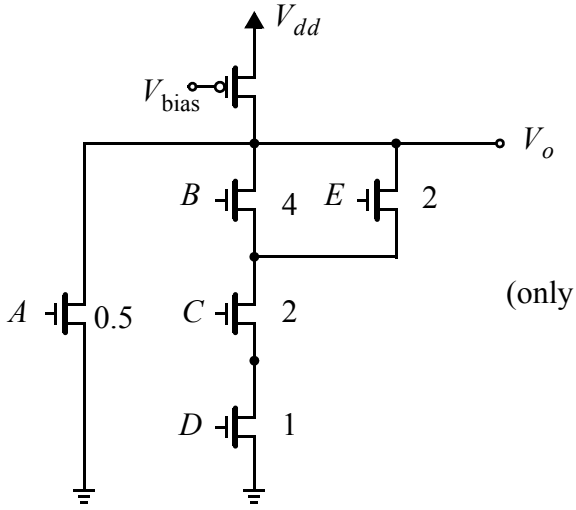


for all transistors $V_{DD} = 2.5$, $W = 1\mu m$, $L = 0.25\mu m$

a) When V_W is initially 0V and then goes to V_{DD}, find the final voltage values at V_X, V_Y, and V_Z.

b) When V_W is initially V_{DD} and then goes to 0V, find the final voltage values at V_X, V_Y, and V_Z.

[6] Question 4: Using the concept of equivalent transistors, simplify the n-channel driver network shown below to a single pull-down transistor with a width of W_n (all lengths are same and minimum). Find this equivalent transistor for 2 cases: $W_{n(\text{fast})}$ representing the input pattern with the fastest pull-down and $W_{n(\text{slow})}$ for the slowest pull-down input case.

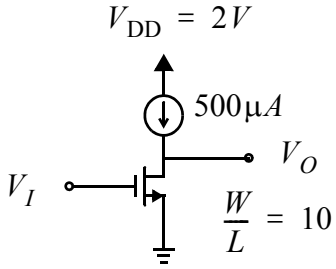


$W_{n(\text{fast})}$ =

$W_{n(\text{slow})}$ =

(only widths shown, all length are minimum)

[6] Question 5: Consider the following inverter circuit. Assume the current source is ideal until the voltage across it is 1mV at which point it linearly drops to 0mA at 0V across it. Use CMOS parameters on equation sheet (last page).



a) Sketch the input/output transfer curve for V_I from zero to V_{DD}.

b) Find the output logic high and output logic low levels assuming V_I goes from 0 to V_{DD}.

Last Name: _____

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}$ JK^{-1} ; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26$mV at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0} e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to 0} f C_L V_{DD}^2$; $P_{dp} = 0.5 P_{1\to 0} f V_{DD} I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_{\square} = \rho/t$; $C = (\varepsilon_{ox} wl)/t$; $C = \varepsilon_{ox} l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;

Max delay constraint: $T_c \geq t_{pcq} + t_{pd} + t_{setup}$ **Min Delay constraint:** $t_{hold} \leq t_{ccq} + t_{cd}$ **Metastability:** MTBF $= e^{T/\tau_s}/(t_{rd} F_D F_{CLK})$

SRAM: M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,

SRAM read: $W_1/W_3 \geq (V_{DD} - V_A - V_{tn})^2/(2((V_{DD} - V_{tn})V_A - V_A^2/2))$; $I_{cell} = ((\mu_n C_{ox})/2)(W_3/L)(V_{DD} - 2V_{tn})^2$
$\Delta V_{BL} = (I_{cell}\Delta t)/C_{BL}$

SRAM write: $W_3/W_5 \geq (\mu_p(V_{DD} + V_{tp})^2)/(2\mu_n((V_{DD} - V_{tn})V_A - V_A^2/2))$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9$V

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	0.3
PMOS	-0.4	0.4	30	0.1	6	0.3	2	0.3

V_{T0} is the threshold voltage with zero bulk-source voltage; γ is used to account for non-zero bulk-source voltage; μC_{ox} is the transistor current gain parameter; λ is to account for the transistor finite output impedance (channel length modulation); C_{ox} is the gate capacitance per unit area; C_o is the gate overlap capacitance per unit length; C_j is the drain/source junction capacitance per unit area; C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters