University of Toronto

Term Test 2

Date - Mar 17, 2010

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Only tests written in pen will be considered for a re-mark.
3. Calculator type unrestricted
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T F When creating metal wires on a chip, first silicon dioxide is grown and photoresist is used to etch where wires should exist. Next, aluminum is sprayed on using silicon dioxide as a mask.

T F When creating metal wires on a chip, first aluminum is sprayed on the entire micro-chip, then photoresist and silicon oxide is used to mask where wires should exist and the rest is etched off.

T F In a self-aligned process, the drain/source junctions are first formed and then the gate is formed above the drain/source junctions so that it is self-aligned.

T F The silicon dioxide layer formed under the gate region is grown using wet oxidation instead of dry oxidation.

T F Tungsten is used in via and contact holes due to its low resistance.

T F P-type silicon is made by doping pure silicon with boron.

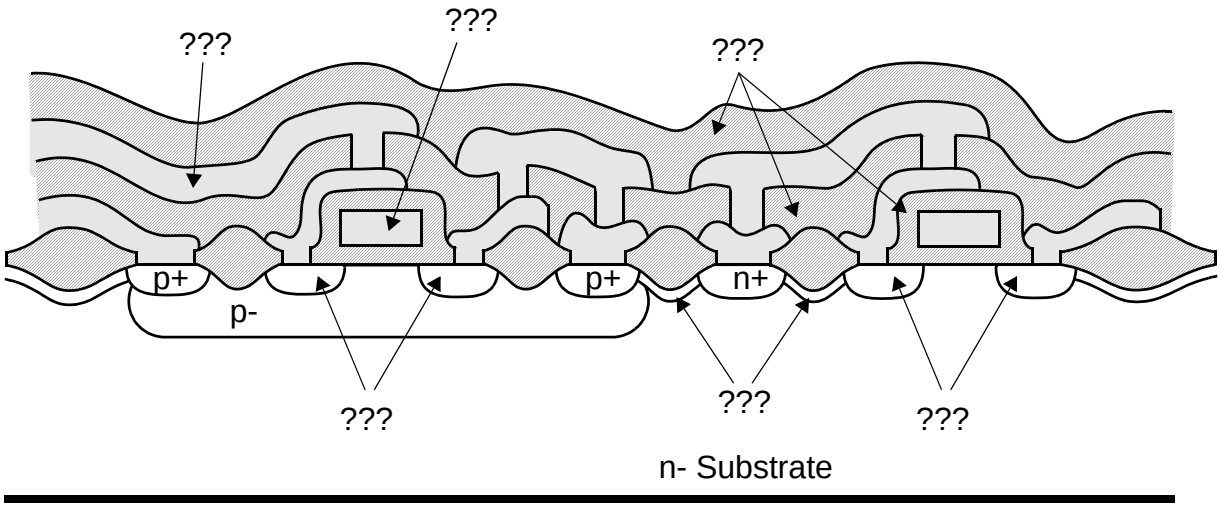
T F The dynamic power of a digital chip is due to the energy being dissipated across capacitors in the chip.

T F In CMOS circuits, to keep all the drain/source diodes reverse biased, the substrate (or bulk) of all NMOS transistors should be tied to V_{dd} while the substrate (or bulk) of all PMOS transistors should be tied to ground.

T F A pseudo-NMOS gate with power supplies 0 and V_{dd} has it's output high level equal to V_{dd} while it's output low level is a value greater than 0.

T F V_{TH} for an inverter is defined to be the input voltage where the inverter's gain is largest.

[6] Question 2: Consider the following cross-section of a p-well process (not n-well)



a) On the above diagram, label all the "???" signs with the material name (i.e. polysilicon, silicon dioxide, metal, p+, n+, p-, n-, etc.).

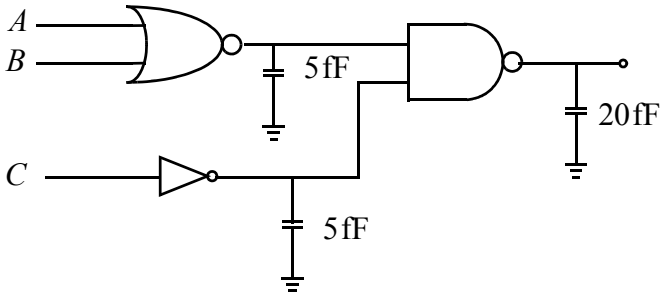
b) What is the purpose of the p+ in the p-well and the n+ in the n- substrate?

c) What is the purpose of field-implants?

d) Explain clearly why metal is not used as the gate material in a self-aligned process.

[6] Question 3: Find the dynamic power dissipation, P_{dyn}, for the following CMOS circuit assuming the clock is 1GHz, $V_{DD} = 2.5\text{V}$ and the inputs have the following probability values that change on the rising edge of the clock.

$P(\text{A=1}) = 0.5$, $P(\text{B=1}) = 0.4$, $P(\text{C=1}) = 0.7$



P_{dyn} =

Last Name: _____

[6] Question 4: Consider a metal 1 (first layer of metal) aluminum wire that is $0.8\mu m$ above the substrate, is $0.5\mu m$ in height and has a width of $0.25\mu m$ and has a length of 5 mm .Recall that the resistivity of aluminum is $2.8\ \mu\Omega \bullet cm$

a) Find the resistance per μm, R_w and the capacitance per μm, C_w.

R_w =

C_w =

a) Estimate the delay, t_d, of this wire assuming the delay is 1.2τ.

t_d =

b) Estimate the delay of this wire if the width is increased to $1\mu m$ and other parameters are unchanged.

t_d =

[6] Question 5: It is desired to drive a 1pF capacitive load given that a minimum size inverter has a gate capacitance of 4fF and it's inherent delay is 15ps.

a) Find the delay if a single inverter is used.

b) Find the delay if an inverter chain is used where a fanout factor of 4 is used for inverter sizing.

c) Explain why a fanout factor of 4 is generally used for inverter sizing in an inverter chain instead of a factor of e which was derived in class to be optimum. (hint: what was overlooked in the class derivation?)

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}\,\mathrm{JK}^{-1}$; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26\,\mathrm{mV}$ at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0} e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to 0} f C_L V_{DD}^2$; $P_{dp} = 0.5 P_{1\to 0} f V_{DD} I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_\square = \rho/t$; $C = (\varepsilon_{ox} wl)/t$; $C = \varepsilon_{ox} l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;