University of Toronto

Term Test 2

Date - Mar 16, 2011

Duration: 1.5 hrs

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Equation sheet is on last page of test.
2. Only tests written in pen will be considered for a re-mark.
3. Calculator type unrestricted
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Each correct answer is worth 0.5 marks.

For the questions below, circle one of True [T] or False [F].

T F In a 45nm CMOS process, the subthreshold leakage current is due to current leaking in and out of the mosfet gates due to very thin gate oxides.

T F Dynamic direct-path power dissipation increases as clock and data edge slew-rates decrease.

T F CMOS gates are made out of polysilicon so they will not melt during annealing.

T F A self-aligned process means that the different masks are self-aligned with each other.

T F A CMOS schmitt trigger is often used at the outputs of a digital chip to reduce noise.

T F When creating metal wires on a chip, first silicon dioxide is grown and photoresist is used to etch where wires should exist. Next, aluminum is sprayed on using silicon dioxide as a mask.

T F The silicon dioxide layer formed under the gate region is grown using wet oxidation instead of dry oxidation.

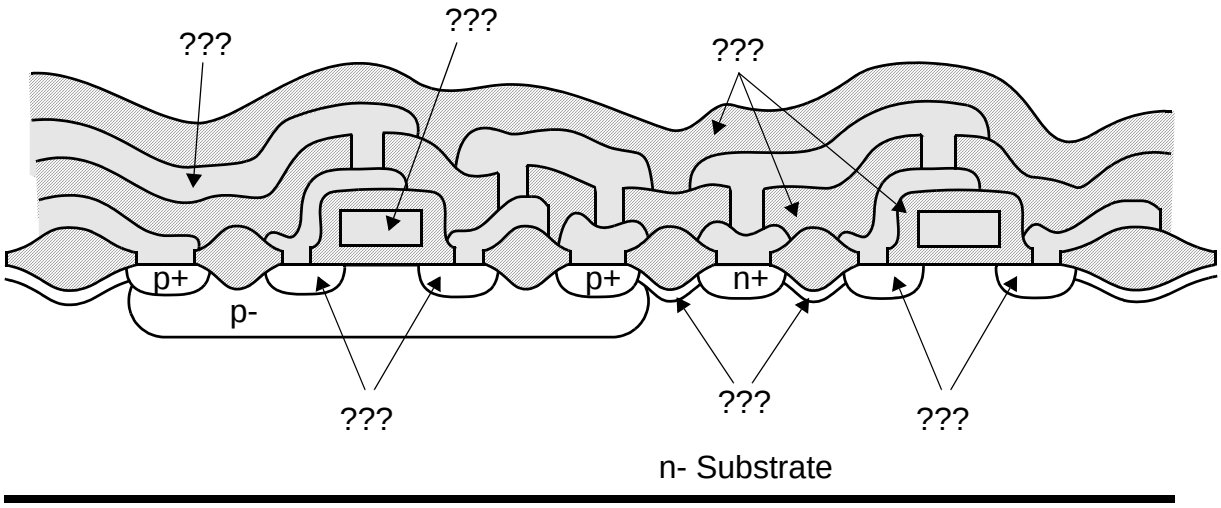
T F Tungsten is used in via and contact holes due to its low resistance.

T F The lowest level metal on a microchip is thicker than the highest level metal.

T F For interconnect metal wires, the fringe capacitance is usually larger than the parallel plate capacitance.

[6] Question 2: Given that a minimum size inverter has a gate capacitance of 4fF and it's inherent delay equals 15ps, find the number of inverters for an inverter chain that minimizes the propogation delay to drive a 10pF load when using a fan-out factor of 4 for inverter sizing. Also, what is the propogation delay?

[6] Question 3: Consider the following cross-section of a p-well process (not n-well)



a) On the above diagram, label all the "???" signs with the material name (i.e. polysilicon, silicon dioxide, metal, p+, n+, p-, n-, etc.).
b) How is **annealing** performed and why is it performed after ion implantation?

c) Name a dopant that can be used to make p-type silicon.

d) Name a dopant that can be used to make n-type silicon.

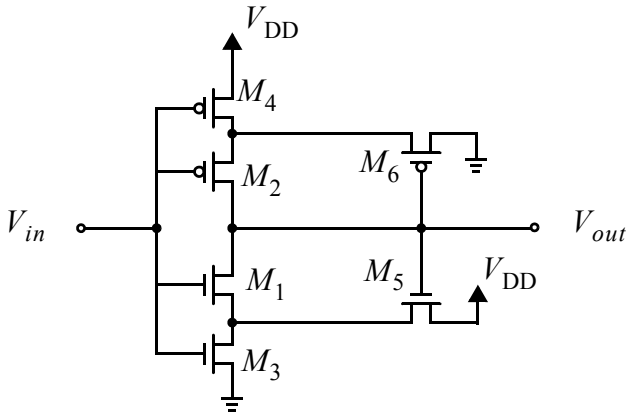
[6] Question 4:

a) A metal wire has a thickness of 480nm, a width of 250nm and is 800nm above the p- substrate. Find the capacitance per unit length in units of $fF/\mu m$. Also, out of the total capacitance, find the percentage capacitance that relates to the parallel plate model and the percentage that relates to the fringe capacitance (the sum of the 2 should equal 100%).

b) A metal wire has a sheet resistance of $0.08\ \Omega/\square$ and a capacitance of $0.2\ fF/\mu m$. Given that the wire is $1\ \mu m$ wide and $2\,mm$ long, construct a 3 segment π-model for the wire.

c) For the above model in part b), what would be the Elmore time-constant for a source driving a resistor of size $1k\Omega$ at one end of the wire with a capacitive load at the other end of 67 fF.

[6] Question 5: Consider the Schmitt trigger below. All transistors have minimum channel length and transistor relative widths are shown. Derive an expression for the switching threshold as V_{in} is increased from 0V. Ignore the body effect.



$$W_1 = 2W_3 = 4W_5$$
$$W_2 = 2W_4 = 4W_6$$

(blank sheet for scratch calculations)

Last Name: _____

ECE334 Digital Electronics Equation Sheet

Constants: $k = 1.38 \times 10^{-23}$ JK^{-1} ; $q = 1.602 \times 10^{-19}$ C ; $V_T = kT/q \approx 26$mV at 300 °K ;
$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m ; $k_{ox} = 3.9$; **caps:** $C_{ox} = (k_{ox}\varepsilon_0)/t_{ox}$; $C_j = C_{j0}/(1 + V_R/\phi_0)^{M_j}$;

NMOS: $\beta_n = \mu_n C_{ox}(W/L)$; $V_{tn} > 0$; $V_{DS} \geq 0$; (triode) $I_D = \beta_n((V_{GS} - V_{tn})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_n(V_{GS} - V_{tn})^2$;
(triode) $V_{DS} \leq (V_{GS} - V_{tn})$; (active) $V_{DS} \geq (V_{GS} - V_{tn})$; $V_{tn} = V_{tn0} + \gamma(\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s})$;
(subthreshold) $I_D = I_{D0} e^{((V_{GS} - V_{tn})/(nV_T))}(1 - e^{-V_{DS}/V_T})$;

PMOS: $\beta_p = \mu_p C_{ox}(W/L)$; $V_{tp} < 0$; $V_{DS} \leq 0$; (triode) $I_D = \beta_p((V_{GS} - V_{tp})V_{DS} - (V_{DS}^2/2))$; (active) $I_D = 0.5\beta_p(V_{GS} - V_{tp})^2$;
(triode) $V_{DS} \geq (V_{GS} - V_{tp})$; (active) $V_{DS} \leq (V_{GS} - V_{tp})$;

Simple cap model: $C_g = C_{ox}WL$; if L_{min} ; $C_{gu} \equiv C_{ox}L_{min}$; $C_g = C_{gu}W$; $C_d = C_s = C_{du}W$;

CMOS inverter: $V_{TH} = (V_{DD} + V_{tp} + V_{tn}r)/(1 + r)$; $r = \sqrt{(\mu_n(W/L)_n)/(\mu_p(W/L)_p)}$;

RC delay est: $t_{dr} = t_{df} = 1.2\tau$; $\tau = R_{eq}C$; $R_{eqn} = 2.5/(\mu_n C_{ox}(W/L)_n(V_{DD} - V_{tn}))$; $R_{eqp} = 2.5/(\mu_p C_{ox}(W/L)_p(V_{DD} + V_{tp}))$;
$(W_p/W_n)_{opt} = \sqrt{\mu_n/\mu_p}$ **Unit delay est:** $t_{df2}/t_{df1} = (C_{L2}/C_{L1}) \times ((W/L)_{n1}/(W/L)_{n2})$

Min delay: $t_{delay} = \tau_{inv}(C_{out}/C_{in})$; $\text{total}_{delay} = Nf\tau_{inv}$; $f^N = C_{out}/C_{in}$; usually $f = 4$

Power diss: $P_{dyn} = P_{1\to 0} f C_L V_{DD}^2$; $P_{dp} = 0.5 P_{1\to 0} f V_{DD} I_{peak}(t_r + t_f)$; $I_{peak} = 0.5\beta_n(V_{TH} - V_{tn})^2$;

Elmore Delay: $\tau_i \cong \sum_k C_k R_{ik}$; dist RC, $\tau \cong RC/2$;

Interconnect: $R = (\rho l)/(tw)$; $R_\square = \rho/t$; $C = (\varepsilon_{ox} wl)/t$; $C = \varepsilon_{ox} l(w/h + 0.77 + 1.06(w/h)^{0.25} + 1.06(t/h)^{0.5})$;

Max delay constraint: $T_c \geq t_{pcq} + t_{pd} + t_{setup}$ **Min Delay constraint:** $t_{hold} \leq t_{ccq} + t_{cd}$ **Metastability:** $\text{MTBF} = e^{T/\tau_s}/(t_{rd} F_D F_{CLK})$

SRAM: M3 is cell access transistor, M1 is inverter NMOS, M5 is inverter PMOS,

SRAM read: $W_1/W_3 \geq (V_{DD} - V_A - V_{tn})^2/(2((V_{DD} - V_{tn})V_A - V_A^2/2))$; $I_{cell} = ((\mu_n C_{ox})/2)(W_3/L)(V_{DD} - 2V_{tn})^2$
$\Delta V_{BL} = (I_{cell}\Delta t)/C_{BL}$

SRAM write: $W_3/W_5 \geq (\mu_p(V_{DD} + V_{tp})^2)/(2\mu_n((V_{DD} - V_{tn})V_A - V_A^2/2))$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9$V

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	0.3
PMOS	-0.4	0.4	30	0.1	6	0.3	2	0.3

V_{T0} is the threshold voltage with zero bulk-source voltage; γ is used to account for non-zero bulk-source voltage; μC_{ox} is the transistor current gain parameter; λ is to account for the transistor finite output impedance (channel length modulation); C_{ox} is the gate capacitance per unit area; C_o is the gate overlap capacitance per unit length; C_j is the drain/source junction capacitance per unit area; C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters