Chapter 16 - Problems

16.1) $f_{osc} = 10\ MHz + (V_{cntl} - 2.5)5\ MHz \Rightarrow K_{osc} = 2\pi \times 10^7\ rad/V.s$

$\tau_{PLL} = 50\ \mu s \Rightarrow \omega_0 = \frac{1}{\tau_{PLL}} = 20\ k\ rad/s$

$K_{pd} = \frac{V_{DD}}{\pi} = 1.59\ V/rad$. $K_{PLL} = \sqrt{K_{pd} K_{lp} K_{osc}} = 9995\ s^{-1/2}$

Using (16.32) : $\tau_p = 0.25\ sec$

Using (16.36) : $\tau_z = 0.1\ msec$

choosing arbitrarily $C_1 = 100\ nF \Rightarrow R_2 = \frac{\tau_z}{C_1} = 1K\Omega$

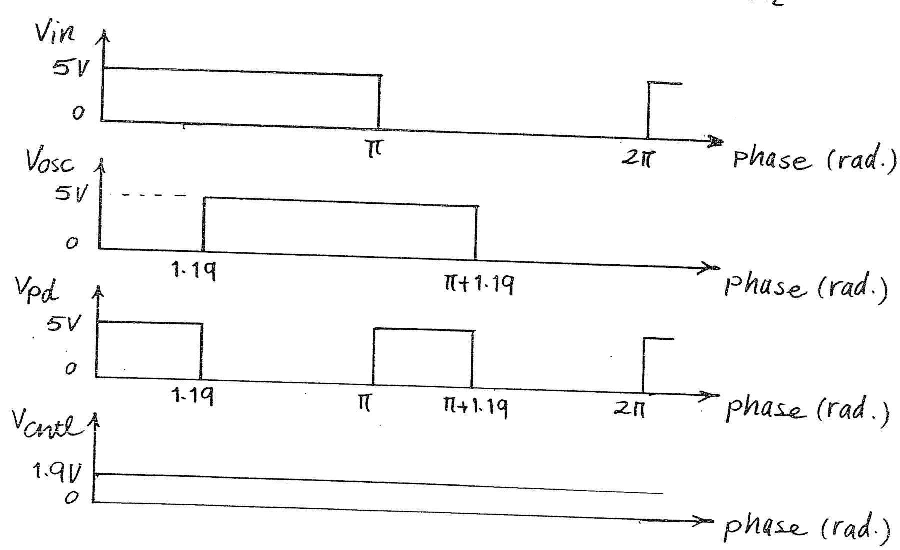
$R_1 = \frac{\tau_p}{C_1} - R_2 = 2.5 M\Omega$

$f_{osc} = 7MHz \Rightarrow V_{cntl} = 1.9\ V \Rightarrow \Delta\phi_{in} = \frac{1.9\ V}{K_{pd}} = 1.19\ rad.$

$1 < V_{cntl} < 4 \Rightarrow 2.5\ MHz < f_{osc} < 17.5\ MHz$

Deglitching Capacitor C_2 can be chosen to be : $C_2 = \frac{C_1}{10} = 10nF$

C_2 has little effect on the PLL performance since the high-frequency gain of the filter is very small ($\frac{R_1}{R_2} < 0.001$) !



16.2) $K_{pd} = 3\,V/rad$, $K_{osc} = 2\pi \cdot 50\,k\,rad/V.s$

$Q = 0.707$, $\tau_p = \frac{1}{2\pi f_p} = \underline{31.8\ \mu sec}$

$f_{osc} = 5\,MHz + V_{cntl} \cdot 50\,KHz$

In order to have a lock range of $\pm 100\,KHz$, we must have:

" $-2V < V_{cntl} < 2V$ ".

$K_{pd} = 3V/rad \Rightarrow \underline{A = 2/3}$

Using (16.34) : $\underline{K_{PLL} = 792.7\ s^{-1/2}}$

Using (16.33) : $\underline{\tau_z = 8.5\,\mu sec}$

Choosing arbitrarily $\underline{C_1 = 10\,nF} \Rightarrow R_2 = \frac{\tau_z}{C_1} = \underline{847\,\Omega}$

$R_1 = \frac{\tau_p}{C_1} - R_2 = \underline{2333\,\Omega}$

The lock range will increase with an increase in gain if V_{cntl} is not limited by the VCO design.

16.3) From (16.9): $V_{cntl} = K_{pd} K_{lp} \sin\phi$

The linearized model of this equation at $\phi = 0$ is:

$$\Delta V_{cntl} = K_{pd} K_{lp} \Delta\phi \qquad (at\ \phi = 0)$$

At the frequency half-the-lock-range away from f_{fr},

$\sin\phi = \frac{1}{2}$ or $\phi = \pi/6$. At this phase, the linearized model is:

$$\Delta V_{cntl} = \left(\frac{\sqrt{3}}{2} K_{pd}\right) K_{lp} \Delta\phi \qquad (at\ \phi = \pi/6)$$

Which means K_{pd} has effectively been reduced (cont.)

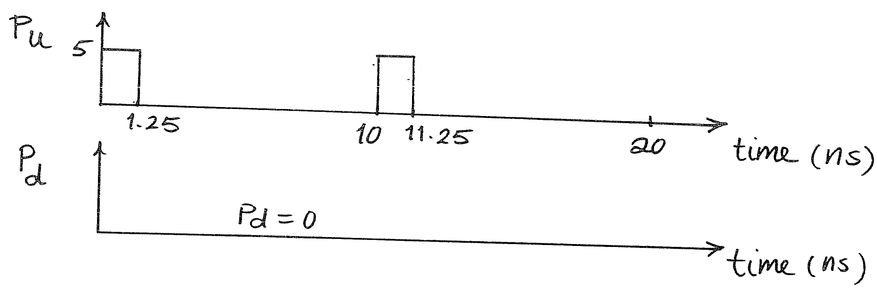
16.3) (cont.) by a factor of $\frac{\sqrt{3}}{2}$. Using (16.32) & (16.35):

$\omega_o = 0.93\ \omega_o\text{(original)}$ & $Q = 1.07\ Q\text{(original)}$

16.4) $f_{osc} = 50\ MHz \Rightarrow T_{osc} = 20\ nsec.$

Therefore, a phase difference of $\frac{\pi}{8}$ corresponds to:

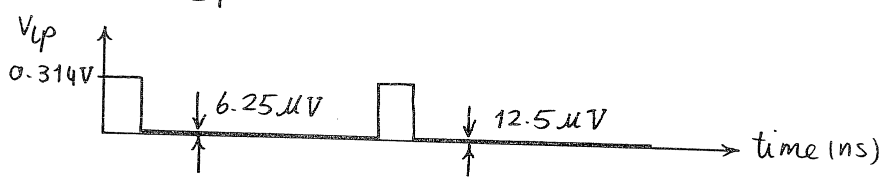
$$\frac{20\ ns}{2\pi} \times \frac{\pi}{8} = 2.5\ ns$$



Case I) without C_2: the initial V_{cp} jump is $I_{ch}R = 0.314V$!

The voltage increment by V_{cp} during half a period is

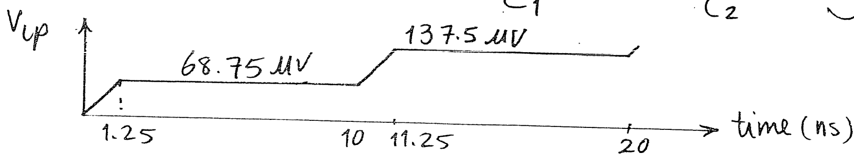
$$\frac{I_{ch} \times 1.25\ ns}{C_1} = 6.25\ \mu V$$



Case II) With C_2: the initial jump is 0 (note that

$RC_2 = 6.28\ \mu s$, ∴ jump during 1.25ns is filtered)

the voltage increment: $\frac{I_{ch} \times 1.25n}{C_1} + \frac{I_{ch} \times 1.25n}{C_2} = 68.75\ \mu V$



16.5) A time constant of 0.5 μs corresponds to

$$\omega_0 = \frac{1}{0.5\mu s} = 2\ M\ rad/s.$$

Using (16.56) and (16.60), we have:

$$C_1 = \frac{1}{\omega_0^2}\frac{I_{ch}}{2\pi}K_{osc} = \underline{62.5\ pF}$$

Let $C_2 = C_1/10 = \underline{6.25\ pF}$.

Let $Q = 0.4$, from (16.61): $R = \frac{1}{Q}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}} = \underline{20\ K\Omega}$

16.6) Since the phase detector of Fig. 16.9 is symmetric with respect to V_{in} and V_{osc}, the voltage waveform for the case $f_{osc} \gg f_{in}$ are the same as those shown in Fig. 16.10 with V_{in}, P_u, and $P_{u\text{-}dsbl}$ interchanged with V_{osc}, P_d, and $P_{d\text{-}dsbl}$, respectively.

16.7) $$f_{fr} = \frac{I_1}{4V_D C_{osc}}.$$

Assuming $V_D \approxeq 0.7\ V \Rightarrow 10\ M = \frac{I_1}{2.8\ C_{osc}} \Rightarrow \frac{I_1}{C_{osc}} = 28\ M$

Choosing $\underline{C_{osc} = 0.5\ pF} \Rightarrow \underline{I_1 = 14\ \mu A}$

$V_D\ (T_{nom} + 20^\circ) = 700\ mV - 20 \times 2\ mV = 0.66\ V$

$$\Rightarrow f_{fr}(T_{nom} + 20^\circ) = \frac{14\ \mu}{4 \times 0.66 \times 0.5p} = \underline{10.6\ MHz}$$

16.8) Since $f_{osc} \propto V_{DD}$:

$$f_{osc}\Big|_{V_{DD}=5.5V} = \frac{5.5}{5} f_{osc}\Big|_{V_{DD}=5V} = 1.1\ f_{osc}\Big|_{V_{DD}=5V}$$

That is a 10 % increase in the frequency of osc.

$$\text{Time-Jitter} = T_{osc}(5V) - T_{osc}(5.5V) \simeq 0.1\ T_{osc}(5V)$$

16.9) Assuming a small differential voltage can switch the inverter, the delay of each stage is the time required for each output to change by $V_{ref}/2$.

$$V_o(t) = V_{ref}\left(1 - e^{-\tau_{inv}/RC_L}\right) = V_{ref}/2 \Rightarrow \tau_{inv} = RC_L \ln 2$$

Also, $R = V_{ref}/I_b$. Therefore, $f_{osc} = \dfrac{I_b}{nV_{ref}C_L \ln 2}$

where n is the number of stages.

16.10) Using the result of the previous problem, and noting $I_b = \dfrac{V_{cntl}}{R}$, we have: $f_{osc} = \dfrac{V_{cntl}}{nV_{ref}RC_L \ln 2}$

For $n=4$, $V_{ref}=1V$, $R=100\,K\Omega$, $C_L=0.1\,pF$, and $V_{cntl}=1V$:

$f_{osc} \simeq 36\,MHz$, $K_{osc} = 2\pi \cdot 36\ MHz/s.V$

16.11) If t_1 = "the time required to discharge C_1 from V_{DD} to V_{ref}"

t_2 = "the time " " " C_2 " " " "

Then: $T_{osc} = t_1 + t_2$

Using $I = \frac{V_{cntl}}{R}$ & $I = C\frac{dV}{dt} \Rightarrow t_1 = \frac{V_{cntl}}{RC_1(V_{DD} - V_{REF})}$

& $t_2 = \frac{V_{cntl}}{RC_2(V_{DD} - V_{REF})}$

$$f_{osc} = \frac{1}{t_1 + t_2} = R\,\frac{C_1 C_2}{C_1 + C_2}\,\frac{V_{DD} - V_{REF}}{V_{cntl}}$$