micromanipulator. Deposition of dots and lines with diameters and widths ranging from 80 nm to some tens of microns are achieved by the application of voltage pulses between 0·5 V and 20 V with 0·5 μs to 1 ms length. An example is shown in Fig. 2. Control of ionic current is possible because

Fig. 2 *Au line deposited on GaAs by electrolytic direct writing process*

of the small size of the tip, the glass insulation and the short pulses applied. Deposition of dots is possible with single pulses, tip retraction, and discharging of the tip between pulses. Writing of lines is possible without retraction and discharging. The structure size is mainly influenced by the radius of the tip and the amount of transported charge depending on the pulses. Linewidth is additionally influenced by the tip movement between the pulses. The mechanism of deposition can be understood by a model, recently presented by Jacobs *et al.*[9] The GaAs surface in contact with the electrolyte is depleted and the application of voltage lowers the barrier for electrons so that Au^+ ions are deposited. Small nuclei, already deposited, lower the barrier compared to other parts of the surface and preferential deposition occurs at these nuclei. These effects allow direct writing of dots and lines. Other metals can of course be similarly deposited.[10]

Conclusion: New processes for etching and metallisation of GaAs in the submicron range have been presented. By the use of electrolytic solutions in pulsed operation, soft etching of GaAs towers with 300 nm diameter and deposition of Au-dots and lines down to 100 nm are easily established. Electrolytic etching appears to be promising for the fabrication of quantum dot or well structures with reduced surface damage compared to dry etching. Metal deposition can be used in split gate electrodes or lateral superlattice structures for electron confinement.

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IIR FILTERING ON SIGMA–DELTA MODULATED SIGNALS

Indexing terms: Filters, Digital filters

A design methodology for realising IIR filters on sigma–delta modulated signals is proposed. It is shown that only $3N$ adders together with minor logic are required to implement an Nth order filter. This type of filtering should prove useful in VLSI technologies where interfaces to analogue signals are required.

Introduction: The use of sigma–delta (Σ–Δ) modulation has been shown to be an effective method for building high resolution analogue-to-digital (A/D) and digital-to-analogue (D/A) convertors.[1,2] Thus, performing signal processing on Σ–Δ modulated signals is desirable as this type of processing could be integrated with other systems in VLSI where interfaces to analogue signals are required. Towards this goal, a recent publication describes a method of realising finite-impulse-response (FIR) filters operating on such signals,[3] however, there is presently no method for realising equivalent infinite-impulse-response (IIR) filters. The purpose of this Letter is to propose such an IIR filter design methodology. We will show that to realise an Nth order filter using second-order Σ–Δ modulators, only $3N$ adders are required together with some minor logic. This IIR approach should result in smaller VLSI implementations than their FIR counterparts in applications where the oversampling ratio is high and a low-order IIR response can replace a high-order FIR response.

Design approach: The method proposed here makes use of standard IIR filter structures except that filter states exist as both multibit and 1 bit signals. The 1 bit signal is obtained by modulating the multibit signal using a fully digital Σ–Δ modulator. A digital second-order Σ–Δ modulator is shown in Fig. 1 where the input and output signals are multibit and 1 bit, respectively.[4] The block $q(\cdot)$ is a 1 bit quantiser implemented by simply taking the most significant bit. The implementation complexity of this modulator can be simplified to two adders if 2's complement arithmetic is used. This low complexity is due to the first and third adders being realisable by simply changing the sign-bit of the multibit signal because the value

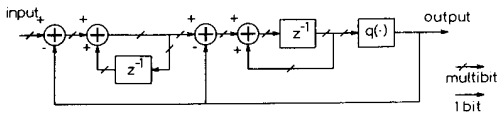

Fig. 1 *Double loop Σ–Δ modulator*
$q(\cdot)$ denotes the 1 bit nonlinear quantisation function

added is either the positive or negative maximum value. In terms of the transfer-function of this modulator within the baseband frequency of interest, the transfer-function appears to be simply z^{-1} (i.e. a single delay stage at the oversampled rate). This fact is used in the design of the IIR filters to be described.

To illustrate the proposed approach, consider first the circuit shown in Fig. 2. A 1 bit input signal $u(n)$ operating at

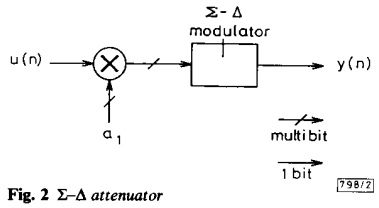

Fig. 2 *Σ–Δ attenuator*
At baseband $Y(z) = a_1 z^{-1} U(z)$

the oversampled rate is multiplied by a multibit fixed coefficient a_1 and the resulting multibit signal is injected into a digital Σ–Δ modulator giving the output 1 bit signal $y(n)$. In the baseband frequency of interest, it is clear that this circuit behaves as an attenuator circuit, although the modulator does add extra noise to the baseband signal. In terms of hardware complexity, because $u(n)$ is a 1 bit signal, the multiplier can be efficiently realised as a 2-input multiplexer (simply changing the sign bit is not sufficient as 2's-complement arithmetic is assumed in order to realise efficient adders). This multiplexer approach results in the multiplier requiring about $4k$ transistors in CMOS technology for a k-bit coefficient. For comparison, a k-bit multiplier requires about $20k^2$ transistors. All multipliers shown in this Letter are of this multiplexer type, a critical requirement as they must operate at the oversampled rate.

As mentioned above, the Σ–Δ IIR filtering proposed here can be applied to standard IIR filter structures. However, structures with good performance for oversampled transfer-functions should be used because these types of functions are a natural consequence of using Σ–Δ modulation. One such structure is a recently developed quasiorthonormal state-space structure.[5] Making use of this structure and the attenuator circuit, described above, results in the Nth-order IIR filter shown in Fig. 3. Each multibit state signal $x_i(n)$ is applied to a Σ–Δ modulator resulting in a 1 bit signal $\hat{x}_i(n-1)$ that closely approximates $x_i(n-1)$ over the baseband frequency. Note

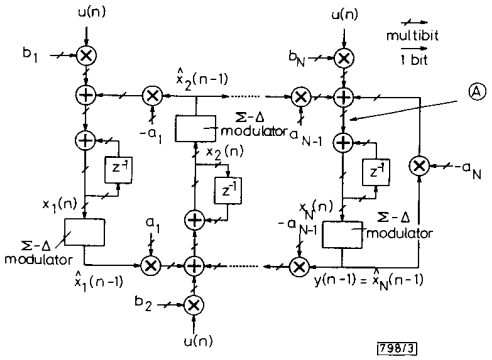

Fig. 3 *Nth order Σ–Δ IIR filter using quasiorthonormal structure*
Note that all multiplications involve a single bit signal

that all the additions shown in Fig. 3 need not be realised as adders. For example, the signal at node A takes on only one of eight possible values and is therefore more efficiently realised as an eight-input multiplexer rather than two adders. In fact, the only adders required are the two in each modulator and one for each filter state. With these simplifications, it is clear that for an Nth order filter using second-order Σ–Δ modulators, only $3N$ adders are required together with some minor logic. This low amount of complexity should make this type of filtering very economical in a VLSI technology.

Simulation results: To demonstrate the validity of this approach, a fifth-order prototype filter was simulated for three different oversampling ratios, $R = 32$, 64, and 128. To measure the frequency response, sine waves at varying frequencies were first passed through a Σ–Δ modulator, then the filter, and finally an FFT and Hamming window of the resulting one-bit stream indicated the magnitude response at the sine wave's frequency. Although this method of measurement is much more computationally intensive than using an impulse response (as in Reference 3), it allows more power at each frequency and therefore gives a more realistic estimate of the signal-to-noise performance of the filter. The frequency responses for the three filters along with the ideal response are shown in Fig. 4. Here, we see that the signal-to-noise performance improves for higher oversampling ratios, as expected.

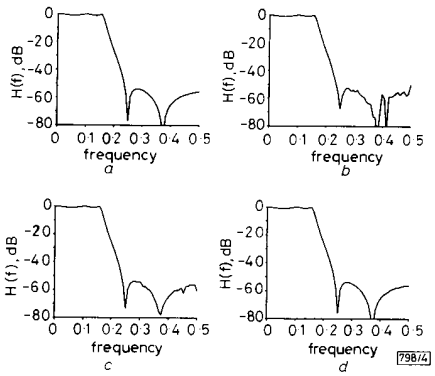

Fig. 4 *Frequency responses of fifth-order lowpass filter for varying values of oversampling ratio R*
a ideal
b $R = 32$
c $R = 64$
d $R = 128$

Conclusions: A design methodology for realising IIR filters on Σ–Δ modulated signals was proposed. The method makes use of standard IIR filter structures except that multibit filter states also exist as one-bit signals obtained by modulating the multibit signals. It was shown that only $3N$ adders together with minor logic are required to implement an Nth order filter using second-order modulators. Future work involves performing a comprehensive noise analysis and investigating other filter structures. This type of filtering should prove useful in VLSI technologies where interfaces to analogue signals are required.

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