A High-Quality Analog Oscillator Using Oversampling D/A Conversion Techniques

Albert K. Lu, Gordon W. Roberts, *Member, IEEE,* and David A. Johns, *Member, IEEE*

Abstract—**This paper describes a high-quality analog oscillator for low-frequency applications, which uses a combination of oversampling and delta-sigma modulation. With the exception of a lowpass filter and a 1-bit D/A, the proposed circuit is entirely digital, providing accurate control over the oscillation frequency and amplitude. At the core of the oscillator is a digital simulation of an *LC*-tank circuit consisting of two cascaded integrators. This arrangement guarantees oscillation by constraining the poles of the resonator to locations on the z-plane unit-circle, even in a finite-precision implementation. To minimize circuit complexity, the entire oscillator is operated at the oversampled rate, thereby eliminating the associated interpolation filter. Furthermore, the incorporation of a delta-sigma modulator inside the resonator loop leads to a very efficient implementation requiring only 4 multi-bit adders and a 2-input multiplexor. The desired analog signal may be recovered by lowpass filtering the 1-bit output of the delta-sigma modulator. Experiments performed thus far have indicated an effective dynamic range exceeding 80 dB.**

I. Introduction

As a result of advancements in *Digital-to-Analog* (D/A) converter technology, analog sinusoidal signals are commonly generated using a combination of *Digital Signal Processing* (DSP) and D/A conversion. Furthermore, for low-frequency applications, oversampling delta-sigma D/A converters have gained in popularity due to their high linearity [1]. For this reason, the task of generating analog signals can be reduced to one of generating the equivalent digital waveforms.

Arbitrary digital sinusoidal signals may be generated using *Direct Digital Frequency Synthesis Techniques* (DDFS). These circuits offer the advantage of fast switching speeds and good frequency resolution. Nonetheless, the sine function, which is computationally intensive to calculate, must be computed using a ROM-based look-up table approach [2]. Although generalized compression algorithms [3] and noise-shaping techniques [4] can be used to minimize the size of the ROM, the resulting hardware requirement may still be unacceptable in applications such as *Built-In-Self-Test* (BIST) [5]. In another approach, a *Lossless Discrete Integrator* (LDI) biquad filter [6] is constructed as a component simulation of an *LC*-tank circuit. In doing so, the poles of the circuit are constrained to lie on the unit-circle of the z-plane, and the desired oscillation frequency can be selected through precise adjustment of the pole locations [7]. While this approach incorporates programmability, it requires at least 1 multi-bit multiplier and an interpolation filter.

This paper describes a high-quality analog oscillator for low-frequency applications, which uses a combination of oversampling and delta-sigma modulation. The oscillator structure is based on the LDI biquad circuit described earlier. However, in this case, no interpolation filter is required since the entire circuit is operated at the oversampled rate. Furthermore, by incorporating a delta-sigma modulator inside the resonator loop, multi-bit multiplications can be avoided resulting in an efficient implementation. If the output is taken at the delta-sigma output, multi-bit D/A conversion is not necessary and the analog signal may be recovered by lowpass filtering the single-bit stream.

The outline of this paper is as follows. Section II begins by developing the fundamental concepts which support the proposed design. Here, parallels are drawn between the well-known *LC*-tank circuit and the proposed oscillator. Equations relating the frequency and amplitude of the oscillatory tone are derived and presented in terms of the programmable circuit parameters. In Section III, a realization of the oscillator is presented. At this point, techniques used to minimize the total circuit area are discussed. Finally, simulated and experimental results of the design are presented in Sections IV and V respectively.

II. Background Theory

A complete synthesis procedure exists for the design of digital filters based on *LC*-ladder networks [8]. The structure of the resulting digital filter is generally formed from a set of coupled second-order resonators. These resonators are formed by cascading two discrete-time integrators of the form $z^{-1}/(1-z^{-1})$ and $1/(1-z^{-1})$ in a loop with the sign of one integrator being positive and the other negative. This arrangement is shown in Fig. 1. As a result of this approach, digital filter circuits with excellent noise and sensitivity properties are known to exist [9].

As a special case of this synthesis procedure, a digital oscillator may be realized by eliminating the effect of damping in the filter. By doing so, the resonant circuit of Fig. 1 may be used as a digital oscillator. In studying this circuit, it is useful to consider its analog counterpart, the *LC*-tank circuit in Fig. 2, as it reveals many of its interesting properties. Being a lossless circuit, it follows that once the *LC*-tank is excited,

Manuscript received July 21, 1993; revised January 3, 1994. This work was supported by NSERC and by the Micronet, a Canadian federal network of centers of excellence dealing with microelectronic devices, circuits and systems for ultra large scale integration. This paper was recommended by Associate Editor V. Gopinathan.

A. K. Lu and G.W. Roberts are with the Department of Electrical Engineering, McGill University, 3480 University Street, Montreal, PQ, Canada H3A 2A7.

D. A. Johns is with the Department of Electrical Engineering, University of Toronto, 10 King's College Road, Toronto, Ont., Canada M5S 1A4.

IEEE Log Number 9403062.

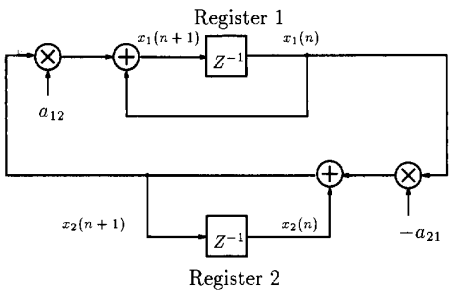


Fig. 1. A second-order digital resonator circuit consisting of a cascade of two integrators in a loop.

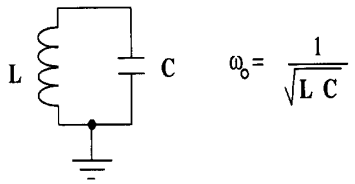


Fig. 2. A simple harmonic oscillator: a parallel *LC* tank circuit.

no energy is lost but instead alternates between electric and magnetic forms. The resulting capacitor voltage and inductor current waveforms represent ideal sinusoids with frequency $\omega_o = 1/\sqrt{LC}$.

Two facts are important to note about the energized *LC*-tank circuit:

1) variations in the capacitor or inductor values do not prevent the circuit from oscillating, but merely shift the frequency of oscillation
2) The amplitude of oscillation is a function of the initial conditions imposed on the capacitor and inductor.

Returning to the second-order digital resonator of Fig. 1, it appears from the first observation that variations in the coefficients a_{12} and a_{21} (corresponding to L and C in the tank circuit) may cause shifts in the oscillation frequency but will not prevent the circuit from oscillating. Furthermore, the second observation suggests that the amplitude of the oscillatory tone will be a function of the initial conditions imposed on registers 1 and 2. These conclusions are easily verified through careful observation of the resonator's characteristic equation. Denoting the values in registers 1 and 2 of Fig. 1 at time $t = nT$ by $x_1(n)$ and $x_2(n)$ respectively, the two difference equations characterizing the oscillator are,

$$x_1(n+1) = x_1(n) + a_{12}x_2(n+1) \tag{1}$$

$$x_2(n+1) = -a_{21}x_1(n) + x_2(n). \tag{2}$$

Using z-transforms, $x_2(n)$ may be eliminated resulting in a single equation in $x_1(n)$. The result, with $X_1(z)$ representing the z-transform of $x_1(n)$, is the following

$$z^2X_1(z) + (a_{12}a_{21} - 2)zX_1(z) + X_1(z) = 0. \tag{3}$$

Furthermore, the characteristic equation is given by

$$z^2 + (a_{12}a_{21} - 2)z + 1 = 0. \tag{4}$$

The location of the circuit poles may be determined by finding the roots of the above equation. Solving the quadratic in z yields,

$$z_{1,2} = \left(1 - \frac{a_{12}a_{21}}{2}\right) \pm \frac{1}{2}\sqrt{a_{12}a_{21}(a_{12}a_{21} - 4)}. \tag{5}$$

If the product $a_{12}a_{21}$ is restricted to values between 0 and 4, the discriminant of the above expression will always be negative, yielding complex roots. Moreover, for

$$0 < a_{12}a_{21} \leq 2,$$

corresponding to roots in the right-half plane, the two roots may be written using polar notation as,

$$z_{1,2} = e^{\pm j\cos^{-1}\left(1 - \frac{a_{12}a_{21}}{2}\right)}. \tag{6}$$

Similarly, for

$$2 < a_{12}a_{21} < 4,$$

corresponding to solutions in the left-half plane, the roots are positioned according to the following equation,

$$z_{1,2} = e^{\pm j\left(\pi - \cos^{-1}\left(1 - \frac{a_{12}a_{21}}{2}\right)\right)}. \tag{7}$$

From (6) and (7) it is evident that the roots of the characteristic equation must lie on the unit-circle for all values of the product $a_{12}a_{21}$ between 0 and 4. As a result, oscillation is guaranteed. In addition, the precise frequency of oscillation ω_o may be obtained directly from the phase terms of (6) and (7). Assuming the resonator is clocked at a rate $f_{os} = \frac{1}{T}$, the expression for ω_o will take the following form:

$$\omega_o = \begin{cases} f_{os}\cos^{-1}\left(1 - \frac{a_{12}a_{21}}{2}\right) & \text{for } 0 < a_{12}a_{21} \leq 2 \\ f_{os}\pi - f_{os}\cos^{-1}\left(1 - \frac{a_{12}a_{21}}{2}\right) & \text{for } 2 < a_{12}a_{21} < 4. \end{cases} \tag{8}$$

Fig. 3 illustrates the relationship between the oscillation frequency and the product $a_{12}a_{21}$. For values of $a_{12}a_{21}$ between 0 and 4, the oscillation frequency varies continuously between 0 and $f_{os}/2$. If however, the coefficients are limited to discrete values (which is the case in a finite-precision implementation), the selectable oscillation frequencies will also be limited to discrete values. Nonetheless, as mentioned earlier, because the poles of the circuit remain on the unit circuit for all values of $a_{12}a_{21}$ betwen 0 and 4, the circuit is guaranteed to oscillate even in a finite-precision implementation.

The second point, which may be drawn from the *LC*-tank analogy, is the fact that the amplitude of oscillation may be controlled through the initial conditions of the circuit. To see this, consider once again the two difference equations given in (1) and (2). From the previous z-plane analysis, it is apparent that the solution of these difference equations is a single tone of frequency ω_o. By assuming a solution of the form,

$$x_1(n) = A\sin(\omega_o nT + \phi), \tag{9}$$

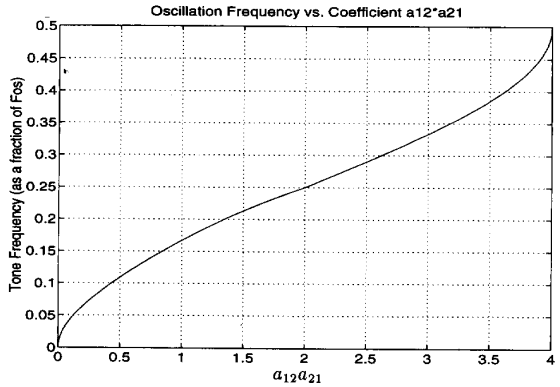


Fig. 3. Illustrating the functional relationship between oscillation frequency (as a fraction of the sampling frequency f_{os}) and the product $a_{12}a_{21}$.

with $T = \frac{1}{f_{os}}$, the values contained in registers 1 and 2 at sampling instants $n = 0$ and $n = 1$ are

$$x_1(0) = A\sin(\phi) \tag{10}$$

and

$$x_1(1) = A\sin(\omega_o T + \phi). \tag{11}$$

Furthermore, by combining (1) and (2), an expression relating the state of register 1 at sampling instant $n = 1$ to the values initially stored in registers 1 and 2 may be obtained, and is given by

$$x_1(1) = (1 - a_{12}a_{21})x_1(0) + a_{12}x_2(0). \tag{12}$$

Finally, by combining (10), (11), and (12), the two unknown constants, A and ϕ, may be solved for in terms of the two initial register values. The resulting equations are given below.

$$A = \frac{(1 - a_{12}a_{21})x_1(0) + a_{12}x_2(0)}{\sin(\omega_o T + \phi)} \tag{13}$$

$$\phi = \tan^{-1}\left(\frac{x_1(0)\sin(\omega_o T)}{(1 - a_{12}a_{21} - \cos(\omega_o T))x_1(0) + a_{12}x_2(0)}\right) \tag{14}$$

To demonstrate the properties of (13), two graphs are presented in Figs. 4 and 5 which show the sinusoidal amplitude as a function of the initial register conditions. Here, the coefficients a_{12} and a_{21} have been chosen arbitrarily and do not affect the general characteristics of the relationship. Specifically, the values $a_{12} = 2^{-6}$ and $a_{21} = 0.0068796752790$ were selected, corresponding to an oscillation frequency of $0.00165301 \times f_{os}$. Fig. 4 illustrates how the amplitude of oscillation varies with the initial value of register 1. In this plot, register 2 has been assigned an initial value of zero. In a similar way, Fig. 5 illustrates the reverse situation: how the amplitude varies with the initial value set in register 2. Here, the initial value of register 1 has been set equal to zero. As indicated by both plots, the relation is very near linear with respect to the initial conditions.

Realization of a digital oscillator in this manner has recently been demonstrated by Turner [7]. The following section explains how this digital oscillator may be incorporatated in the design of a low-frequency, analog oscillator.

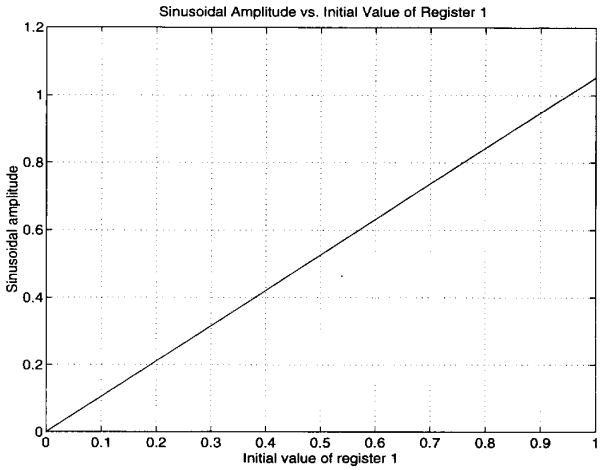


Fig. 4. Oscillation amplitude as a function of the initial value in register 1.

III. An Area-Efficient Oscillator Circuit

The generation of an analog tone may be achieved easily by passing the output of the digital resonator through a *Digital-to-Analog Converter* (DAC). A typical 1-bit oversampling DAC is illustrated in Fig. 6 and consists of a digital interpolation filter, a delta-sigma modulator, and an analog reconstruction filter. As shown, the interpolation filter receives an N-bit word at rate f_n and upsamples it to a rate f_{os} (the oversampling frequency). This signal is then passed to the delta-sigma modulator where it is converted to a single-bit stream (at the same rate f_{os}) containing the original signal information plus shaped quantization noise. While the majority of this noise resides at high frequencies, it is the in-band component of the noise which ultimately limits the signal-to-noise ratio of the analog output signal after filtering. Defining the oversampling ratio (OSR) as the ratio of the oversampling frequency to the Nyquist rate

$$OSR \triangleq \frac{f_{os}}{2f_{BW}}, \tag{15}$$

it can been shown [1] that for a second-order modulator, the rms signal-to-noise ratio is related to the OSR according to

$$SNR_{rms} \approx \frac{\sqrt{60}}{\pi^2}(OSR)^{\frac{5}{2}}. \tag{16}$$

Equivalently, the in-band noise falls by 15 dB for every doubling of the sampling frequency, providing 2.5 extra bits of resolution. In practice, an OSR=128 makes in-band quantization noise consistent with 16-bit resolution possible [1]. With this in mind, both the oversampling frequency f_{os} and the signal bandwidth f_{BW} should be selected carefully to yield an acceptable OSR.

While cascading a digital resonator with a 1-bit DAC is a simple and viable method of analog signal generation, the large amount of silicon area required by the interpolation filter may be unacceptable in many applications (including BIST). An alternate design, described next, alleviates this problem by operating the entire resonator at the oversampling rate thereby

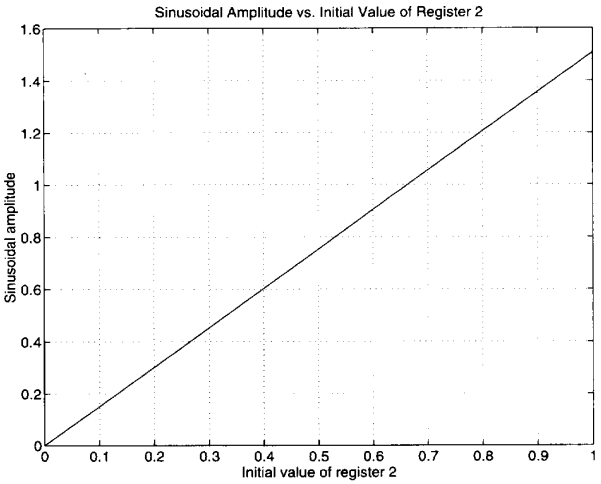


Fig. 5. Oscillation amplitude as a function of the initial value in register 2.

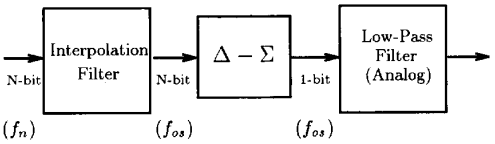


Fig. 6. Block diagram of a typical oversampled DAC.

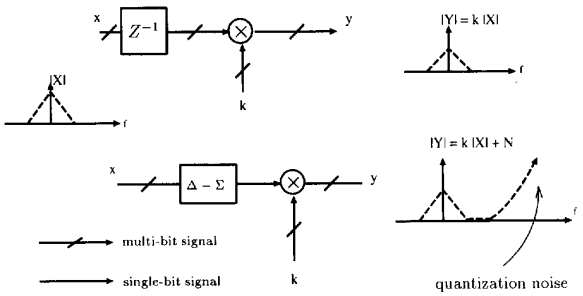


Fig. 7. Delta-sigma attenuator circuit. Except for the additional quantization noise at the output of the delta-sigma attenuator, the circuit performs the same multiplication operation as the N-by-N bit multiplier circuit.

eliminating the need for an interpolation filter. Furthermore, by moving the delta-sigma modulator inside the resonator loop, the two multi-bit multiplications may be simplified drastically resulting in a very efficient implementation.

Fig. 7 demonstrates how a unit-delay in series with an N-by-N multiplication, may be approximated by a delta-sigma modulator followed by a 1-by-N multiplication. As the output spectra indicate, the latter circuit, known as a *delta-sigma attenuator* [10], approximates the former accurately at low frequencies. Consequently, in cases where the signal information resides at low frequencies relative to the oversampling frequency f_{os}, the delta-sigma attenuator may be used to perform N-by-N bit multiplication. As will be seen later, this substitution is very advantageous since it simplifies the design drastically.

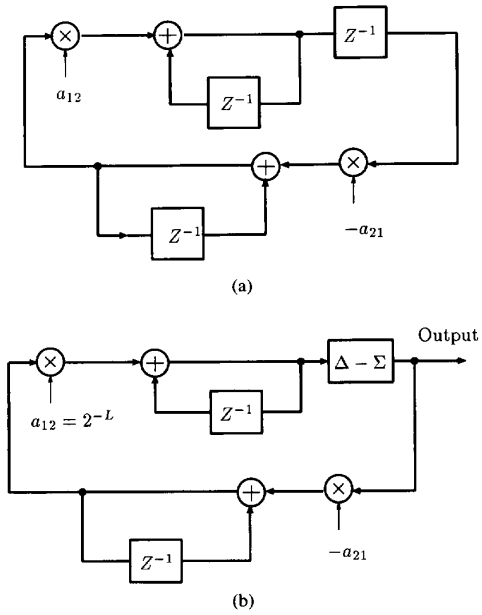


Fig. 8. (a) Re-arranged form of the digital resonator circuit of Fig. 1. (b) Replacing the N-by-N bit multiplier in series with the unit delay of part (a) by a delta-sigma attenuator circuit. The remaining N-by-N bit multiplier may be simplified by setting coefficient a_{12} to a fixed power of two.

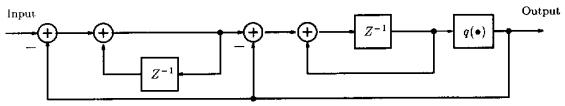


Fig. 9. A second-order digital delta-sigma modulator. The block $q(\bullet)$ represents a one-bit quantizer.

With the in-band model of the delta-sigma attenuator circuit in mind, the digital resonator circuit of Fig. 1 may be rearranged using a simple signal-flow-graph manipulation. Referring to the top integrator of Fig. 1, the unit-delay in the feedforward path may be moved into the feedback path if another unit delay is placed in series with the output. The resulting configuration is shown in Fig. 8(a). At this point, the unit-delay in series with the N-by-N bit multiplier may be replaced by the delta-sigma attenuator. The resulting circuit is shown in Fig. 8(b) where the delta-sigma modulator is assumed to be a second-order modulator of the type shown in Fig. 9. Notice that if the output of the resonator is taken directly from the output of the delta-sigma modulator, D/A conversion may be carried out by lowpass filtering the output bit-stream. The complexity of the analog filter will depend largely on the oversampling ratio and therefore may be reduced by increasing the oversampling frequency f_{os}.

To further reduce the complexity of the design, we recognize from (8) that the oscillation frequency ω_o, is a function of the product $a_{12}a_{21}$. This property has been exploited in Fig. 10 where a_{12} has been set to a fixed integer power of 2 and therefore may be implemented using a fixed shift of L to the right. Furthermore, because the delta-sigma output may only take on the values $+1$ and -1, the multiplication by a_{21} may

TABLE I
PARAMETERS USED IN THE SIMULATION OF THE RESONATOR IN FIG. 10
Comdisco Simulation Parameters

$f_o = \frac{\omega_o}{2\pi}$	a_{12}	a_{21}	$x_1(0)$	$x_2(0)$	f_{os}	Precision
4998 Hz	2^{-6}	0.00668796752790	0.0	0.015625	3.072 MHz	32 bits

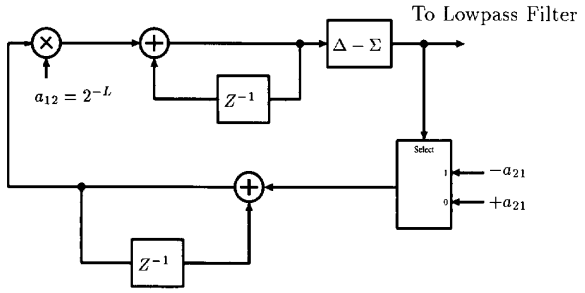


Fig. 10. Replacing the 1-by-N bit multiplier in the circuit of Fig. 8(b) with a 2-input multiplexor.

be achieved with a two-input multiplexor. The result, shown in Fig. 10, is a very efficient implementation requiring only 4 adders, 4 registers, and a 2-input multiplexor.

At this point, it should be noted that (13) and (14) describing the amplitude and phase of the oscillatory tone were derived for the original digital resonator of Fig. 1 and do not necessarily characterize the modified resonator of Fig. 10. Nonetheless, provided the analog oscillator is operated within the passband of the delta-sigma modulator, these equations have been found to approximate the modified circuit's behavior with exceptional accuracy. Experiments have confirmed amplitude accuracy exceeding 0.02% for $a_{12}a_{21} < 10^{-4}$ (corresponding to the delta-sigma passband).

IV. SIMULATION RESULTS

This section presents the results of digital simulations performed on the circuit in Fig. 10, using *Comdisco Systems'* DSP simulation tool [11]. The simulations were performed using 32-bit precision, and a two's complement number system with values ranging from -1 to $+1$.

With the coefficients and initial conditions as indicated in Table I, a transient analysis was executed for approximately 85 ms at a clock frequency $f_{os} = 3.072$ MHz. On completion, the spectral content of the single-bit output was studied using the *Fast Fourier Transform* (FFT). Although the exact dynamics of the system could not be characterized analytically, the simulated results were sufficient to verify that any start-up transient associated with the oscillator, only lasted for a short period of time and was of no great significance. For this reason, the FFTs shown in this section have been taken from time-zero with little consequence. Furthermore, Blackman windowing was incorporated in all cases to reduce the effects of spectral smearing. Fig. 11 shows the simulated output spectrum over a 20 kHz bandwidth. In this plot, the oscillatory tone may be seen roughly 80 dB above the distortion and noise. In Fig. 12,

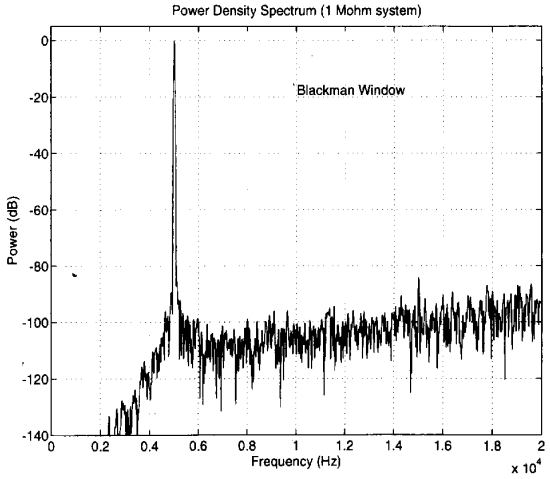


Fig. 11. Simulated output spectrum of the circuit in Fig. 10, clocked at 3.072 MHz.

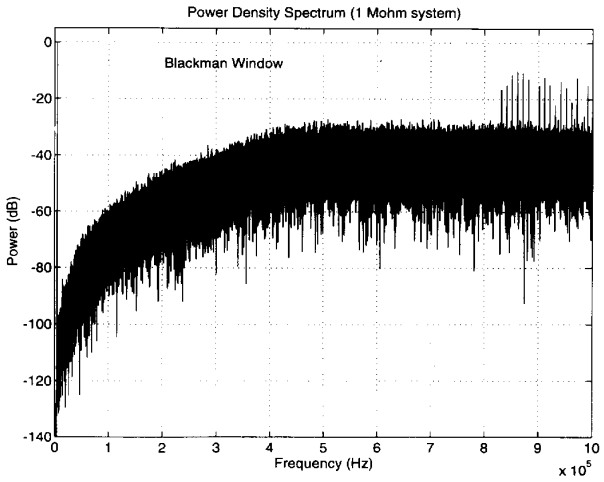


Fig. 12. Simulated broad-band output spectrum of the circuit in Fig. 10, clocked at 3.072 MHz.

the same output spectrum is shown over a 1 MHz bandwidth. Here, the noise-shaping characteristic of the second-order modulator may be observed.

To further investigate the circuit's performance, the simulation described above was repeated with a clock frequency $f_{os} = 15$ MHz. The resulting in-band spectrum is shown in Fig. 13. As expected, the increased sampling frequency improved the performance of the oscillator, increasing the dynamic range to approximately 110 dB.

TABLE II
PARAMETERS USED IN THE SIMULATION OF THE RESONATOR IN FIG. 10

FPGA Experimental Oscillator Parameters

$f_o = \frac{\omega_o}{2\pi}$	a_{12}	a_{21}	f_{os}	Precision
5000 Hz	2^{-6}	0.0066931955	3.07 MHz	33 bits

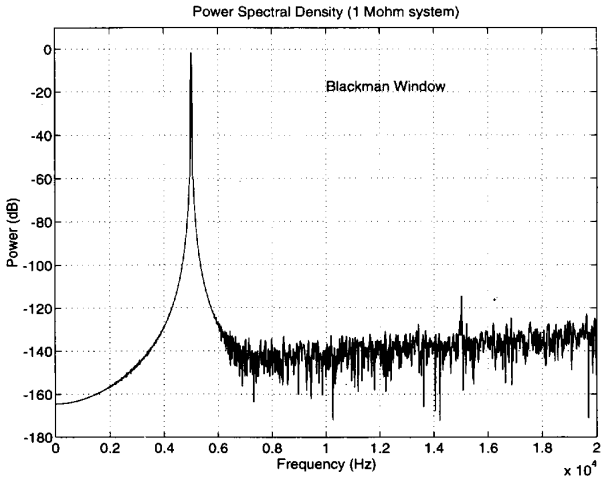


Fig. 13. Simulated output spectrum of the circuit in Fig. 10, clocked at 15 MHz.

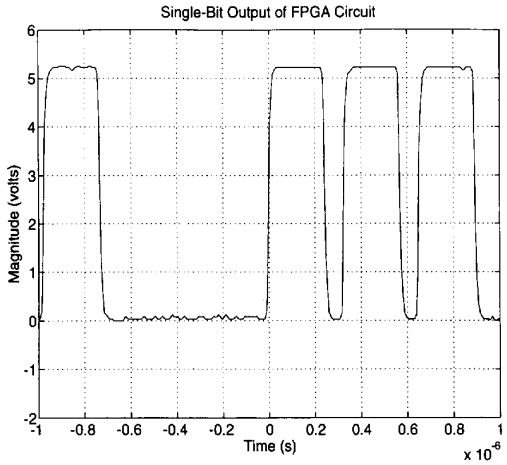


Fig. 14. Measured results of the delta-sigma modulated sine wave—time-domain signal prior to lowpass filtering.

V. EXPERIMENTAL RESULTS

At this point, the results of a *Field-Programmable Gate-Array* (FPGA) implementation of the oscillator are discussed. These results were collected using FPGA technology to realize the digital portion of the oscillator with a modified, commercially available evaluation board [12] performing the 1-bit D/A conversion and lowpass filtering operations.

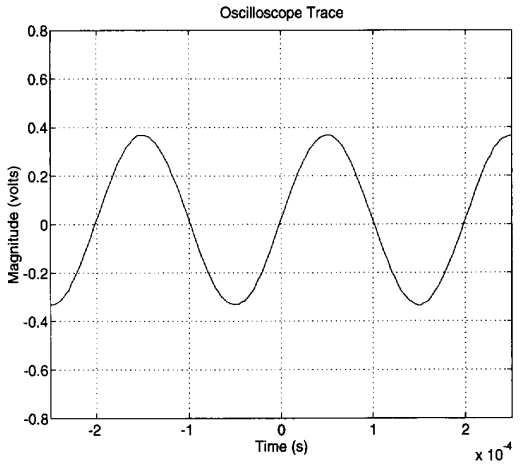


Fig. 15. Measured results of the delta-sigma modulated sine wave—time-domain signal after lowpass filtering.

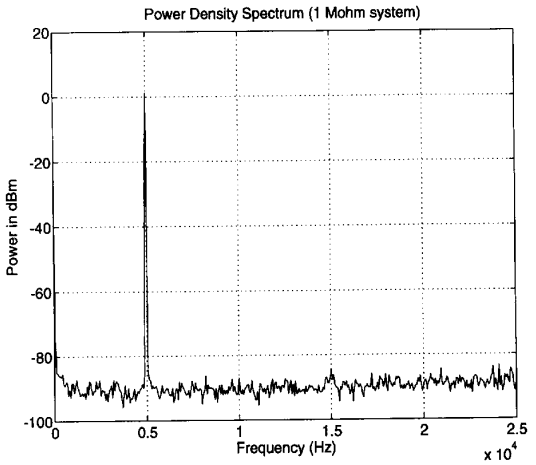


Fig. 16. Measured results of the delta-sigma modulated sine wave in-band spectrum over 25 kHz.

Figs. 14–16 contain the resulting waveforms of an experiment performed using the parameters listed in Table II. Fig. 14 depicts an actual oscilloscope trace of the 1-bit delta-sigma modulated output of the oscillator. Here, a return-to-zero coding scheme was adopted to minimize distortion. Therefore, during a logic 1, the signal was held high for 75% of the clock cycle before returning to zero for the remaining interval. During a logic 0, the signal simply remained low.

Fig. 15 illustrates the time waveform of the bit-stream in Fig. 14 after lowpass filtering by the 6th-order, Butterworth filter supplied on the evaluation board [12]. As expected, the output signal is indeed sinusoidal with an amplitude of approximately 0.35 V and a period of 0.2 ms, corresponding to a 5 kHz tone. The measured spectral plot of the output is given in Fig. 16. Here, the 5 kHz tone is visible with 2nd and 3rd harmonics, respectively roughly 88 dB and 86 dB below the fundamental.

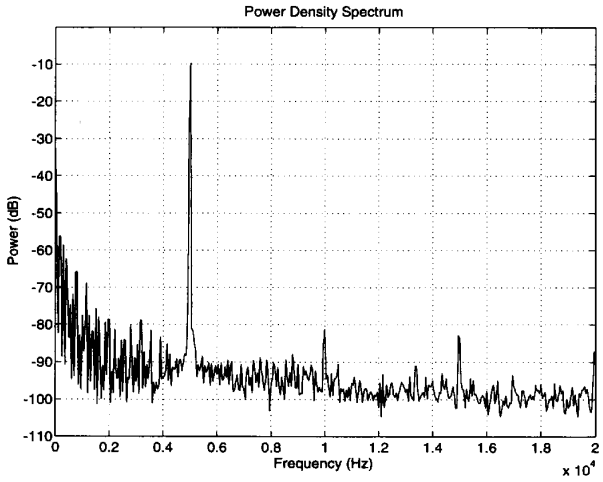


Fig. 17. Sample spectrum of a sinewave generated by an HP3314A signal generator.

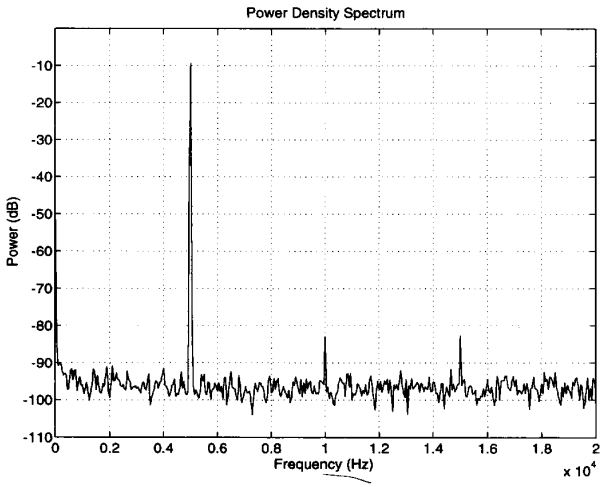


Fig. 18. Sample spectrum of a sinewave generated by an HP3245A signal generator.

It is worth noting that even at a resolution bandwidth of 88 mHz, no deviation in the oscillation frequency could be observed. Furthermore, the oscillator was operated continuously for over 24 hours at 5 kHz without difficulty. However, increasing the oscillation frequency to 20 kHz caused the circuit to overflow within a few minutes. The exact cause of this behavior is not presently known and is the topic of continued investigation. Nonetheless, if the oscillator is operated at low frequencies, relative to the oversampling frequency f_{os}, no problems should arise.

For the purpose of comparison, the output spectra of two reasonably-priced, low-frequency, sinewave generators have been included in Figs. 17 and 18. Fig. 17 shows the spectrum of an HP3314A Function Generator while the spectrum in Fig. 18 corresponds to the HP3245A Universal Source. Comparison of both plots with the results obtained in Fig. 16 indicates that the proposed design is indeed comparable to both sources.

VI. Conclusions

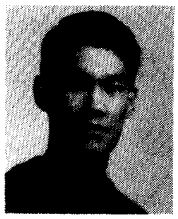
This paper has demonstrated a new technique for creating a high-quality analog oscillator using oversampling techniques. With the exception of an analog reconstruction filter, the circuit is completely digital, providing accurate control over the oscillation frequency and amplitude. Experiments performed to date have indicated an effective dynamic range exceeding 80 dB.

Acknowledgment

The authors wish to acknowledge Lysander Lim of the University of Toronto, Ontario, Canada, for performing the FPGA experiments appearing in Section V of this paper.

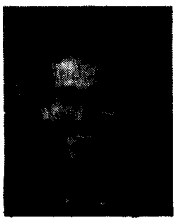
References

[1] J.C. Candy and G.C. Temes, "Oversampling methods for A/D and D/A conversion," *Oversampling Delta-Sigma Converters*, Eds. J.C. Candy and G.C. Temes, IEEE Press, 1991.
[2] H.T. Nicholas and H. Samueli, "A 150–MHz direct digital frequency synthesizer in 1.25μm CMOS with -90 dBc spurious performance," *IEEE J. of Sol.-State Circuits*, vol. 26, pp. 1959-1969, Dec. 1991.
[3] H.T. Nicholas, III, H. Samueli, and B. Kim, "The optimization of direct digital frequency synthesizer performance in the presence of finite word length effects," *Proc. 42nd Ann. Freq. Control Symp. USERACOM*, Ft. Monmouth, NJ, May 1988, pp. 357-363.
[4] P. O'Leary and F. Maloberti, "A Direct-Digital Synthesizer with Improved Spectral Performance," *IEEE Trans. Commun.*, vol. 39, no. 7, July 1991.
[5] M. Toner and G.W. Roberts, "A BIST scheme for an SNR test of a sigma-delta ADC", *IEEE Int. Test Conf.*, Baltimore, Maryland, Oct. 1993. pp. 805-814.
[6] L.T. Bruton, "Low sensitivity digital ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-22, pp. 168-176, Mar. 1975.
[7] L.E. Turner, "A fully programmable digital oscillator," CMC Workshop, Kingston, June 1992.
[8] L.E. Turner and B.K. Ramesh, "Low sensitivity digital LDI ladder filters with elliptic magnitude response," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 7, pp. 697-706, July 1986.
[9] B. Nowrouzian, N. R. Bartley, and L. Bruton, "Design and DSP-chip implementation of a novel bilinear-LDI digital jaumann filter," *IEEE Trans. Circuits Syst.*, vol. CAS-37, no. 6, pp. 695-706, June 1990.
[10] D.A. Johns and D.M. Lewis, "IIR filtering on delta-sigma modulated signals," *Electron. Lett.*, vol 27, pp. 307-308, Feb. 1991.
[11] Comdisco Systems, Inc., "SPW^{TM}, System, Installation and Tutorial, User's Guide," 2.7 revision, Aug. 1990.
[12] A/D Conversion IC's Data Book, vol. 1, Crystal Semiconductor Corp., Apr. 1992.



Albert K. Lu received the B.Eng. degree from McGill University, Montreal, Quebec, Canada in 1992 and since then has been pursuing a Master's degree, also at McGill.

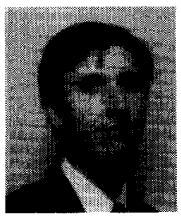
His research interests include delta-sigma modulated data converters, mixed-signal testing, and integrated circuits for telecommunications.



Gordon W. Roberts (S'84–M'89) received the B.A.Sc. degree from the University of Waterloo, Canada, in 1983 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, in 1986 and 1989, respectively, all in electrical engineering.

In 1983 he joined Northern Telecom Canada Ltd. as a Failure Analysis Engineer. In 1989 he joined the faculty at McGill University, Montreal, Quebec, Canada, where he is presently an Assistant Professor. He has co-authored an undergraduate textbook with Adel Sedra entitled *Spice for Microelectronic Circuits*, published by Saunders College Publishing and has contributed five chapters to various edited volumes related to analog IC design. He presently serves as a member of the board of directors for the IEEE Circuits and systems Society and is the present Director of the Microelectronics and Computer Systems Laboratory at McGill University. His area of research includes analog IC design and mixed-signal testing.

Dr. Roberts was the recipient of the Murata Erie North America Inc. Award in 1982 and the John H. Chapman Memorial Prize from Spar Aerospace in 1983. In 1989 he received an Outstanding Teaching Assistant Award from the University of Toronto. In 1993 he received the Overall Best Teacher Award from the Students of the Electrical Engineering Department and the Engineering Class of '51 Award for Outstanding Teaching from the Faculty of Engineering, both at McGill University.



David A. Johns (S'82–M'88) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Canada, in 1980, 1983, and 1989, respectively.

From 1980 to 1981 he worked ans an applications engineer in the semiconductor division of Mitel Corp., Ottawa, Canada. From 1983 to 1985 he was an analog IC designer at Pacific Microcircuits, Ltd., Vancouver, Canada. Upon completion of his doctoral work, he was hired at the University of Toronto where he is currently an assistant professor. His research interests are in the areas of analog CMOS and BICMOS circuit design, oversampling, and adaptive systems.

He is presently an associate editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING.