

HIGH-SPEED OVERSAMPLING ANALOG-TO-DIGITAL CONVERTERS

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This paper is mainly tutorial in nature and discusses architectures for oversampling converters with a particular emphasis on those which are well suited for high frequency input signal bandwidths. The first part of the paper looks at various architectures for discrete-time modulators and looks at their performance when attempting high speed operation. The second part of this paper presents some recent advancements in time-interleaved oversampling converters. The next section describes the design and challenges in continuous-time modulators. Finally, conclusions are made and a brief summary of the recent state of the art of high-speed converters is presented.

Keywords: oversampling, delta-sigma, analog-to-digital

1. Introduction

Data conversion is an important operation that finds applications in many circuits today. *Delta-sigma* ($\Delta\Sigma$) modulation is a relative simple and low cost means of performing data conversion. While $\Delta\Sigma$ modulators can obtain a high dynamic range and excellent linearity with the use of a 1-bit quantizer, they are most often found in low-frequency applications since they oversample the data to achieve a high *signal-to-noise ratio* (SNR), thus limiting the input bandwidth by the speed at which the sampler can operate.

The sampler in a $\Delta\Sigma$ modulator must operate at a speed much greater than the bandwidth of the input signal since it must oversample the data. When standard CMOS technology is used, the sampling frequency of the modulator is limited to a few hundred megahertz. This limits the bandwidth of the input signal to around ten megahertz, depending on the *oversampling ratio* (OSR). Some methods of overcoming this bandwidth limitation include a feedforward architecture, time-interleaving discrete-time $\Delta\Sigma$ modulators, or using continuous-time circuitry.

This paper is laid out as follows: Section 2 discusses discrete-time $\Delta\Sigma$ modulator topologies; Section 3 demonstrates various time-interleaved discrete-time $\Delta\Sigma$ modulator topologies; Section 4 explains some design issues for continuous-time $\Delta\Sigma$ modulators; and Section 5 presents recent publications on high-speed $\Delta\Sigma$ modulators and states the conclusions.

2. Single-Loop $\Delta\Sigma$ Modulator Topologies

This section provides a comparison of single-loop $\Delta\Sigma$ modulator topologies used for analog-to-digital converter applications that are suitable for high-speed implementation in deep sub-micron CMOS processes. To keep the scope of the analysis focused, the discussion is limited to $\Delta\Sigma$ modulators with pure differentiator type NTFs that employ internal quantizers with a sufficient number of levels to keep the modulator stable for any out-of-band gain. The relation of the topologies to their integrated-circuit implementation is emphasized.

The two main $\Delta\Sigma$ modulator topologies are the *chain of integrators with distributed feedback* (CIFB) and the *chain of integrators with weighted feedforward summation* (CIFF). To alleviate some of the drawbacks of the CIFB and CIFF topologies, the input-signal feedforward approach can be used as a modification. The resulting topologies, named *CIFB with input-signal feedforward* (CIFB-IF) and *CIFF with input-signal feedforward* (CIFF-IF), are discussed later. Note that, for the sake of simplicity, only modulators with all their zeros at dc will be discussed although these modulators can be modified with localized feedback to create non-dc zeros to optimize the NTF for a given OSR.

2.1. Chain of Integrators with Distributed Feedback

The simplest method to construct high order $\Delta\Sigma$ modulators is to cascade several integrators in the forward path, with each integrator receiving feedback from the quantizer to ensure stability. This CIFB topology is illustrated for a second-order modulator in Fig. 1.

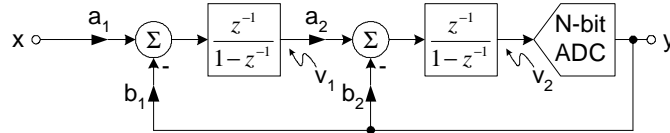


Fig. 1: Second-order CIFB modulator

Analysis of the linearized system with $a_1 = a_2 = b_1 = 1, b_2 = 2$ leads to the following results:

$$STF = \frac{y}{x} = z^{-2} \quad (1)$$

$$NTF = \frac{y}{q} = (1 - z^{-1})^2 \quad (2)$$

$$v_1 = z^{-1}(1 + z^{-1})x - z^{-1}(1 - z^{-1})q \quad (3)$$

$$v_2 = z^{-2}x - z^{-1}(2 - z^{-1})q \quad (4)$$

where q is the quantization noise from the ADC, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively. The STF exhibits an all-pass response and the NTF provides a second-order pure differentiator type high-pass response.

The main advantages of the CIFB topology are that it is easy to implement with low sensitivity to component variations. The main disadvantage of this topology is that the signals at the output of the integrators are a function of the input-signal as given in Eqs. (3) and (4) above, resulting in two effects. First, the signal swing at the output of the opamps is large which makes their implementation in the low-voltage, deep sub-micron technology more difficult. Second, opamp nonlinearities generate harmonic distortion that depends on the input-signal. The opamp distortion can severely limit the achievable SQNR. Another disadvantage of the CIFB topology is that the NTF and STF cannot be set independently. Therefore, if we pick a certain NTF, then the STF is fixed.

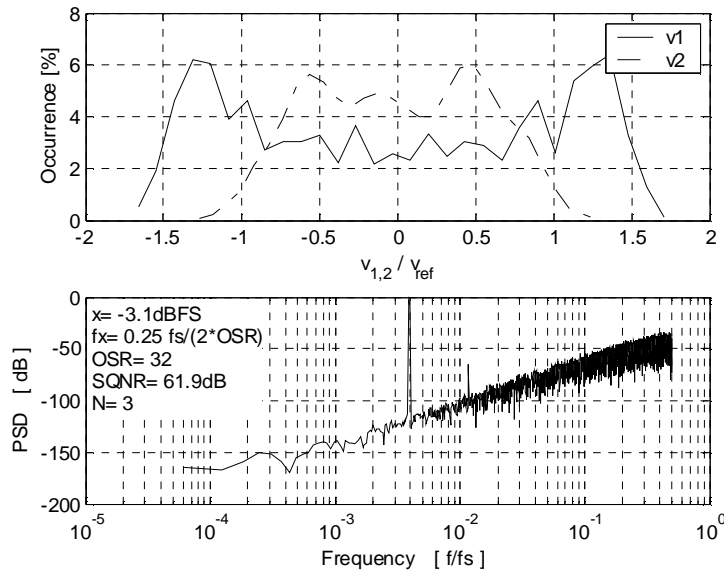


Fig. 2: Signal swing at Opamp outputs and sample output spectrum for CIFB

The CIFB topology is simulated using MATLAB[®] and Simulink[®]. The probability density function of integrator outputs and a sample output spectrum including opamp third-order distortion are shown in Fig. 2. The third-order distortion model is in the form of a power series with the third-order term corresponding to 1% third-order harmonic distortion for full scale signal. Simulations indicate the signal swings can be more than 1.5 times larger than the ADC reference voltage. On the other hand, the input-signal range is from 50 to 80% of the ADC reference voltage and depends on the loop order and number of bits in the quantizer.¹ Therefore, the input-signal is going to be relatively small when compared to other topologies, and to meet thermal noise requirements the capacitor

sizes must be larger, leading to greater power dissipation. The third harmonic generated by the opamp nonlinearity is clear in the output spectrum shown in Fig. 2. Distortion severely reduces the SQNR of the CIFB topology from the ideal 76dB to 62dB for the example shown in Fig. 2.

The CIFB is the most commonly used topology to implement $\Delta\Sigma$ modulators. An example of the CIFB topology is implemented as a third-order CIFB $\Delta\Sigma$ modulator using a 4-bit internal quantizer and operating with a sampling frequency of 100MHz.² The modulator achieves an SNDR of 67dB and a peak SNR of 68dB with a 12.5MS/s conversion rate. The modulator is implemented in 0.65 μ m technology and powered with 5V supply while consuming 380mW.

2.2. Chain of Integrators with Weighted Feedforward Summation

Distributed feedback was used to ensure stability of the cascade of integrators in the forward path. Alternatively, weighted feedforward paths can be used to establish stability. The resulting chain of integrators with the CIFF topology for a second-order modulator is shown in Fig. 3.

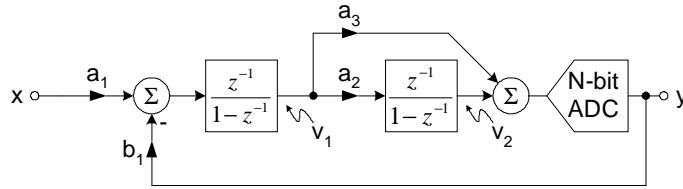


Fig. 3: Second-order CIFF modulator

Analysis of the linearized system with $a_1 = a_2 = b_1 = 1, a_3 = 2$ leads to the following results:

$$STF = \frac{y}{x} = z^{-1}(2 - z^{-1}) \quad (5)$$

$$NTF = \frac{y}{q} = (1 - z^{-1})^2 \quad (6)$$

$$v_1 = z^{-1}(1 - z^{-1})x - z^{-1}(1 - z^{-1})q \quad (7)$$

$$v_2 = z^{-2}x - z^{-2}q \quad (8)$$

where q is the quantization noise from the ADC, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively.

The CIFF improves the performance of CIFB in terms of the signals at the output of the integrators. As can be seen from Eq. (7), the signal at the output of the first opamp contains a first-order noise shaped input-signal component in addition to shaped quantization noise. This reduces signal swing and reduces dependence of the distortion on the input-signal. Both of these benefits are illustrated in Fig. 4. The signal swing at the output of the first opamp is significantly reduced and the output spectrum does not show

harmonic distortion. The second opamp still contains an input-signal component, however, nonlinearities at this stage are not as important since they are second-order noise shaped when referred back to the input.

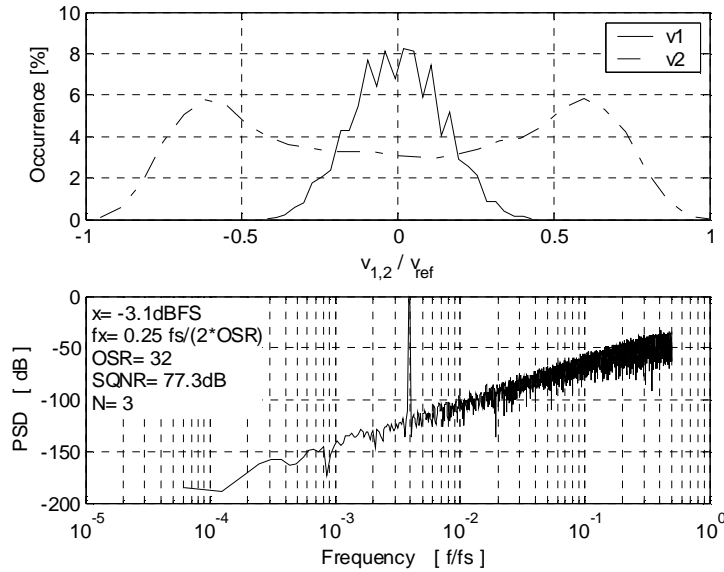


Fig. 4: Signal swing at Opamp outputs and sample output spectrum for CIFF

The main disadvantage of the CIFF topology can be seen by investigating its STF given in Eq. (5). The STF has a high frequency boost with a gain of one at low frequencies and three at high frequencies. The amplification of the out-of-band frequencies due to the high frequency boost can overload the quantizer and drive the modulator into instability. Unfortunately, the NTF and STF are not independent; therefore, the high frequency boost in STF is fixed by the choice of the NTF.

One of the fastest CMOS $\Delta\Sigma$ modulators reported in literature is implemented using the CIFF topology where a fifth-order CIFF $\Delta\Sigma$ modulator uses a 4-bit internal quantizer and operates at a 200MHz sampling frequency.³ The modulator achieves an SNDR of 72dB with a peak SNR of 82dB at a conversion rate of 25MS/s. This performance is achieved in 0.18 μm CMOS technology.

2.3. CIFB with Input-Signal Feedforward

The input-signal component at opamp outputs in the CIFB topology can be eliminated by feeding the input-signal forward such that the input-signal components cancel out. The resulting CIFB-IF topology is illustrated for a second-order modulator in Fig. 5.

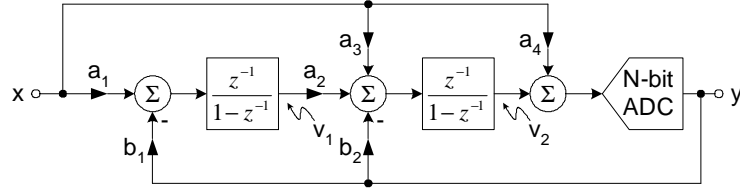


Fig. 5: Second-order CIFB-IF modulator

Analysis of the linearized system with $a_1 = a_2 = a_4 = b_1 = 1$, $a_3 = b_2 = 2$ leads to the following results:

$$STF = \frac{y}{x} = 1 \quad (9)$$

$$NTF = \frac{y}{q} = (1 - z^{-1})^2 \quad (10)$$

$$v_1 = -z^{-1}(1 - z^{-1})q \quad (11)$$

$$v_2 = -z^{-1}(2 - z^{-1})q \quad (12)$$

where q is the quantization noise from the ADC, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively.

The input-signal feedforward modifies v_1 , v_2 , and the STF without affecting the NTF. The signals v_1 and v_2 are free of the input-signal component. Therefore, the signal swings are smaller and the distortion generated by the opamps is input-signal independent. These advantages are illustrated in Fig. 6.

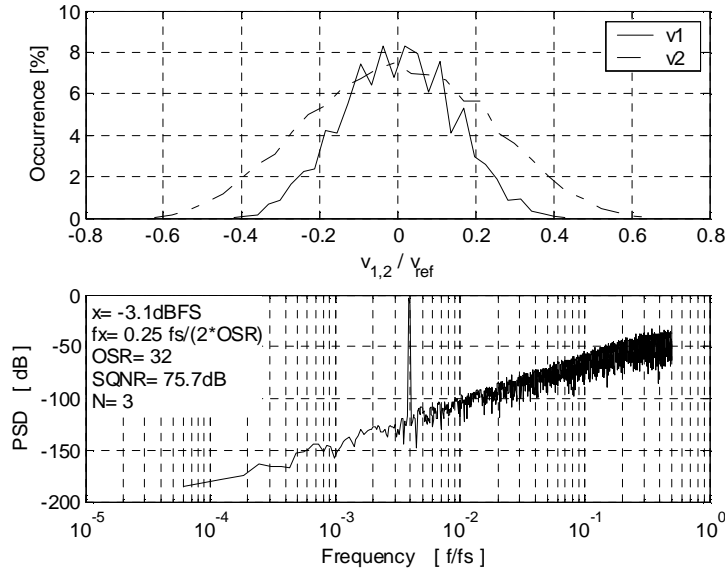


Fig. 6: Signal swing at Opamp outputs and sample output spectrum for CIFB-IF

The disadvantage of the CIFB-IF topology is the increased loading that the input has to drive, which can be particularly large for higher order modulators. This is because of the distributed feedforward paths that are needed to achieve the input-signal cancellation. In the second-order case, for example, there is the main sampling capacitor at the input as well as two extra sampling capacitors to feed the input-signal forward. It should be mentioned that the extra capacitors are usually smaller than the input sampling capacitor because the thermal noise on these capacitors is noise shaped and therefore, their size can be smaller.

An example of the CIFB-IF topology is implemented as a second-order modulator using a single-bit internal quantizer and operating with a sampling frequency of 105MHz.⁴ The modulator achieves a dynamic range of 88dB with a peak SNR of 82dB. The modulator is implemented in 0.13 μ m CMOS technology and powered with a 1.5V supply while consuming only 8mW of power.

2.4. CIFF with Input-Signal Feedforward

The main problem with the CIFF topology is the high frequency boost in the STF. The input-signal feedforward concept can be used to modify the STF of the CIFF topology without affecting the NTF. The CIFF-IF topology is illustrated in Fig. 7 for a second-order modulator.⁵

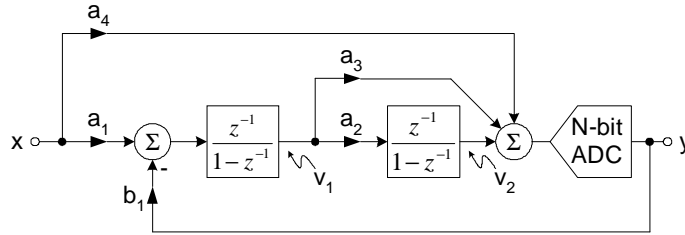


Fig. 7: Second-order CIFF-IF modulator

Analysis of the linearized system with $a_1 = a_2 = a_4 = b_1 = 1, a_3 = 2$ leads to the following results:

$$STF = \frac{y}{x} = 1 \quad (13)$$

$$NTF = \frac{y}{q} = (1 - z^{-1})^2 \quad (14)$$

$$v_1 = -z^{-1}(1 - z^{-1})q \quad (15)$$

$$v_2 = -z^{-2}q \quad (16)$$

where q is the quantization noise from the ADC, and v_1 and v_2 are the signals at the outputs of the first and second integrators respectively.

The input-signal feedforward changes the problematic high frequency boost in the STF of the CIFF topology to an all-pass STF in the CIFF-IF topology with no effect on

the NTF. It is interesting to note that this modulator achieves the smallest signal swings at the output of the opamps among the topologies discussed, as seen in Fig. 8.

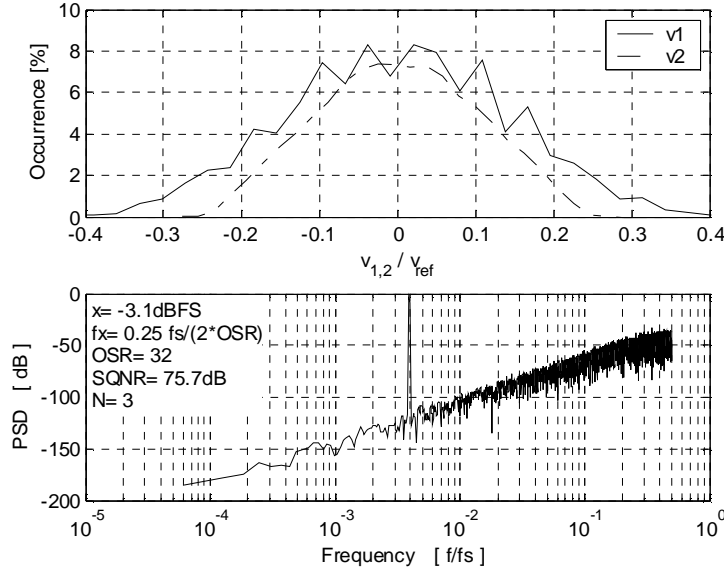


Fig. 8: Signal swing at Opamp outputs and sample output spectrum for CIFF-IF

3. Time-Interleaved $\Delta\Sigma$ Modulators

This section presents time-interleaved $\Delta\Sigma$ modulator topologies based on block filtering theory. The usual system level design parameters for $\Delta\Sigma$ modulators are the loop-order, OSR, and the number of bits in the internal quantizer. High-speed applications require low OSRs, thereby, limiting the choices available for the designer. One method to add another degrees of freedom is to use parallel $\Delta\Sigma$ structures. The simplest method of making parallel converters is through the use of *time-interleaving* (TI) which is simply a time-division multiplexing scheme where an array of individual converters are clocked at different instants in time. Unfortunately, exploiting simple time-interleaved parallelism is not a straightforward process for $\Delta\Sigma$ modulators due to their recursive nature. Straightforward TI adaptation to $\Delta\Sigma$ modulators results in a 3dB improvement in the SNR for each doubling of converters regardless of the order of the modulator. To overcome this problem, different schemes of parallel modulators have been devised. They can be classified in one of three main categories: *frequency division multiplexing* (FDM),⁶ *code division multiplexing* (CDM),⁷ and *time division multiplexing* (TDM).⁸

TDM can be implemented by deploying the theory of block digital filtering. The principle of block digital filtering is based on transforming a linear time-invariant (LTI) single-input single-output system (SISO) with transfer function $H(z)$ to an equivalent multi-input multi-output system with transfer function $\bar{H}(z)$, as shown in Fig. 9.

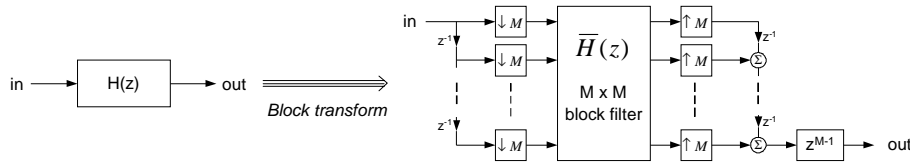


Fig. 9: $H(z)$ and its blocked version with block length M

The internal circuitry of the block filter operates in parallel and at a reduced rate by the factor M . For example, using this transformation for a $\Delta\Sigma$ modulator with $M=2$ allows the internal modulators to either operate at half-speed for the same resolution, or at enhanced resolution for the same speed. This improvement is significant in wide bandwidth applications where the sampling speed is limited by the technology and resolution requirements.

The block digital filtering has facilitated the design and construction of a true TI $\Delta\Sigma$ modulator.⁸ A second-order, time-interleaved by 2 ($M=2$), CIFB $\Delta\Sigma$ modulator is shown in Fig. 10 as an example of the technique.⁸

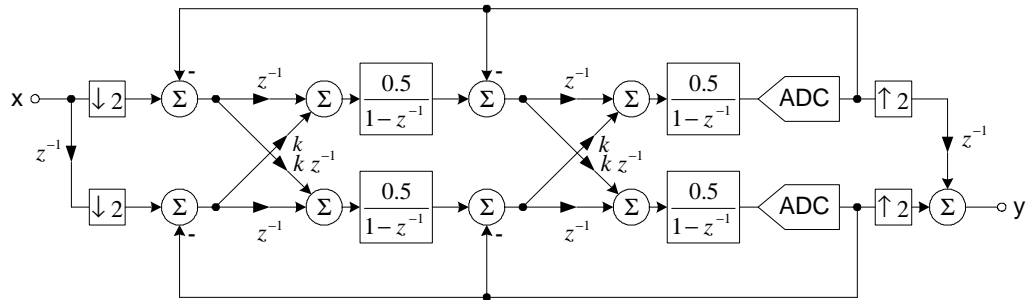


Fig. 10: Second-order time-interleaved by 2 CIFB $\Delta\Sigma$ modulator

The k -factor shown in Fig. 10 is used to deal with the issue of opamp DC offsets.⁸ DC offsets are problematic in time-interleaved modulators because the difference in offset between the two branches drives the modulator to instability. Reducing the cross-coupling coefficients gives more control to each parallel $\Delta\Sigma$ modulator, thus enabling the negative feedback loop to adjust; which maintains DC stability. However, reducing k from unity modifies the STF and results in an increase of the quantization noise in the signal band, thereby reducing the SQNR. The choice of k is a tradeoff between the offset value that the modulator can tolerate and the achievable SNR. A time-interleaved modulator that does not suffer from DC offsets is presented below.

A high-speed input demux is needed at the input of the modulator to sample the input-signal and distribute it to the individual internal modulators. The demux operates at the full speed of the overall modulator. For example, the demux in a time-interleaved by 4 modulator operates at four times the speed of the individual $\Delta\Sigma$ modulators. The high-speed demux can become the limiting factor in the performance of the modulator

especially for higher-order TI structures ($M > 2$). A solution for the demux problem for $M=2$ is to sample each branch in the time-interleaved modulator at a different phase of the two non-overlapping phases.⁸ Therefore, the demux is inherent in the operation of the modulator. Another more general solution that can be used for any M is called the zero-insertion interpolation technique,⁹ which is shown in Fig. 11 for $M=2$ second-order CIFB topology. The *zero-insertion time-interleaved* (ZI-TI) modulator samples the input-signal at the operating frequency of the individual $\Delta\Sigma$ modulator and applies these samples to the first branch only with the inputs to the others grounded.

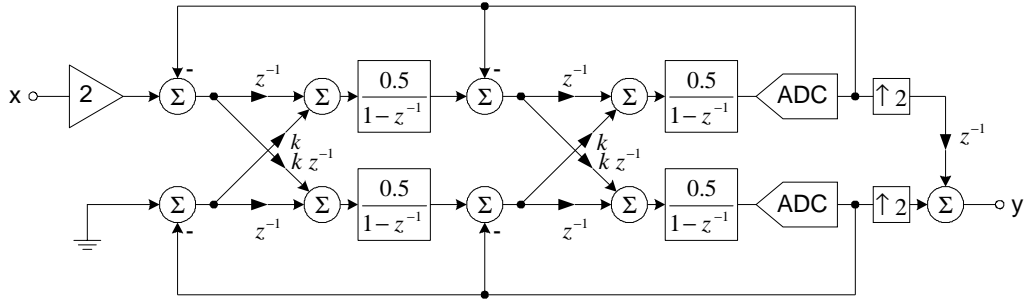
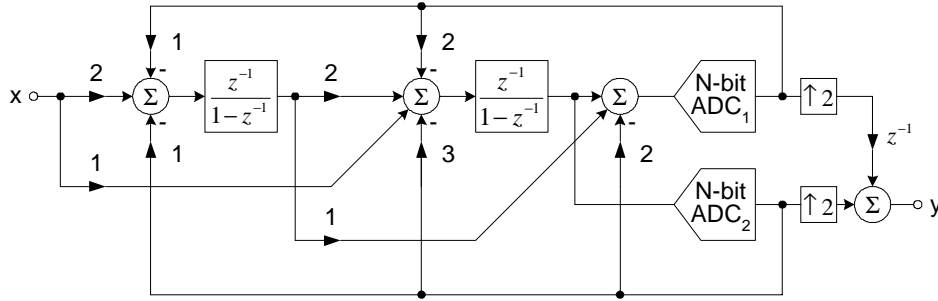


Fig. 11: Second-order ZI-TI with $M=2$ CIFB $\Delta\Sigma$ modulator

The sampled input must be amplified (by M) to compensate for the lost signal power resulting from supplying zero input instead of the input-signal to the other branches. The ZI-TI modulator still suffers from DC offsets and therefore the cross-coupling coefficient k must be set appropriately.

A new *modified time-interleaved* (MTI) $\Delta\Sigma$ modulator that eliminates the input demux and alleviates the DC offset problem is shown in Fig. 12. The modulator can be derived starting from the TI (Fig. 10) by removing the demux and applying the input-signal to both branches simultaneously. The resulting second-order MTI CIFB $\Delta\Sigma$ modulator, after some modifications, is shown in Fig. 12. The MTI uses two integrators only instead of the four used in TI, and in general, it uses the same number of integrators as the basic $\Delta\Sigma$ modulator for a given loop order. Therefore, there is no DC offset difference between the two branches that would otherwise lead to instability. In summary, the MTI eliminates the high-speed analog demux, alleviates the DC offset problems, and uses fewer integrators.


 Fig. 12: Second-order modified time-interleaved by 2 CIFB $\Delta\Sigma$ modulator

Removing the demux at the input has some consequences. Analysis of the linearized system of Fig. 12 leads to the following results:

$$y = z^{-2}(1+z^{-1})x + z^{-1}(1-z^{-1})^2 q_1 + (1-z^{-1})^2 q_2 \quad (17)$$

where q_1 and q_2 are the quantization noise from ADC_1 and ADC_2 respectively. Due to the output mux, the quantization noise q_1 is only added to the output once for every two samples, which is also true for q_2 . Therefore, the overall noise contribution can be rewritten as:

$$NTF = \frac{y}{q} = (1-z^{-1})^2 \quad (18)$$

which is simply second-order noise shaped. Clearly, the removal of the demux does not affect the TI NTF, however the STF is affected. The first term in the STF is z^{-2} , which is the expected STF of a second-order CIFB modulator. The second term, $(1+z^{-1})$, resulted from the removal of the input demux. The extra term adds a notch at half the sampling frequency and filters the amplitude response of the STF as shown in Fig. 13. Due to oversampling, the frequency variation is not significant within the signal band. Also, it can be easily compensated for in the digital domain.

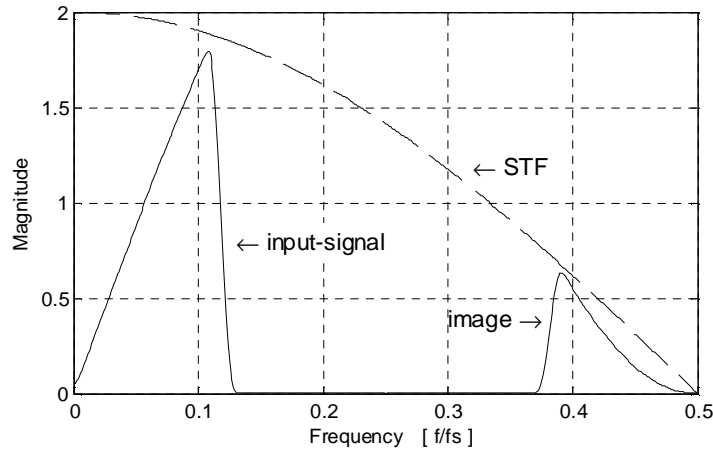


Fig. 13: STF and imaging issue for MTI

Another effect of removing the demux is that the signal is under the influence of the upsamplers only. The effect of upsampling by M is M -fold compression and repetition of the frequency-domain magnitude response.¹⁰ The process generates images shaped by the STF at frequencies less than half the sampling frequency as shown in Fig. 13 for a sample input spectrum. The design of the anti-aliasing and decimation filters should take the imaging issue into account.

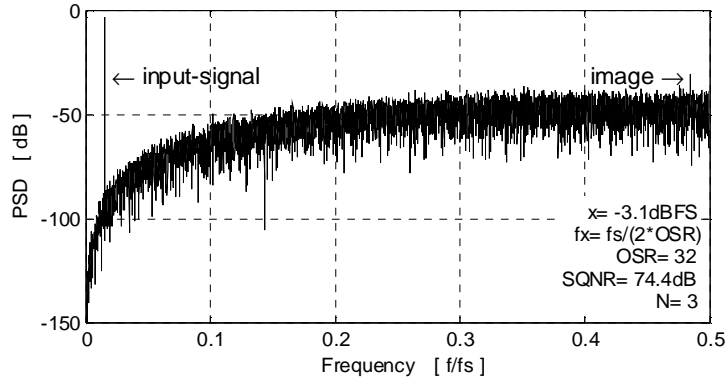


Fig. 14: Sample output spectrum for MTI

A sample output spectrum for the MTI is shown in Fig. 14. It also highlights the shaped image of the input-signal. For this example, the integrators are clocked at half the rate as the single-loop topologies presented earlier. The MTI modulator achieved a slightly lower SQNR because the STF attenuates the input-signal which reduces the input power.

4. Continuous-Time $\Delta\Sigma$ Modulators

Employing continuous-time loop filters instead of discrete-time loop filters is one way to increase the input signal bandwidth. The main advantage of continuous-time filters is that no sampling is performed within the filters, so the restriction of the maximum sampling frequency is only imposed on the quantizer, as well as on the feedback DAC. Practically, continuous-time modulators can operate with clock frequencies about 2-4 times greater than regular discrete-time modulators, while suffering from reduced linearity and accuracy.¹¹ Also, continuous-time modulators eliminate the need for an anti-aliasing filter on the input since it is inherent in the signal transfer function (STF).

There do exist some disadvantages of continuous-time $\Delta\Sigma$ modulators when compared to discrete-time modulators. High-speed continuous-time modulators suffer more severely from two non-idealities, namely excess loop delay and DAC clock jitter. The following section will explain some of the more important design considerations, including a brief description on how to design a continuous-time $\Delta\Sigma$ modulator from a

discrete-time $\Delta\Sigma$ modulator while avoiding excessive STF peaking, and some methods of reducing excess loop delay and DAC clock jitter.

4.1. Discrete-to-Continuous Transform

To design a continuous-time $\Delta\Sigma$ modulator, a discrete-time $\Delta\Sigma$ modulator may be designed and simulated, and then a conversion between the two modulators can be performed to realize the desired loop filters of the continuous-time $\Delta\Sigma$ modulator. One method of finding equivalence between a continuous-time and discrete-time modulator is to recognize that an implicit sampling occurs in the quantizer of the continuous-time modulator.¹² If the open-loop modulators are analyzed, as shown in Fig. 15, the two modulators are equivalent as long as the outputs are equal at the sampling instants. Therefore, if $w[n] = w(t)|_{t=nT}$ for all n , then the loop filters will be equivalent. The resulting condition for the two filters $B(z)$ and $B(s)$ to be equivalent is:¹³

$$Z^{-1}\{B(z)\} = L^{-1}\{R(s) \cdot B(s)\}|_{t=nT} \quad (19)$$

This transformation is known as the impulse-invariant transformation,¹⁴ where Z^{-1} represents the inverse z-transform, L^{-1} represents the inverse Laplace transform, and $R(s)$ represents the DAC pulse.

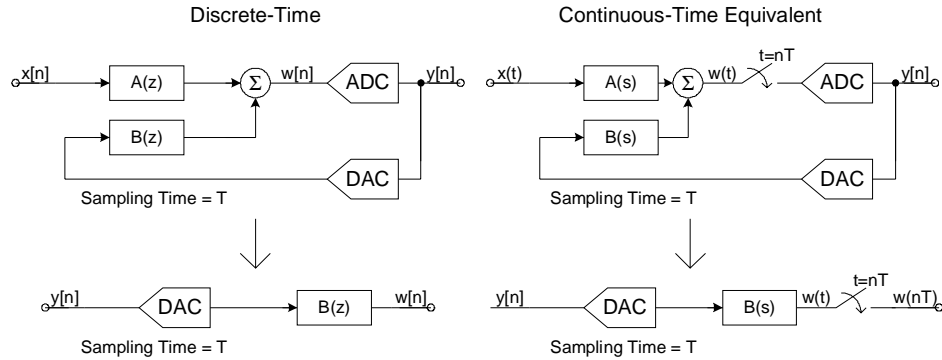


Fig. 15: Open loop continuous-time equivalent of discrete-time modulator

To properly account for the shape of the DAC pulse, Eq. (19) is rewritten with the DAC pulse $R(s)$ represented by:¹²

$$R(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{sT} \quad (20)$$

The time domain representation of this DAC pulse transfer function $R(s)$ is:

$$r(t) = \begin{cases} 1, & \alpha \leq t < \beta, \quad 0 \leq \alpha < \beta \leq T \\ 0, & \text{otherwise} \end{cases} \quad (21)$$

Eqs. (20) and (21) assume that the pulse is rectangular and has a magnitude of one, lasting from $t = \alpha$ to $t = \beta$.

As an example, if a discrete-time $\Delta\Sigma$ modulator were designed with an NTF of $H(z) = (1 - z^{-1})^2$ (with an STF $G(z) = z^{-1}$), then the continuous-time $\Delta\Sigma$ modulator would be designed as follows:

1) Referring to Fig. 15, $A(z)$ and $B(z)$ are found as follows from the given NTF and STF:

$$B(z) = \frac{-2z^{-1} + z^{-2}}{1 - 2z^{-1} + z^{-2}} = \frac{-2z + 1}{z^2 - 2z + 1} \quad (22)$$

$$A(z) = \frac{z^{-1}}{1 - 2z^{-1} + z^{-2}} = \frac{z}{z^2 - 2z + 1} \quad (23)$$

2) The filters $A(z)$ and $B(z)$ are dissected into their partial fraction representation:

$$B(z) = \frac{-1}{z^2 - 2z + 1} + \frac{-2}{z - 1} \quad (24)$$

$$A(z) = \frac{1}{z^2 - 2z + 1} + \frac{1}{z - 1} \quad (25)$$

3) Using Eqs. (24) and (25) for $A(z)$ and $B(z)$ (where $R(s)$ would have $\alpha = 0$ and $\beta = T$), the resulting equivalent continuous-time filters are (using the transforms $\frac{1}{z-1} \rightarrow \frac{1}{Ts}$, $\frac{1}{(1-z)^2} \rightarrow \frac{-Ts+2}{2T^2s^2}$):

$$B(s) = \frac{Ts-2}{2T^2s^2} + \frac{-2}{Ts} = \frac{-3Ts-2}{2T^2s^2} \quad (26)$$

$$A(s) = \frac{-Ts+2}{2T^2s^2} + \frac{1}{Ts} = \frac{Ts+2}{2T^2s^2} \quad (27)$$

4) These loop filters $A(s)$ and $B(s)$ can be converted into a $\Delta\Sigma$ modulator topology. An example of one possible modulator is shown in Fig. 16.

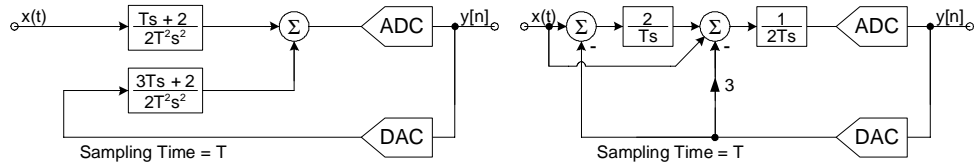


Fig. 16: Continuous-time modulator to realize derived loop filters

4.2. Signal Transfer Function

In the example above, $A(z)$ was designed to be $\frac{z}{z^2 - 2z + 1}$. An extra delay in this path does not change the discrete-time transfer function, but it can alter the continuous-time transfer function when the discrete-to-continuous transform is applied. The result is that there can be potentially more or less peaking in the STF. This can be hazardous since it can cause instability in the modulator for certain input frequencies. Therefore, the STF should be computed and analyzed to ensure minimal peaking.

Assuming a linearized model of the $\Delta\Sigma$ modulator where the quantizer is replaced by a unity-gain block, the STF can be computed as the input loop filter $A(s)$ multiplied by

the discrete-time NTF. The NTF is discrete-time due to the sampling in the quantizer. To make them both a function of the same frequency, the discrete-time transfer function is evaluated at $z = e^{j2\pi fT}$ while the continuous-time transfer function is evaluated at $s = j2\pi fT$.¹¹ When the resulting transfer function is plotted, the inherent anti-aliasing property of the continuous-time STF is apparent.

Using an $A(z)$ of higher order to illustrate the change in the STF, the functions $\frac{1}{z^3 - 3z^2 + 3z - 1}$, $\frac{z}{z^3 - 3z^2 + 3z - 1}$ and $\frac{z^2}{z^3 - 3z^2 + 3z - 1}$ can all be converted to their equivalent continuous-time input loop filters $A(s)$. These discrete-time filters $A(z)$ all result in the same transfer functions, except for a difference in the latency at the output. But when the equivalent $A(s)$ for all three cases is multiplied by the NTF $H(z) = (1 - z^{-1})^3$ (evaluated at $z = e^{j2\pi fT}$), the resulting continuous-time STFs are shown in Fig. 17. Only two graphs are plotted since the continuous-time STFs are the same when $A(z)$ equals either $\frac{1}{z^3 - 3z^2 + 3z - 1}$ or $\frac{z^2}{z^3 - 3z^2 + 3z - 1}$. But in both these cases, the STF peaks 1.4dB higher than when $A(z) = \frac{z}{z^3 - 3z^2 + 3z - 1}$, resulting in a potentially less stable $\Delta\Sigma$ modulator due to this unwanted gain.

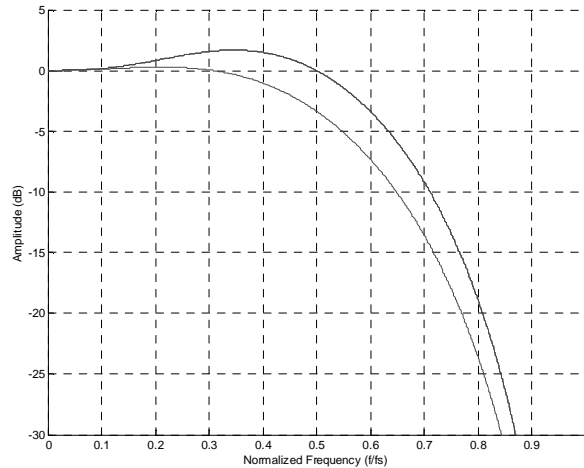


Fig. 17: Comparison of continuous-time STF for various discrete-time input transfer functions

4.3. Excess Loop Delay

One of the major difficulties with continuous-time $\Delta\Sigma$ modulators is that a small delay t_d exists between the quantizer sampling instant and when the DAC pulse is valid because the transistors cannot switch instantaneously. This is known as excess loop delay.¹² The excess loop delay in a continuous-time modulator effectively increases the order of the

modulator if the pulse enters the next clock period, as demonstrated in Fig. 18. When the pulse enters the adjacent clock period, the resulting order of the equivalent discrete-time transfer function increases.¹² This increase in order can be illustrated by modeling the output of the DAC pulse with excess loop delay t_d as the sum of two pulses as follows:

$$DAC_{(td, T+td)}(t) = DAC_{(td, T)}(t) + DAC_{(0, td)}(t - T) \quad (28)$$

where $DAC_{(td, 1)}(t)$ represents a pulse from $\alpha = t_d$ to $\beta = T$, and $DAC_{(0, td)}(t - T)$ represents a pulse from $\alpha = 0$ to $\beta = t_d$ that has been shifted in time by the sampling period T . The resulting z-transform will be the sum of two pulses, one of which has an extra z^{-1} term due to the delayed DAC pulse $DAC_{(0, td)}(t - T)$, and this will contribute to the increased order of the transfer function. Using this analysis, the transfer function:¹²

$$H(z) = \frac{-2z + 1}{(z - 1)^2} \quad (29)$$

becomes

$$H(z) = \frac{(-2 + 2.5t_d - 0.5t_d^2)z^2 + (1 - 4t_d + t_d^2)z + (1.5t_d - 0.5t_d^2)}{z(z - 1)^2} \quad (30)$$

where the extra order is evident. This reduces the stability of the $\Delta\Sigma$ modulator, and is more significant at larger values of the excess loop delay t_d . Also, the excess loop delay increases the noise floor of the $\Delta\Sigma$ modulator. This analysis facilitates simulation of the equivalent discrete-time modulator to fully evaluate the acceptable excess loop delay in a given $\Delta\Sigma$ modulator design.

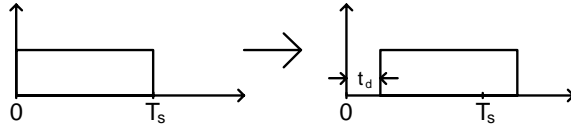


Fig. 18: Excess loop delay in a full period DAC pulse

The use of an additional feedback term directly into the quantizer from the DAC in the continuous-time $\Delta\Sigma$ modulator has been shown to mitigate the effects of excess loop delay.^{15, 16} In fact, it was shown that in some cases a delay greater than T can be used, as long as the delay is properly chosen.¹⁵ This technique is shown in Fig. 19 with the extra f path.

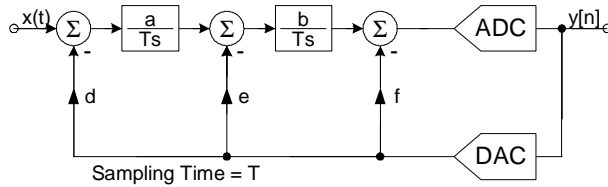


Fig. 19: Additional path to reduce effects of excess loop delay

Another simple way of reducing the effects of excess loop delay is to use *return-to-zero* (RZ) DAC pulses. Under this condition, the width of the pulse in Fig. 18 can be adjusted so that it does not extend beyond the sampling interval T . The value of the continuous-time filters must then be adjusted accordingly since the α and β parameters of Eqs. (20) and (21) will be modified. One difficulty with this solution is that the loop filters of the $\Delta\Sigma$ modulator will have been designed specifically for a given α and β , and changes in the value t_d will alter the rise and fall instants of the feedback pulse. Therefore, these rise and fall instants should be very well controlled with respect to the quantizer clock, especially at high speeds. It is also possible to introduce a variable delay block between the quantizer clock and the RZ DAC pulse clock so that this delay value can be manually or automatically tuned for increased precision.

4.4. Clock Jitter

Clock jitter is statistical variations of clock edges.¹⁷ Two clocks are present in a CT $\Delta\Sigma$ modulator and both can be affected by clock jitter. One of the clocks controls the decision instant of the quantizer (or comparator) while the other clock controls the DAC output. Since the output of the comparator is shaped by the NTF (like the quantization noise), the impact of this error will be relatively small. Conversely, the output of the DAC is shaped by the STF because this signal adds to the input signal and thus, the impact of this error affects the passband noise in the $\Delta\Sigma$ modulator.¹⁸

There are two varieties of clock jitter, delay clock jitter and pulse-width clock jitter. In a second-order $\Delta\Sigma$ modulator, the delay clock jitter is affected by the NTF while the pulse-width clock jitter manifests itself as white noise.¹⁹ Thus, the pulse-width clock jitter degrades the SNR of the $\Delta\Sigma$ modulator more severely since the white noise fills in the notch in the signal band, directly reducing the noise floor in the band of interest. Therefore, the clock jitter discussed will be the pulse-width clock jitter incurred in the DAC.

Discrete-time $\Delta\Sigma$ modulators are relatively insensitive to pulse-width clock jitter since they utilize switched-capacitor circuits. The insensitivity is due to the sloping form of the feedback pulse.¹⁷ Because most of the charge transfer in a switched-capacitor circuit occurs at the beginning of the clock period, clock jitter introduces a minimal amount of error in the charge lost ΔQ_d (see Fig. 20).²⁰ The capacitor is discharged over a switch with very low on-resistance, thus reducing the value of $\tau = RC$ and causing a fairly steep slope as the DAC discharges.²⁰ In contrast, continuous-time $\Delta\Sigma$ modulators transfer charge at a constant rate over the clock period (ideally), and thus, the charge loss ΔQ_c , due to a timing error, is proportionally much greater than that of the discrete-time $\Delta\Sigma$ modulator.

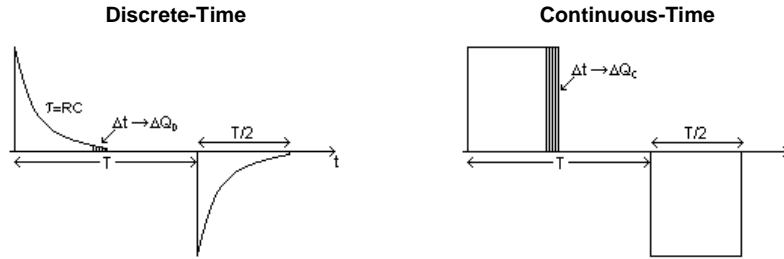


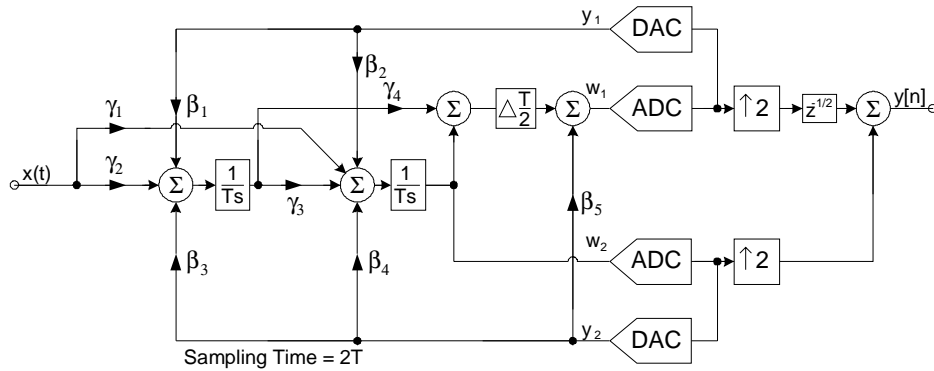
Fig. 20: Clock jitter in discrete-time and continuous-time modulators

The clock jitter with RZ DAC pulses is going to be more detrimental than that for the *non-return-to-zero* (NRZ) DAC pulses for a couple of reasons. First, with RZ DAC pulses, since the width of the pulse is smaller, this proportionally results in a larger percentage difference of the total integrated signal when jitter is introduced, when compared to a full period NRZ DAC pulse. Second, in every clock period, the RZ DAC pulse returns to zero, independent of the previous value, and thus introduces clock jitter in every pulse. Conversely, in the NRZ DAC pulse, adjacent pulses may have the same value, thus introducing no clock jitter in that period. And finally, similar to the last point, in a multi-bit $\Delta\Sigma$ modulator the output of adjacent DAC pulses typically do not span the entire range of the feedback DAC, and are typically a few levels apart. Therefore, the clock jitter will be present in a smaller fraction of the total pulse area. However, when a RZ DAC pulse is used, the output pulse must return to zero during every period, and thus, the change in level is greater than that of an NRZ pulse. On average, this increases the presence of clock jitter when using an RZ pulse as compared to an NRZ pulse in a multibit feedback DAC.

The effects of clock jitter for two low-pass $\Delta\Sigma$ modulators with single-bit quantizers were analyzed, where one used RZ DAC pulses, and the other used NRZ DAC pulses.²⁰ It was found that the noise power in the case with RZ DAC pulses was about 3 times worse than that with NRZ DAC pulses.

4.5. Time-Interleaving

Continuous-time $\Delta\Sigma$ modulators can also be time-interleaved. As an example, the second-order discrete-time modulator shown in Fig. 11 can be converted to its time-interleaved by 2 continuous-time equivalent with various manipulations of the loop filters (since there are now clearly more than just $A(z)$ and $B(z)$ as the loop filters). The resulting modulator is shown in Fig. 21 where the ADCs and DACs are operating at half of the original frequency, meaning that clock jitter has about half the impact on the $\Delta\Sigma$ modulator. Furthermore, the higher bandwidth requirements on an RZ DAC operating at high-speeds (assuming the choice of an RZ DAC pulse to reduce the excess loop delay) is reduced by a factor of two by time-interleaving.


 Fig. 21: Time-interleaved continuous-time $\Delta\Sigma$ modulator

5. Conclusions

This paper discussed a variety of techniques for designing high-speed oversampling analog-to-digital converters including an input feedforward architecture, time-interleaving and continuous-time modulators. Some design challenges were highlighted and potential solutions described. Some recent publications of higher-speed CMOS $\Delta\Sigma$ modulators are shown in Table 1 and give an indication of the present state-of-the-art for input signal bandwidths greater than 5MHz. While continuous-time modulators tend to dominate at higher input signal bandwidths, we see from Table 1 that excellent results can still be obtained using a discrete-time modulator through careful architecture and circuit design.³

 Table 1: Recently published high-speed $\Delta\Sigma$ modulators

| Ref. | Technology | Sampling Frequency | SNDR | Power | Bandwidth | Topology |
|------|-------------------------|--------------------|-------|--------|-----------|-----------|
| 2 | 0.65 μm CMOS | 100 MHz | 67 dB | 295 mW | 6.25 MHz | DT (CIFB) |
| 21 | 0.13 μm CMOS | 80 MHz | 50 dB | 80 mW | 10 MHz | CT |
| 22 | 0.13 μm CMOS | 160 MHz | 57 dB | 122 mW | 10 MHz | CT |
| 3 | 0.18 μm CMOS | 200 MHz | 72 dB | 200 mW | 12.5 MHz | DT (CIFI) |
| 23 | 0.13 μm CMOS | 300 MHz | 64 dB | 70 mW | 15 MHz | CT |
| 21 | 0.13 μm CMOS | 160 MHz | 50 dB | 120 mW | 20 MHz | CT |

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