Combining Multipath and Single-Path Time-Interleaved Delta-Sigma Modulators

Ahmed Gharbiya and David A. Johns

***Abstract*—In this brief, single-path time-interleaved delta-sigma modulators are analyzed and evaluated. It is found that finite opamp gain and bandwidth result in a mismatch between the noise transfer functions of the internal quantizers which degrades the performance of the architecture. A hybrid topology where the first stage uses multiple integrators while the rest of the modulator uses a single path of integrators is proposed to mitigate the mismatch problem.**

***Index Terms*—Analog-to-digital converter (ADC), delta-sigma, oversampling, time-interleaved.**

I. Introduction

DELTA-SIGMA ($\Delta\Sigma$) modulators are widely used for high-resolution and low-bandwidth analog-to-digital converters (ADCs). Time-interleaving, where arrays of individual converters are clocked at different instants in time, can be exploited to increase the speed of $\Delta\Sigma$ modulators. Unfortunately, implementing simple time-interleaved parallelism is not a straightforward process for $\Delta\Sigma$ converters due to their recursive nature. To overcome this problem, the block filtering concept can be used to implement time-interleaved $\Delta\Sigma$ modulators [1]. The internal circuitry of the block filter operates in parallel and at a reduced rate by the interleaving factor J. For example, using this transformation for a $\Delta\Sigma$ modulator with $\mathrm{J} = 2$ allows the internal modulators to either operate at half-speed for the same resolution or double the conversion rate for the same speed. This improvement is significant in wide-bandwidth applications where the sampling speed is limited by the technology and resolution requirements.

Original time-interleaved topologies require J individual modulators to achieve an interleaving factor of J [1], [2], therefore, they are referred to as the *multipath time-interleaved* (MPTI) $\Delta\Sigma$ modulators. Modified time-interleaved $\Delta\Sigma$ architectures that require a single modulator with extra quantizers and interconnects have been reported [3]–[7]. Since these topologies require a single modulator regardless of the interleaving order, they are referred to as the *single-path time-interleaved* (SPTI) $\Delta\Sigma$ modulators [4]. Two SPTI modulators have been realized in 0.18-μm CMOS technology: [5] presented a continuous-time implantation and [7] presented a discrete-time implementation. Although SPTI modulators reduce the number of integrators, the requirements of the opamps in these integrator increases significantly as shown later in this brief. Another interesting topology uses time-interleaving within a multirate system to clock all of the integrators at the same low rate [8].

There are two main contributions of this paper. The first contribution is an analysis of SPTI modulators where we see that their sensitivities to opamp bandwidth and dc gain are significantly worse than those of multipath modulators. The second contribution is the presentation of a new modulator by combining multipath and single-path topologies to result in a modulator with better sensitivities and lower power. It should be mentioned that this paper does not deal with the critical path issue in time-interleaved modulators, but that problem can be addressed through the use of output prediction as described in [4].

The outline of this paper is as follows. Section II presents the SPTI derivation procedure which is used later in the derivation of the new topology. Section III evaluates the SPTI architecture with nonideal integrators, compares it to conventional topologies, and identifies the noise transfer function (NTF) mismatch problem. Section IV proposes a hybrid topology that combines the multipath and single-path concepts to alleviate the SPTI NTF mismatch. Finally, conclusions are presented Section V.

II. Method to Build SPTI Modulators From MPTI Modulators

The derivation method for the SPTI discrete-time architecture utilizing a first-order modulator with an interleaving factor of 2 is presented next. The procedure is general and can be applied to any $\Delta\Sigma$ architecture and for any order. The chosen topology is used as an example. The procedure is used later to develop the proposed hybrid topology in Section IV.

The starting point of the derivation is the MPTI modulator [1] with the input analog demux removed and the input-signal fed to both branches of the modulator as shown in Fig. 1(a). Note that the digital output mux is omitted to keep the schematic simple, however, it is added later into the final modulators [Fig. 1(d) and (e)].

Due to the removal of the input demux, both branches of the modulator in Fig. 1(a) sample the same input simultaneously at the reduced rate. This is different from traditional time-interleaved structures where each branch processes alternating samples [1]. The modified sampling has no effect on the NTFs of the modulator, however, the signal transfer function (STF) is changed [6]. The modified STF has a negligible effect on the

Manuscript received February 18, 2008; revised June 01, 2008. Current version published December 12, 2008. This paper was recommended by Associate Editor S. Pamarti.

The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada M5S 3G4 (e-mail: a.gharbiya@utoronto.ca; johns@eecg.utoronto.ca).

Digital Object Identifier 10.1109/TCSII.2008.2008062

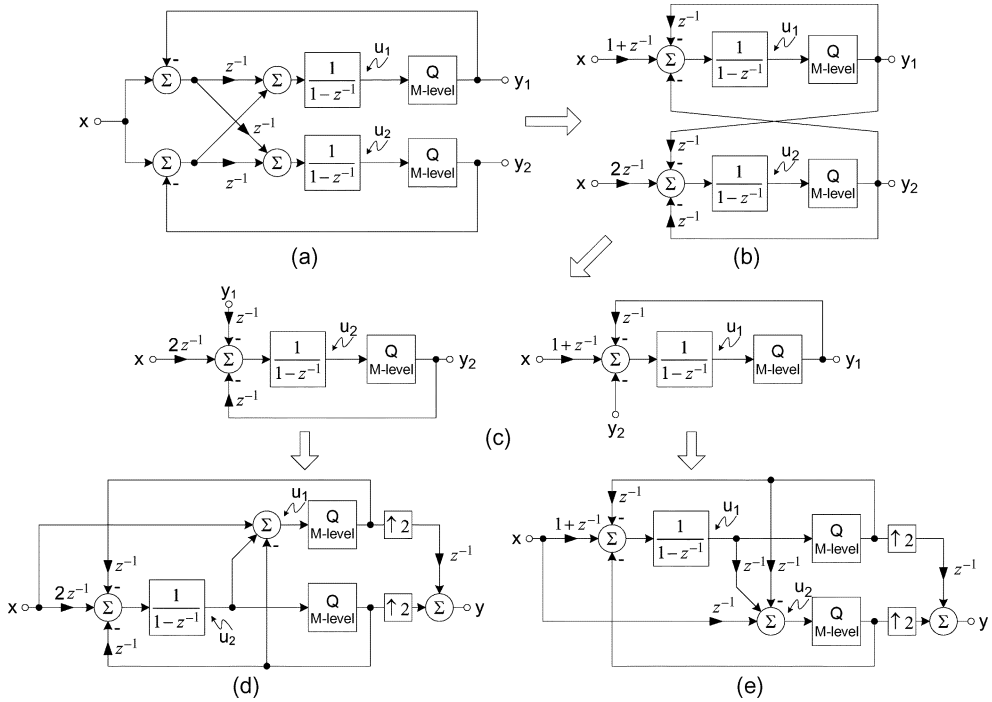

Fig. 1. Transforming a first-order time-interleaved-by-2 MPTI into two first-order time-interleaved-by-2 SPTI modulators. The quantizers in the SPTI modulators [(d) and (e)] require the same number of levels and have similar dynamic range as the original MPTI modulator (a).

achievable SNR. It introduces a notch at half the sampling frequency and an image of the signal [6]. However, due to oversampling, these modifications are not critical.

The first step in the derivation is to determine the outputs of the integrators. They can be derived directly from the block diagram in Fig. 1(a) as

$$u_1 = \frac{1}{1-z^{-1}}\left[(1+z^{-1})x - z^{-1}y_1 - y_2\right] \quad (1)$$

$$u_2 = \frac{1}{1-z^{-1}}[2z^{-1}x - z^{-1}y_1 - z^{-1}y_2]. \quad (2)$$

Next, combine the two adders in the top path into a single adder as well as combining the two adders in the bottom path. With the combined adders, the modulator can be redrawn as shown in Fig. 1(b). Then, the rearranged modulator is split into two separate entities as shown in Fig. 1(c). The only connection between the two halves of the modulator in Fig. 1(c) is the output from the other half. Therefore, if the output needed by one of the entities can be synthesized from variables within it, the other entity can be eliminated. In other words, if we can generate y_2 from x, y_1, and u_1, the right branch can operate as a stand alone time-interleaved modulator. Similarly, if we can generate y_1 from x, y_2, and u_2, the left branch can operate as a stand alone time-interleaved modulator.

To generate a SPTI modulator from the left path, we can manipulate (1) and (2). First, solve (2) for y_1

$$y_1 = z\left(2z^{-1}x - z^{-1}y_2 - (1-z^{-1})u_2\right).$$

Next, substitute y_1 into (1) to yield

$$u_1 = x - y_2 + u_2.$$

Since y_1 is the quantized value of u_1 : y_1 can be generated from x, y_2, and u_2 as desired. Therefore, the left path of Fig. 1(c) can be used as a time-interleaved modulator as shown in Fig. 1(d).

Similarly, to generate a SPTI modulator from the right path, we solve (1) for y_2 and substitute it into (2) to obtain

$$u_2 = z^{-1}x - z^{-1}y_1 + z^{-1}u_1$$

Since y_2 is the quantized value of u_2 : y_2 can be generated from x, y_1, and u_1 as desired. Therefore, the right path of Fig. 1(c) can be used as a time-interleaved modulator as shown in Fig. 1(e).

Using extensive Matlab simulations, the modulators in Fig. 1(d) and (e) are found to have similar performance. The simulations were run for several oversampling ratios (OSRs) and with different number of levels in the internal quantizers. The expected signal-to-noise-plus-distortion ratio (SNDR) at a certain input level and the maximum stable input point are the performance parameters used in the comparison.

The internal quantizers in the SPTI topologies [Fig. 1(d) and (e)] require the same number of levels as the original MPTI modulator [Fig. 1(a)]. In addition, the dynamic range of the quantizer input remains similar, therefore, the quantizer reference voltage does not change. This is because the inputs to the quantizer in both the MPTI and SPTI modulators are mathematically equivalent even though they are synthesized differently. In contrast, a quantizer in the SPTI modulator in [4] requires a larger number of quantization levels with respect to the MPTI topology because of an increase in the required dynamic range. Note that the analog adder at the quantizer input in the SPTI modulator of Fig. 1 is not critical because nonidealities in the adder are noise-shaped when referred back to the input, which is even more significant if a higher order modulator is used.

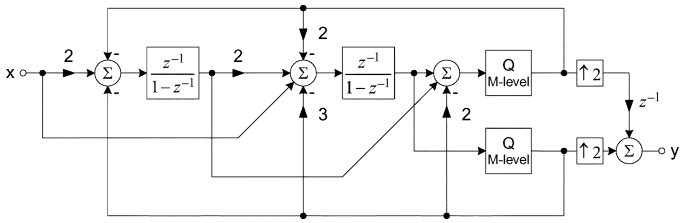

Fig. 2. Second-order SPTI $\Delta\Sigma$ modulator with an interleaving factor of 2 used to evaluate the concept and compare it with CIFB and MPTI architectures assuming finite opamp gain and bandwidth.

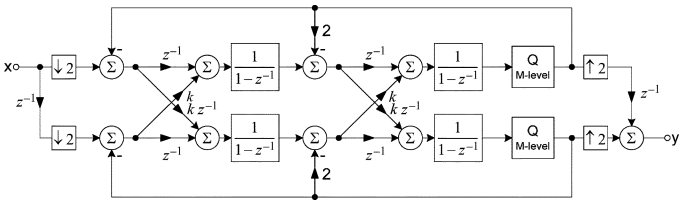

Fig. 3. Second-order MPTI $\Delta\Sigma$ modulator with an interleaving factor of 2 used in the evaluation of SPTI architecture.

Utilizing the zero-insertion concept [2], additional SPTI discrete-time $\Delta\Sigma$ modulators can be developed using the method presented above [9].

III. Evaluation of the SPTI $\Delta\Sigma$ Modulator

Several simulations using Matlab and Simulink are used to evaluate the performance of the SPTI modulator and compare it to traditional structures. The focus of the evaluation is assessing the gain and bandwidth requirements for the opamps in the switched-capacitor integrators such that the modulator can achieve the desired performance. To understand the effect of these non-idealities, consider the delaying non-inverting integrator ideal transfer function as an example:

$$\frac{v_o}{v_i} = \alpha \frac{z^{-1}}{1 - z^{-1}}$$

where $\alpha = (C_S/C_I)$ is the integrator coefficient and C_S and C_I are the sampling and the integrating capacitors respectively. Finite opamp gain (A) introduces a gain error (ε_α) and a phase error (ε_θ) which modifies the integrator transfer function as follows [10]:

$$\frac{v_o}{v_i} = \alpha \frac{(1 - \varepsilon_\alpha) z^{-1}}{1 - (1 - \varepsilon_\theta) z^{-1}}$$

where $\varepsilon_\alpha \approx 1/(A\beta)$, $\varepsilon_\theta \approx \alpha/A$, and $\beta = C_I/(C_I + C_S)$ is the integrator feedback factor.

Next, finite opamp unity-gain frequency introduces a gain error (ε_u) in the integrator output in response to a step input: $\varepsilon_u \approx e^{-t_{\text{settle}}/\tau}$, where t_{settle} is the available settling time which is approximately half of the period, and $\tau = 1/\omega_{-3\text{dB}}$ where $\omega_{-3\text{dB}}$ is the integrator closed-loop bandwidth.

A. Evaluating the SPTI Modulator

The architectural evaluation focuses on comparing opamp gain and bandwidth requirements in the SPTI modulator with traditional MPTI and single-loop topologies. For this purpose, the second-order SPTI modulator shown in Fig. 2 [6] is compared to a traditional second-order cascade of integrators with feedback (CIFB) $\Delta\Sigma$ modulator [11] and the MPTI modulator shown in Fig. 3 [1] with a k-factor of 1. The time-interleaved-by-2 modulators are clocked at half of the rate of the CIFB modulator. In other words, the OSR of the CIFB and the effective oversampling ratio of the time-interleaved modulators $(\text{OSR}_{\text{eff}})$ are equal, hence, their expected SNDR is similar. Note that, since the SPTI architectures in Fig. 2 and in [4] have almost identical results, they are plotted together in Figs. 4 and 7.

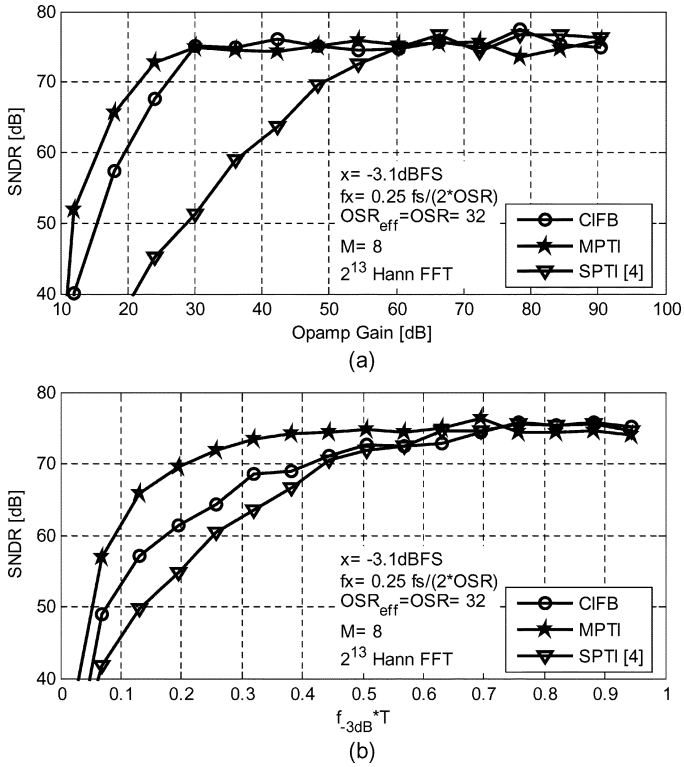

Fig. 4. SNDR versus (a) opamp gain (with infinite bandwidth) and (b) normalized bandwidth (with infinite gain). Opamps in the MPTI modulator require less gain and bandwidth than those in the CIFB topology as expected. This is a desired characteristic that allows the MPTI to achieve higher conversion rate. On the other hand, the SPTI topology requires large opamp gain and bandwidth to achieve the target SNDR which translates to large power consumption.

The simulation results with finite opamp gain and bandwidth are summarized in Fig. 4. The opamps in the second stage have 5% less gain and bandwidth than those in the first stage. In addition, a 2% mismatch between the opamps in the two paths of the MPTI modulator is considered.

We can observe that the MPTI requires less opamp gain and bandwidth than the CIFB which is close to the prediction in [1]. This reduction of circuit requirements allows time-interleaving to achieve higher conversion rates. On the other hand, the SPTI requires much larger opamp gain and approximately the same bandwidth to achieve the same SNDR as the CIFB even though they are clocked at half the speed. In other words, the SPTI topology can not achieve a larger conversion rate if it is opamp bandwidth limited. Furthermore, it needs larger opamp gain than

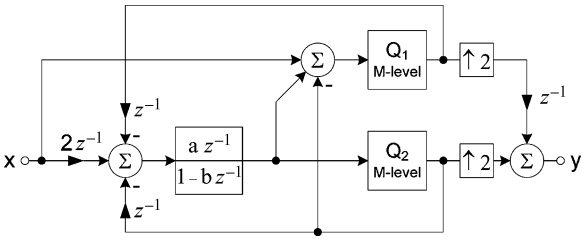

Fig. 5. Time-interleaved-by-2 first-order SPTI $\Delta\Sigma$ modulator with nonideal integrator due to finite opamp gain and bandwidth.

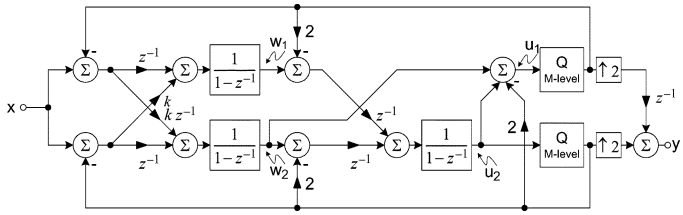

Fig. 6. MPSPTI $\Delta\Sigma$ modulator uses multipath first stage and single-path for later stages to alleviate the NTF mismatch. The MPSPTI saves power when compared to the SPTI because it considerably reduces the required opamps gain and bandwidth for all opamps. Alternatively, the MPSPTI can achieve higher conversion rate for the same opamp gain and bandwidth as the SPTI. Furthermore, the MPSPTI saves power when compared to the MPTI because it uses fewer components with similar requirements. Note that an analog demux can be used at the input since the first stage of the modulator is multipath.

the CIFB which means more power consumption for the same performance. Note that the effect of finite opamp gain was investigated in [3] where the large gain requirements were also observed.

B. Identifying the SPTI Limitation

The first-order SPTI $\Delta\Sigma$ modulator shown in Fig. 1(d) is used in the identification of the cause of the large gain and bandwidth requirements. For this purpose, the modulator is redrawn with non-ideal integrator as shown in Fig. 5. The factors a and b represent the modified gain and phase due to finite opamp gain and bandwidth. Next, the transfer functions of the modulator are derived as

$$\mathrm{STF} = \frac{y}{x} = \frac{z^{-1}\left(1 + az^{-1} + (a-b)z^{-2}\right)}{1 + (a-b)z^{-2}}$$
$$\mathrm{NTF}_1 = \frac{y}{q_1} = \frac{z^{-1}\left(1 - az^{-1} + (a-b)z^{-2}\right)}{1 + (a-b)z^{-2}}$$
$$\mathrm{NTF}_2 = \frac{y}{q_2} = (1 - z^{-1})$$

where q_1 and q_2 are the quantization from the first and second quantizers respectively. We observe that NTF_2 is not affected by the nonidealities at all, however, NTF_1 is modified. Since the overall NTF is a combination of NTF_1 and NTF_2, the mismatch between individual NTFs introduces an error in the final NTF which causes an increase in the noise floor and therefore degrades the achievable SNDR. Therefore, by increasing the gain and bandwidth, the analog integrators become more ideal and the NTF matching improves. The NTFs in higher order SPTI modulators also suffer from the mismatch problem. However, the algebra becomes more tedious and numerical solutions become necessary.

The MPTI modulator, on the other hand, does not suffer from the NTF mismatch problem. This is because each NTF is modified by the errors in a separate path. Thus, assuming the opamps have similar gains and bandwidths, the errors in the different paths are similar, resulting in a small NTF mismatch. Consequently, the gain and bandwidth requirements of the MPTI are less than SPTI.

IV. Mitigating the NTF Mismatch

The SPTI $\Delta\Sigma$ modulator suffers due to opamp nonidealities which results in high gain and bandwidth demands. The stringent requirements are incompatible with high-speed data converters which is the target application of time-interleaving. Therefore, it is essential to develop techniques to reduce the dependence of the SPTI topology on nonidealities in the integrators.

A hybrid structure of an MPTI and SPTI modulator is derived in an attempt to overcome the NTF mismatch problem. The hypothesis here is as follows: if the first stage in the modulator uses multipath topology while later stages use single path, then errors due to the NTF mismatch in the single-path stages are attenuated when referred back to the input.

A second-order multi-path single-path time-interleaved (MPSPTI) discrete-time $\Delta\Sigma$ modulator with an interleaving factor of 2 is shown in Fig. 6 as an example. It can be derived by applying the method presented in Section II to the second stage of the MPTI modulator in [1]. The first step is to determine the outputs of the integrators in the second stage

$$u_1 = \frac{1}{1 - z^{-1}}[z^{-1}w_1 + w_2 - 2z^{-1}y_1 - 2y_2]$$
$$u_2 = \frac{1}{1 - z^{-1}}[z^{-1}w_1 + z^{-1}w_2 - 2z^{-1}y_1 - 2z^{-1}y_2].$$

Next, we can manipulate the above equations to obtain

$$u_1 = w_2 - 2y_2 + u_2.$$

Therefore, u_1 can be synthesized as shown in Fig. 6. Note that the same input signal is applied to both input terminals of the MPSPTI modulator in Fig. 6. Alternatively, since the first stage of the modulator is multipath, the input signal can be applied through an analog demux like the MPTI.

The simulation results with finite opamp gain and bandwidth are summarized in Fig. 7. The opamps in the second stage have 5% less gain and bandwidth than those in the first stage. In addition, a 2% mismatch between the opamps in the two paths of the MPTI and the first stage of the MPSPTI modulators is considered.

As shown in Fig. 7, the MPSPTI modulator requires significantly less opamp gain and bandwidth than the SPTI counterpart. Therefore, even though the MPSPTI modulator requires an extra integrator, it consumes less power than the SPTI topology because each opamp requires considerably less gain and bandwidth. Alternatively, the MPSPTI can achieve higher conversion rate for the same opamp gain and bandwidth as the SPTI. Furthermore, the MPSPTI saves power when compared to the MPTI

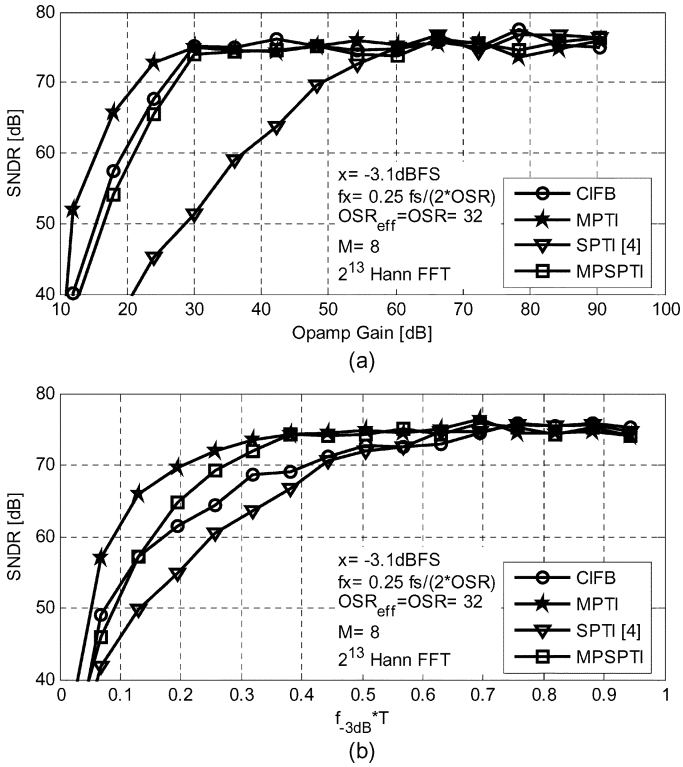

Fig. 7. SNDR versus (a) opamp gain (with infinite bandwidth) and (b) normalized bandwidth (with infinite gain). The opamps in the proposed MPSPTI modulator require much lower gain and bandwidth than the SPTI modulator. Therefore, even though the MPSPTI requires one extra integrator, it saves power by reducing circuit requirements for all opamps. Furthermore, the MPSPTI uses fewer components but with similar requirements to the MPTI, therefore, it consumes less power.

since it uses fewer components with similar requirements. The power saving is even more profound if a higher order modulator is used since only the first stage has to be multi-path while the rest can use single path. In addition, the analog adder at the quantizer input can be implemented passively with low power overhead. However, the k-factor [1] must be set appropriately in the first stage of the MPSPTI topology. Furthermore, the critical path problem due to the quantizers can be overcome by utilizing output prediction [4].

V. Conclusion

The problem of the NTF mismatch in the SPTI $\Delta\Sigma$ modulator due to finite opamp gain and bandwidth was discussed and analyzed. In order to mitigate the problem, the MPSPTI is proposed. It uses fewer circuits than the traditional MPTI $\Delta\Sigma$ modulator while maintaining the relaxed opamp requirements, therefore, it has better power efficiency than the MPTI and the SPTI architectures.

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