

A 2.5mW Sub-GHz RF Receiver Front-End with Enhanced Blocker Tolerance

Zhong Hong Jiang, David A. Johns, Fellow, IEEE, and Antonio Liscidini, Senior Member, IEEE

Abstract— This paper presents a class-AB sub-GHz RF receiver front-end suitable for ultra-low power application. By exploiting transistors' class-AB operation in both the RF and baseband sections, the receiver front-end achieves a very low sensitivity and an elevated blocker tolerance while keeping a low power consumption. Such performance makes the receiver suitable for both short-range and long-range applications. The proposed RF front-end is based on the low-IF architecture with a current-mode LNA, passive quadrature mixers, and 3rd order baseband filtering profile. It has been implemented in 0.13 μ m CMOS technology, operates in the 868/915MHz ISM bands, and exhibits an in-band gain of 50dB, noise figure of 2.7dB, out-of-band IIP3 of +2dBm, out-of-band IIP2 of +37dBm, out-of-band P1dB of -10.5dBm, while draining 2.1mA from a 1.2V supply.

Index Terms—Sub-GHz, class-AB, blocker tolerance, low-IF receiver, IoT, IEEE 802.15.4.

I. INTRODUCTION

The emerging development of Internet of Things (IoT) has opened up a huge market for sub-GHz applications in areas such as sensor networks, smart cities and personal health monitoring systems. Sub-GHz wireless systems have several advantages over their 2.4GHz counterparts, including longer operation range, lower power consumption, and lower cost. According to Frii's law, for a given power consumption, lower frequency signals can travel for a longer distance than higher frequency signals. T-mobile recently announced that its 700MHz (Band 12) Extended Range LTE signals travel twice as far from the tower and four times better in buildings, providing increased coverage and capacity [1]. Since operation range is enhanced for sub-GHz systems, fewer repeaters are needed between the two communication ends. This reduces the

This paragraph of the first footnote will contain the date on which you submitted your paper for review. It will also contain support information, including sponsor and financial support acknowledgment. For example, "This work was supported in part by the U.S. Department of Commerce under Grant BS123456."

The next few paragraphs should contain the authors' current affiliations, including current address and e-mail. For example, F. A. Author is with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: author@boulder.nist.gov).

S. B. Author, Jr., was with Rice University, Houston, TX 77005 USA. He is now with the Department of Physics, Colorado State University, Fort Collins, CO 80523 USA (e-mail: author@lamar.colostate.edu).

T. C. Author is with the Electrical Engineering Department, University of Colorado, Boulder, CO 80309 USA, on leave from the National Research Institute for Metals, Tsukuba, Japan (e-mail: author@nrim.go.jp).

maintenance cost such as deployment cost and battery replacement. Overall, sub-GHz wireless systems seem to be a better candidate for applications that demand a longer operation range with limited power consumption.

The trend in recent works [2], [3] for IoT receiver design is to primarily target ultra-low power consumption (sub-mW) while sacrificing the performance in sensitivity and linearity (i.e., the radio spurious free dynamic range SFDR). Though a low power consumption is important for battery-powered systems, worse sensitivity reduces the operating range by making such solutions not compliant with low power wide area networks (LP-WAN) [4]. Many ultra-lower power receiver designs rely on reducing power supply voltage to reduce overall power. However, the on-chip supply voltage ultimately comes from an off-chip regulator whose voltage supply cannot be arbitrarily low. As a result, the effective power saving depends also on the total current consumption of the circuit. The second issue is the linearity performance. There exists a trade-off between power consumption and linearity, and reducing power inevitably leads to reducing linearity. This compromises the device's co-existence performance, especially in the presence of large interferers. To address the above two issues, this paper proposes a sub-GHz RF receiver front-end solution which targets long-range low power IoT applications. While the proposed front-end in this work is designed based on the IEEE 802.15.4 specification, the general design methodology can be applied to other sub-GHz standards as well, such as LoRa and LTE Cat NB1. The highlight of this work is to introduce the first example at system level how the class-AB operation in both RF and baseband sections can lead to an enhancement in the sensitivity and blocker resilience while maintaining a low power consumption. The paper is structured as follows: In section II the receiver architecture is presented. In section III detailed circuit implementations are reported with emphasis on the class-AB low-noise amplifier (LNA) and class-AB filtering trans-impedance amplifier (TIA). The paper ends with the measurement results and a comparison with the state-of-the-art.

II. RECEIVER FRONT-END ARCHITECTURE

Modern RF receivers commonly adopt either Direct-Conversion or Low-IF architectures to perform quadrature down conversion. For narrow band applications such as IEEE 802.15.4 standard receivers, it is more feasible to choose the low-IF structure due to its insensitivity to DC offset and 1/f noise. To eliminate the DC offset, a high-pass filter can be introduced in the receiver. For low-IF receivers, such a

TABLE I
IEEE 802.15.4 RADIO SPECIFICATIONS

Channel 0	@868 MHz, 600 KHz bandwidth
Channel 1-10	@902-928MHz, 1.2 MHz bandwidth
Channel Spacing	2 MHz
Adjacent Channel Rejection	0 dB
Alternate Channel Rejection	30 dB
Receiver Sensitivity	-92 dBm
Noise Figure	15 dB
Image rejection	21 dB
IIP3	-44 dBm
SNR	6 dB

high-pass filter can be realized with on-chip RC components with feasible size. The $1/f$ noise is also problematic to narrow band systems since a large portion of the signal band will fall into the $1/f$ region, greatly degrading the SNR. For low-IF receivers, this problem is more relaxed because the baseband signal is located at a higher frequency than DC. Therefore, the receiver proposed in this work is based on a Low-IF architecture.

The radio specification of the receiver can be found from the IEEE 802.15.4 standard and is summarized in Table I. The linearity requirement (IIP3) is implicitly inferred from the blocker profile assuming that the intermodulation product (IM3) equals the noise floor (-113dBm). The image rejection requirement is unspecified in the standard, but with proper selection of the intermediate frequency (e.g. $IF < 1\text{MHz}$), the signal in the adjacent channel (0dBc) can be purposely made to be the image of the desired signal. Therefore, an image rejection of 21dB can attenuate the image below the noise floor.

It is also necessary to take into consideration the power consumption of the ADC when designing the front-end. The front-end should filter out most of the interferers to reduce the signal's dynamic range at the output to reduce ADC's resolution and thus power consumption. If interferers are not filtered, the ADC's full-scale (FS) will be dominated by the -62dBm alternate-channel blocker. Together with a -113dBm noise floor, 3dB crest factor (CF) and 10dB additional margin (to take into account mismatch and PVT variation), Eq. (1) suggests that a 64dB SNDR is required for the ADC.

$$SNDR = FS - \text{Noise Floor} + CF + \text{Margin} \quad (1)$$

The power consumption of the ADC can be estimated based on the well-known figure of merit:

$$FOM = SNDR + 10\log\left(\frac{BW}{Power}\right) \quad (2)$$

The state of the art ADC with a 2MHz bandwidth can achieve a 59.6dB SNDR with 820uW power consumption [5]. Assuming the ADC after the front-end achieves the same FOM as [5], the power consumption of a 64dB SNDR ADC will be at least 4mW (it can be even higher due to aliasing, but such effect is omitted for simplicity). If the receiver chain provides a 3rd order filtering with IF at 0.8MHz and cut-off frequency at 1.8MHz, the alternate channel blocker will be attenuated to -77dBm. The required SNDR will then be lowered to around 50dB which

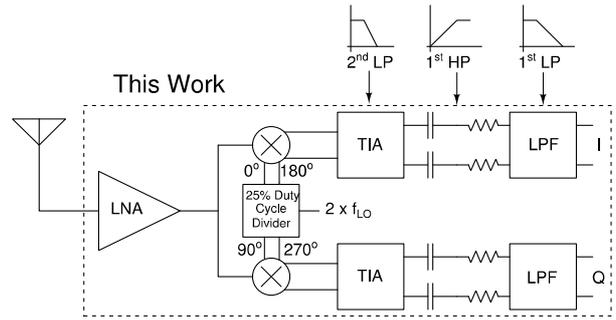


Fig. 1. RX Front-end Block Diagram

results in approximately 160uW power consumption (the I and Q path needs one ADC each and the total power consumption will be 320uW). While the power consumption considered here is a very rough estimation, it nevertheless offers an insight into the choice of the receiver filtering profile. Therefore, the proposed receiver front-end will be designed to have a 3rd order low-pass filtering capability.

RF receivers exploiting class-AB LNA have shown to achieve a promising performance in power usage efficiency and blocker tolerance [6], [7]. Recently, a low power class-AB TIA has also been reported to achieve a high linearity in the receiver baseband [8]. The goal of the proposed solution in this work is to explore the benefit of extending class-AB operation to the entire receiver front-end system. The structure of the proposed receiver is shown in Fig. 1. The LNA is followed by a pair of passive current mixers to implement a low-IF quadrature down conversion scheme. As typically happens in low power RF front-ends, the LNA is single-ended. This choice reduces the power consumption of the RF section and avoids the use of an external balun, which would degrade the RX sensitivity with its insertion loss. The passive mixers, driven by a 25% duty-cycle clock, also perform a single-ended to differential conversion by making the remaining part of the receiver fully differential. An on-chip divider is designed to generate non-overlapping phases from an external LO. The receiver is completed by the analog baseband section where the down-converted current is sensed by a class-AB filtering TIA ac-coupled with a further filtering stage which makes the receiver fully compliant with the IEEE 802.15.4 blocker profile.

In the absence of large interferers, both the LNA and TIA will work in class-A drawing minimum current from the power supply. When large signals show up at the input of the receiver, both the LNA and TIA will operate in class-AB by handling the blockers without saturating the system. The LNA output and the TIA input are biased at the same dc value to ensure that nominally zero dc current flows through the mixer switches [9]. This eliminates the need for large decoupling capacitors at the input of the passive mixers to minimize the impedance seen by the LNA. As a result, the LNA experiences a low output voltage swing even in the presence of large blockers since its load is dominated by the low input impedance provided by the TIA, which is up-converted to the LNA output via the mixer [9]. This

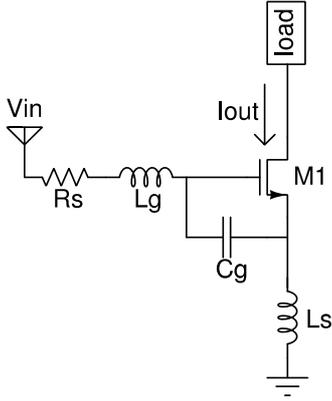


Fig. 2. Classic Common-Source LNA

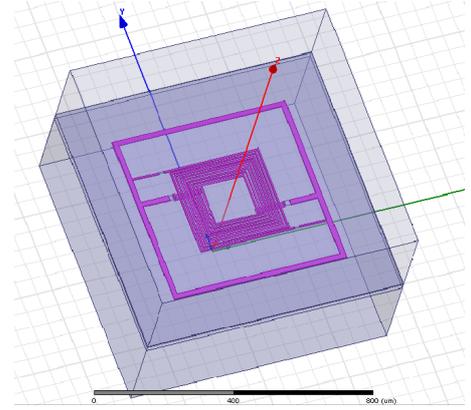


Fig. 4. Interleaved Transformer

$$NF = 1 + \frac{I_{n,M}^2}{4KTg_m^2Q^2R_s} + \frac{I_{n,load}^2}{KTg_m^2Q^2R_s} \quad (4)$$

The passive network at the input not only provides impedance matching but also creates a Q boost on the transistor gate at resonance, which increases the transconductance gain and reduces noise figure. Despite its good performance in gain and noise, this structure suffers from a poor blocker tolerance capability. V_{ov} must be increased to maintain a good linearity under large input swing. However, doing so will require an increase in the power consumption at the same time. Several techniques have been proposed to modify this classic topology to reduce its power consumption and increase its linearity. One of them is the current re-use technique where an n-MOS stage and a p-MOS stage share the bias current thereby increasing the effective g_m for a given bias current [10]. In the design proposed in [10] the structure was biased to operate only in class-A with a limited blocker tolerance. To enhance blocker tolerance without sacrificing power consumption, the LNA can be biased in class-AB [6], [7].

The proposed LNA in Fig.3 uses the PN complementary structure which combines the idea of current re-use and class-AB biasing. The complementary transistors M1 and M4 operate in the weak inversion region to maximize the g_m/I_d ratio. p-MOS transistors are sized two times larger than n-MOS transistors to compensate for their smaller mobility. The transconductance gain and noise figure of this structure are shown in Eq. (5) and Eq. (6).

$$G_m = \frac{g_{mp}Q_p + g_{mn}Q_n}{2} \quad (5)$$

$$NF = 1 + \frac{2I_{n,M}^2}{4KT(g_{mp}Q_p + g_{mn}Q_n)^2R_s} + \frac{I_{n,load}^2}{KT(g_{mp}Q_p + g_{mn}Q_n)^2R_s} \quad (6)$$

The addition of the p-mos input stage approximately doubles the transconductance gain under the same bias current as Fig.2. To understand the noise performance of this structure, a special

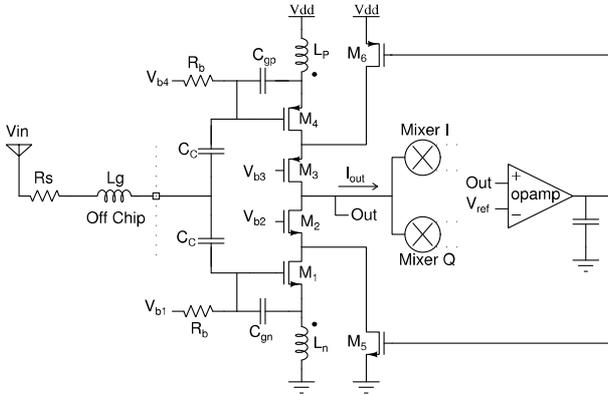


Fig. 3. Class-AB PN Complementary LNA

strategy avoids gain compression at the output of the LNA and improves linearity.

The TIA, with a 2nd order filtering capability, can attenuate large out-of-band blockers at an early stage which greatly improves out-of-band linearity. The TIA together with the channel selection filter create an overall 3rd order Butterworth filtering profile for the receiver front-end. Image rejection will be performed in the digital domain through IQ recombination. With an IF of 800KHz, the baseband signal spans between 200KHz and 1.4MHz. A high-pass filter with a cut-off frequency of as high as 200KHz is sufficient to filter the dc-offset and 1/f noise. The high-pass filter is realized with a passive RC circuit between the TIA and channel selection filter.

III. CIRCUIT IMPLEMENTATIONS

A. Class-AB PN Complementary LNA

The classic inductive-degenerated LNA (Fig.2) has been widely used for narrow band applications because of its high gain and low noise performance. The transconductance gain and noise figure of this structure is shown in Eq. (3) and Eq. (4).

$$G_m = \frac{g_m Q}{2} \quad (3)$$

case is considered where $g_{mp}=g_{mn}=g_m$ and $Q_p=Q_n=Q$. NF is therefore simplified to:

$$NF = 1 + \frac{I_{n,M}^2}{8KTg_m^2Q^2R_s} + \frac{I_{n,load}^2}{4KTg_m^2Q^2R_s} \quad (7)$$

Comparing Eq. (4) and Eq. (7), the noise contribution from active elements is reduced by half, while the noise contribution from the loading is reduced by four times. Since the PN complementary structure requires two inductors, it suffers from a larger silicon area. To reduce the area of the design, L_n and L_p inductors are realized through an integrated transformer (Fig.4) and coupled each other. The g_{mn}/C_{gn} and g_{mp}/C_{gp} ratios have been designed to be approximately the same so that a 1:1 interleaved transformer could be used thereby simplifying the layout and having a full symmetric structure. At sub-GHz frequencies, an off-chip inductor (L_g) is required to resonate the input network and provide the required input impedance matching. The LNA's dc output voltage is set by a current-mode feedback injecting into the source of M2 and M3 via two small transistors M5 and M6. This current-mode approach simplifies the compensation of the feedback loop compared to the other common approach where opamp's output controls directly M1 or M4. The parasitic capacitance introduced by the biasing network is negligible due to its small size.

B. Current-mode passive quadrature mixers

The proposed mixer structure (Fig.5) is the single-ended current-driven passive mixer. Current-Driven passive mixers have been shown to achieve a lower power consumption and lower flicker noise performance compared to active mixers [11] [12]. It also allows baseband low impedance to be up-converted to the RF side and therefore relaxes the linearity bottleneck at the output of the LNA. A single-ended structure is used because LNA is single-ended. To reduce flicker noise, an AC capacitor is usually inserted between LNA and mixer to block DC current flow. There exists a trade-off between the linearity and noise performance when determining this capacitor size. A small size capacitor will increase the impedance seen at the output of the LNA which reduces both the conversion gain and linearity. On the other hand, a large size capacitor will introduce additional parasitic capacitance at the output of the LNA and increase the noise figure. To combat such dilemma, both ends of the mixer can be biased at the same DC level, which ensures zero DC current flowing through and eliminates the need for an AC capacitor altogether. n-MOS transistors are chosen since they can achieve the same on-resistance as p-MOS transistors with a smaller size. A smaller size also means a smaller capacitive loading for the LO generator. A series capacitor C_c isolates the transistor's gate bias from the LO generator thus allows gate bias adjustment.

The operation procedure for this type of mixer has been examined in detail in [13] and an equivalent continuous-time model for the mixer can be constructed as shown in Fig.6. I_{BB} is the down-converted current signal in baseband. Z_{BB} is the input

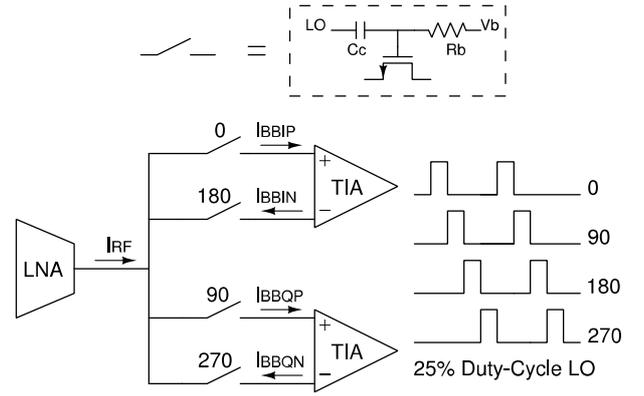


Fig. 5. Current-driven passive mixer

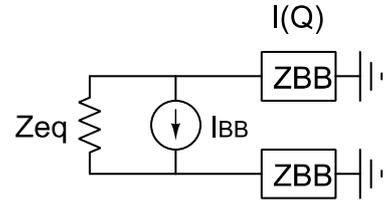


Fig. 6. Continuous-time mixer model

impedance of TIA. Z_{eq} is the impedance looking into the mixer from the baseband and has a magnitude:

$$Z_{eq} = \frac{1+j}{C_{lna}f_{lo}} \quad (8)$$

This continuous time model gives insight on how to dimension the LNA, Mixer and TIA from a system perspective. In this work, C_{lna} is approximately 200fF and f_{lo} is around 900MHz, which leads to $7.86k\Omega Z_{eq}$. A 0.5dB conversion loss due to the current partition between Z_{eq} and $2Z_{BB}$ requires the TIA input impedance (Z_{BB}) to be less than 250Ω . Assuming the TIA has a 40dB open loop gain, the transimpedance in the baseband is limited to $25k\Omega$. Once a specific TIA structure and filtering profile is determined, the total capacitance in the baseband can be calculated, and therefore the approximate area of the baseband circuitry (which is usually dominated by the capacitor bank area) is also determined.

C. Baseband TIA and LPF

In current-mode down-conversion receivers, a low-pass TIA is often used to sense the down-converted current signal and produces a voltage output. Since the TIA is the first baseband stage, its input impedance, noise and linearity can critically affect the performance of the overall chain. A low input impedance is necessary to ensure the theoretical conversion gain of the mixer by maximizing the signal transfer between the RF and BB. It also limits the voltage swing at the output of the mixer to reduce the modulation on the switch resistance when large blockers are present. The goal of the TIA design is to achieve a high gain in the signal band to suppress the noise coming from the following stages, and to provide a high

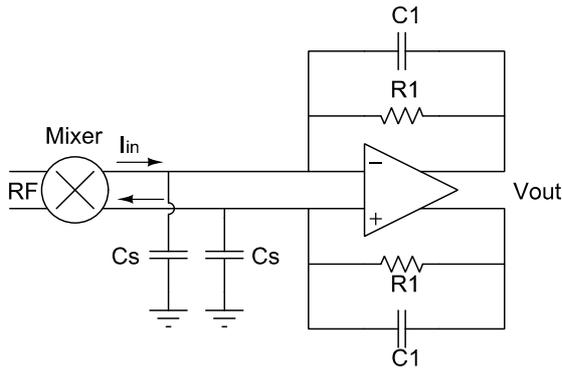


Fig. 7. 1st order active RC TIA

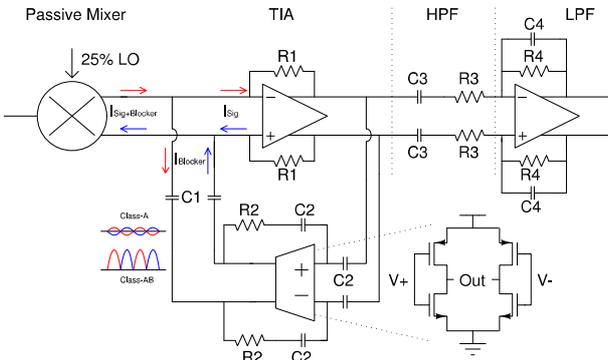


Fig. 8. Class-AB Baseband Circuit

attenuation in the stop band to reject large interferers.

A common TIA structure is the 1st order active RC filter as shown in Fig.7. The trans-impedance gain is provided by the feedback resistor R_1 . A real pole is created by R_1C_1 which achieves a 1st order filtering. At low frequency, the input impedance is R_1 divided by the loop gain of the amplifier and is ideally a virtual ground. At high frequency, a large shunt capacitor C_s maintains a low input impedance as the loop gain of the amplifier drops. This simple structure suffers from several drawbacks. A 1st order filter is insufficient to attenuate large interferers, which can potentially saturate the TIA. Therefore, the gain of the TIA must be compromised in order to maintain a high linearity. A small gain is non-ideal since it not only increases the noise contribution from the following stages, but also increases the baseband area (due to larger capacitance). In addition, a large capacitor C_s should be used to attenuate interferers at the input, which also increases the chip area.

To improve the limitations of a single pole TIA, a TIA topology which exhibits a 2nd order low-pass response and an excellent blocker cancellation capability has been proposed in [8] and is shown as part of the circuit in Fig.8. In the filter pass-band, the feedback path is open (since it's ac-coupled through capacitor C_1) and the current signal goes through the feed-forward operational amplifier (Op-Amp) with a trans-impedance gain of R_1 . On the other hand, in the filter stop-band, the interferers are absorbed by the feedback path through the capacitor C_1 . The two real zeros in the feedback

network (created by C_1 and R_2C_2) become complex conjugate poles in the close-loop transfer function. The finite g_m in the feedback OTA, however, introduces a complex pole in the feedback network which becomes a complex zero in close loop. The transfer function, cut-off frequency, non-ideal zero, and quality factor of the TIA becomes a function of g_m :

$$H(s) = \frac{(s^2 C_1 C_2 R_2 + s(2C_1 + C_2) + 1)R_1}{s^2 (R_1 R_2 C_1 C_2 + \frac{C_1 C_2 (R_2 - R_1)}{g_m}) + s(\frac{2C_1 + C_2}{g_m} + C_1 R_1) + 1} \quad (9)$$

$$\omega_o = \sqrt{\frac{1}{R_1 R_2 C_1 C_2 + \frac{C_1 C_2 (R_2 - R_1)}{g_m}}} \quad (10)$$

$$\omega_z = \sqrt{\frac{g_m}{C_1 C_2 R_2}} \quad (11)$$

$$Q = \frac{\sqrt{g_m^2 R_1 R_2 C_1 C_2 + g_m C_1 C_2 (R_2 - R_1)}}{g_m C_1 R_1 + 2C_1 + C_2} \quad (12)$$

To minimize the effect of the unwanted zero on the filter's selectivity, g_m should be large enough to push the zero at least a decade away from the cut-off frequency. Simulation results show that when such criteria is satisfied, the finite g_m will have negligible effect on the cut-off frequency and quality factor as well. The cut-off frequency of the TIA can be reconfigured by changing C_1 and C_2 , which are implemented as 4-bit binary weighted capacitor banks. The switches are realized with transmission gates and are placed at the side of the capacitors that see a small swing (e.g. input of the Op-Amp and OTA).

The noise and distortion contributed by the feedback network are negligible because they are high-pass shaped by C_1 . Since C_1 is boosted by the feedback network, it can absorb large interferers with a relatively small size. The shunt capacitor C_s can be sized small as well because it is only responsible for draining very far-away interferers in this case. As proposed in [8], the OTA in the TIA's feedback path has been implemented with a complementary topology biasing in class-AB. As a result, the TIA can achieve a low power consumption and low noise during the sensitivity test and a high blocker tolerance in the presence of large blockers [8]. Notice that, the low in-band noise of this topology allows the trans-conductance gain of the LNA to be limited to less than 40mS. This approach not only saves power in the LNA itself but also scales up the impedance level of the filter without saturating the receiver chain. A larger impedance reduces both the area of the baseband section (as discussed in section III-B) and the power consumption in the output stage of the feed-forward Op-Amp.

As mentioned in section I, the receiver should achieve an overall 3rd order filtering capability to relax the dynamic range and hence power consumption of the ADC. As part of the channel selection function (two complex conjugate poles) has already been provided by the TIA, the remaining real pole can be realized by a RC active filter as shown in Fig.9. The filter provides a gain of R_4/R_3 , and a real pole of $1/R_4C_4$. C_4 is also implemented as a 4-bit capacitor bank for cut-off frequency

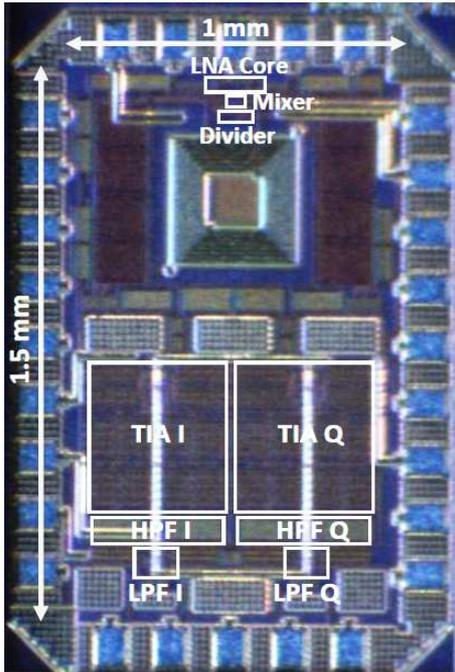


Fig. 9. Die Photo

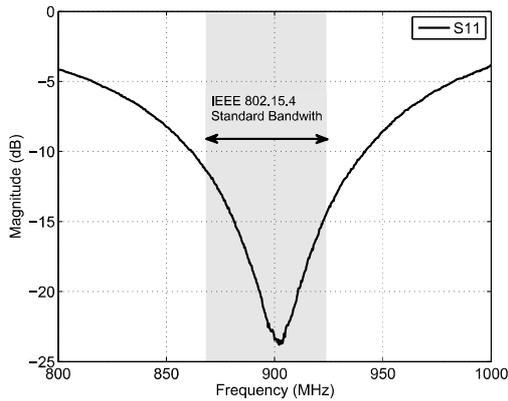


Fig. 10. S11 measurement

reconfiguration. The capacitor bank shares the same control signals with the capacitor banks in the TIA. R_3 and C_3 create a first order high pass filter which is responsible for filtering out the DC offset and flicker noise.

IV. MEASUREMENT RESULTS

The RF receiver front-end prototype was fabricated in 0.13 μ m CMOS technology. It occupies 1mm \times 1.5mm with an active area of 0.5 mm² (Fig. 9). The receiver front-end operates at the 868/915MHz ISM band and consumes 2.46mW in total (0.66mW for LNA, 0.42mW for 25% duty-cycle divider, and 1.38mW for IQ baseband circuits).

The S11 measurement (Fig. 10) shows that good matching ($S_{11} < -10$ dB) is obtained over the desired bandwidth (868MHz-924MHz).

The transfer function was measured by placing a fixed LO at

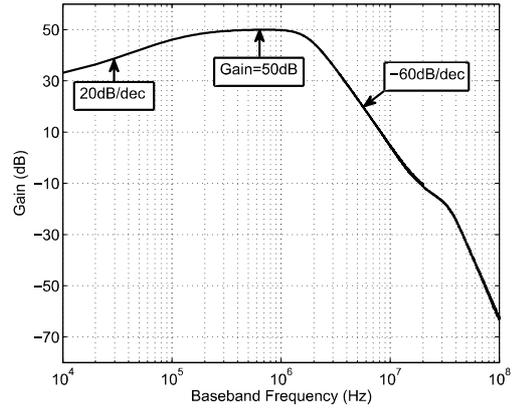


Fig. 11. Transfer Function

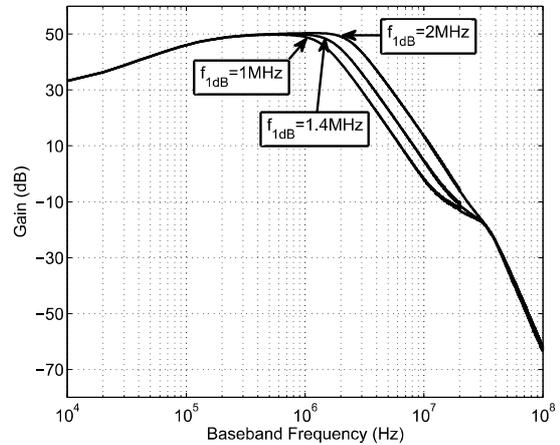


Fig. 12. Reconfigurable bandwidth

1.83GHz (the on-chip divider will then divide it to 915MHz) and sweeping the RF input frequency from LO+10KHz to LO+100MHz. With such setup, the down-converted signal at the I(Q) baseband output spans between 10KHz and 100MHz. Fig. 11 shows the measured transfer function. The receiver front-end achieves a 50dB in-band gain. The 1st order high-pass shape at low frequency is due to the passive high-pass filter between the TIA and channel selection filter (Fig. 7). The stop band achieves a 3rd order Butterworth filtering profile, which provides 15dB and 26dB attenuation on the lower and upper side alternate channel respectively. The small bump in the stop band is due to the finite g_m of the OTA in the TIA feedback path, as mentioned in section III-C. In the absence of large out of band blockers, the small peaking does no harm to the system's linearity. In the presence of large out of band blockers, the OTA will work in class-AB providing a larger g_m proportional to the blocker power and attenuates the peaking [8]. Fig. 12 shows the measured transfer function with reconfigurable bandwidth. By setting the control code of capacitor banks in the TIA and Channel Selection Filter, the 1dB cut-off frequency of the receiver is tunable between 1MHz and 2MHz, which covers the bandwidth requirements for the European and north American bands.

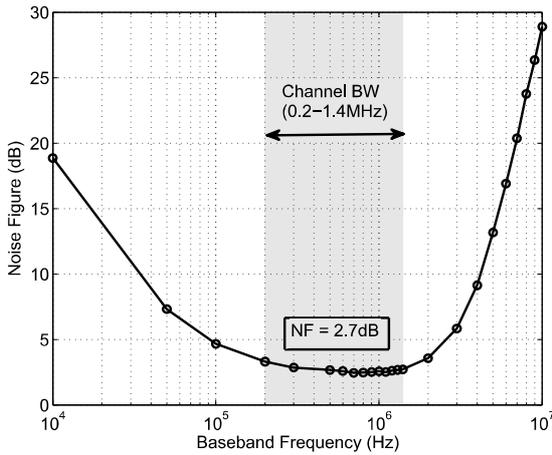


Fig. 13. Noise Figure

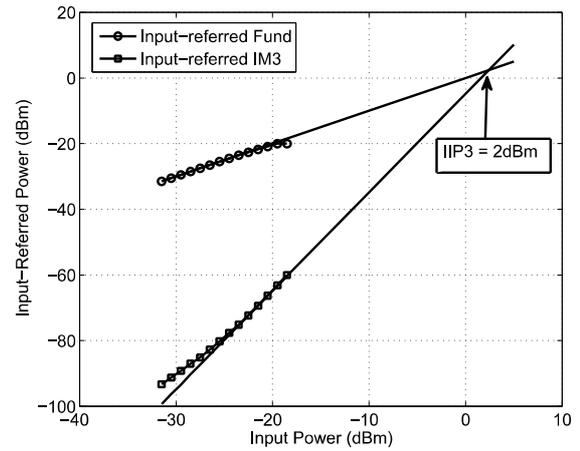


Fig. 15. IIP3 – Two Tones at [LO+50MHz, LO+99MHz]

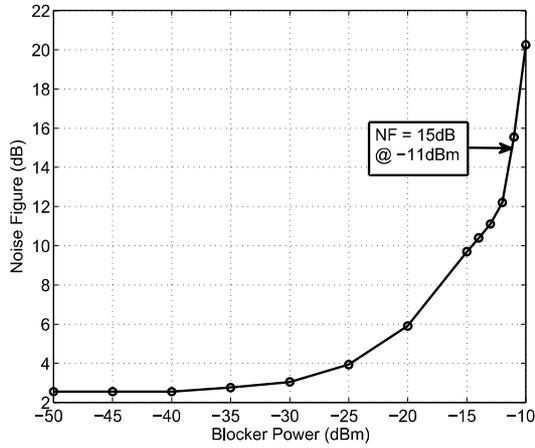


Fig. 14. Noise Figure vs. Blocker Power at [LO+50MHz]

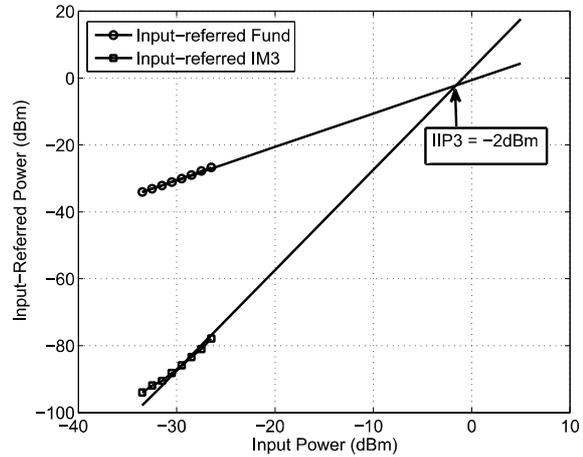


Fig. 16. IIP3 – Two Tones at [LO+10MHz, LO+19MHz]

The noise figure was obtained by terminating the RF input with a 50Ω terminator and referring the noise power at the output back to the input of the receiver. A 20dB-gain on-chip buffer has been implemented after the channel selection filter which boosts the total gain of the receiver to 70dB. Such gain is sufficient to eclipse the additional noise contributed by the test equipment. The average noise figure (NF) over the signal band is 2.7 dB (Fig. 13). To test the NF in the presence of a blocker, the NF was measured with an out-of-band blocker at [LO+50MHz] and its power swept from -50dBm to -10dBm (Fig. 14). The NF is almost unchanged for blocker <-30dBm, and the NF is below the specification's maximum allowable value (<15dB) for blocker <-11dBm.

Linearity tests measure the out-of-band (OB) IIP3, IIP2 and P1dB, and are performed at the maximum gain. The OB-IIP3 test was performed for two scenarios. Two tones at [LO+50MHz, LO+99MHz] were input to the receiver and a +2dbm OB-IIP3 was measured (Fig. 15). The test was then repeated by placing two near-band tones at [LO+10MHz,

LO+19MHz] which resulted in a -2dBm OB-IIP3 (Fig. 16). The OB-IIP2 test was also performed for two scenarios. The first test is the beat frequency leakage due to the mismatch in the quadrature mixers (low frequency beat leaks from RF to BB without frequency translation). To test such effect, two closely-spaced tones at [LO+10MHz, LO+11MHz] were input to the receiver and an IM2 at 1MHz was measured in the baseband. The OB-IIP2 in this case is +37dBm (Fig. 17). The second test measures the IM2 product falling into the signal band due to two farther-spaced tones at [LO+10MHz, 2LO+11MHz] (which create an IM2 at LO+1MHz), and an OB-IIP2 of +35dBm is obtained in this case (Fig. 18). The following relationship can be used to determine the maximum out-of-band blocker the receiver can tolerate for a given OB-IIP2 performance:

$$P_{in-band} + P_{out-band} - IM2 = IIP2 \quad (13)$$

According to the specification, the near band interferer at LO+10MHz is -62dBm. If a maximum 10dB SNR degradation due to IM2 is allowed, the measured OB-IIP2 value allows the

Table II. Performance comparison with the state-of-the-art works

	This Work	JSSC 2014 [2]	MTT 2006 [14]	ESSCIRC 2011[15]	RFIC 2016[16]	CICC 2012 [17]	RFIC 2014 [18]
Technology (nm)	130	65	180	65	180	180	130
Active Area (mm ²)	0.5	0.2	1	0.016	1	0.4	0.12
Architecture	Low IF Single-ended LNA	Low IF Single-ended LNA	DCR Single-ended LNA	DCR/Low IF Single-ended LNA	DCR Mixer First	DCR/Low IF Differential LNA	Low IF Differential LNA
Frequency (MHz)	868/915 ¹	433/860/915/960 ¹	915 ¹	915	900	170/433/868/915/950	960
BW (MHz)	1.2	1.2	1.2	1.2 ⁴	1.2 ⁴	0.01	1.2 ⁴
Gain (dB)	50	50	30	30	34.5	39	59.6
NF (dB)	2.7	8.1	3	9	18.5	6.5	8.2
OB-IIP3 (dBm)	+2/-2	-20.5	-5 ²	-28	+18	-8 ²	-19
OB-IIP2 (dBm)	+37/+35	-	+45 ²	-5	-	-	-
OB-P1dB (dBm)	-10.5	-23	-15 ²	-37	-5	-	-
SFDR (dB) ³	69/66	50	64 ²	44.7 ⁴	69 ⁴	74 ²	51 ⁴
Supply (V)	1.2	0.5	1.8	0.9	1	1.8	1.2
Current (mA)	2.1 ⁵	1 ⁵	2	0.31 ⁵	0.53 ⁵	2.3	2.6 ⁵

1. IEEE 801.15.4 standard 2. In-band linearity test with minimum gain setting 3. $SFDR = \frac{2}{3}(IIP3 - \text{Noise Floor} - NF) - SNR_{min}$ 4. Standard unspecified, number derived based on IEEE 801.15.4 standard 5. Including a clock divider

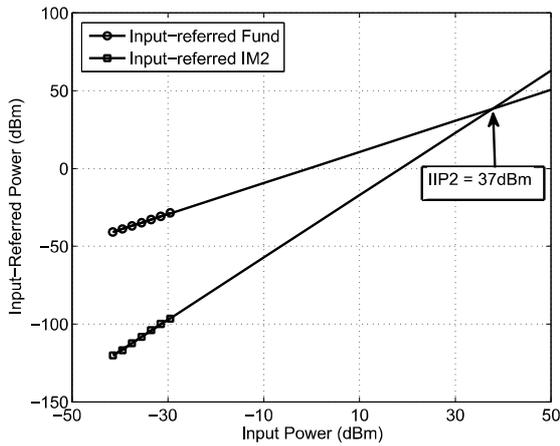


Fig. 17. IIP2 – Two Tones at [LO+10MHz, LO+11MHz]

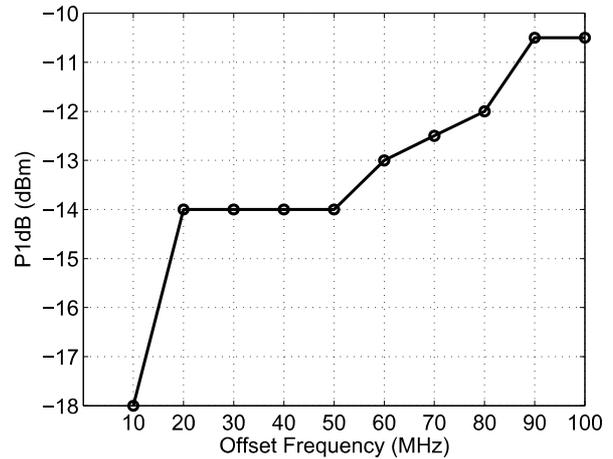


Fig. 19. P1dB compression point test

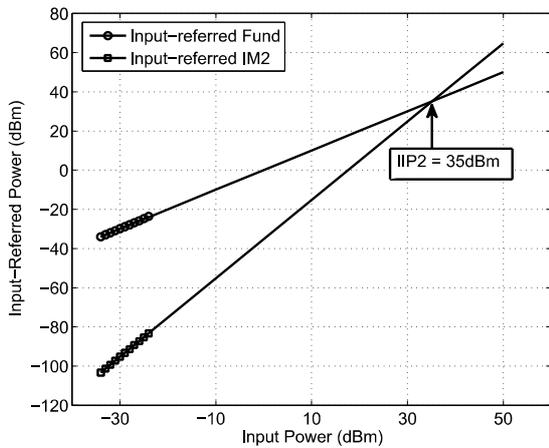


Fig. 18. IIP2 – Two Tones at [LO+10MHz, 2LO+11MHz]

receiver to handle an out-of-band blocker up to -6dBm (which is above the compression point of the system). Finally, the out-of-band P1dB (OB-P1dB) was measured by sweeping the power of an out-of-band blocker until the in-band gain was compressed by 1dB. This test was repeated by placing the blocker at different offset frequencies from the LO and the result is shown in Fig. 19. The receiver front-end exhibits a very high blocker tolerance. The P1dB is -18dBm at a near-band offset frequency (10MHz), and it further increases to -10.5dBm as the blocker offset frequency increases to 100MHz.

Due to the limited number of existing works in sub-GHz receiver design and the lack of description in their measurement setups (especially for linearity tests), it is challenging to present a comprehensive comparison of this work with the state-of-the-art. To the best of the author’s knowledge, previous works with the most comprehensive measurement results are reported in Table II. Compared to [2] and [16], this work consumes more power but achieves a much better performance

in both noise and linearity. A similar noise figure was reported in [14], however, its out-of-band linearity tests were not provided, and its in-band linearity tests were performed with minimum gain setting. In [17], comparable power consumption leads to a much higher noise figure in a channel bandwidth 100 times smaller. Such small bandwidth significantly enhances the sensitivity resulting in a high SFDR. The solutions presented in [15][16][18] did not provide the information regarding the specification, therefore the SFDR was derived based on the IEEE 802.15.4 specification for a fair comparison. While [16] achieves a high SFDR, the high NF makes it infeasible for long range applications. Overall, the proposed class-AB receiver in this work exhibits the best noise figure and a high blocker tolerance compared to the state-of-the-art with a competitive power dissipation.

V. CONCLUSION

This paper presents the design of a low power high SFDR sub-GHz RF receiver front-end. The design exploited class-AB biasing techniques in both RF and baseband sections, resulting in the best in-class sensitivity and an excellent blocker tolerance. The receiver front-end is fully compliant with the IEEE 802.15.4 standard, and its low sensitivity makes it also suitable for the emerging long-range applications.

REFERENCES

- [1] T-Mobile, "T-Mobile 600 MHz Extended Range LTE Now Live in More Than 1,250 Cities & Towns, Laying the Foundation for 5G," [Online]. Available: <https://www.t-mobile.com/news/600-mhz-update-puerto-rico>. [Accessed: 02-Dec-2018].
- [2] Z. Lin, P.I. Mak, R.P. Martins, "A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2990–3004, Dec. 2014.
- [3] A. Selvakumar, M. Zargham, A. Liscidini, "A 600 uW bluetooth low-energy front-end receiver in 0.13 um cmos technology," *ISSCC Dig. Tech. Papers*, pp. 244–245, Feb. 2015.
- [4] J. P. Bardyn, T. Melly, O. Seller and N. Sornin, "IoT: The era of LPWAN is starting now," *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Lausanne, 2016, pp. 25-30.
- [5] M. Yoshioka, K. Ishikawa, and K. Takayama, "A 10b 50MS/s 820uW SAR ADC with On-Chip Digital Calibration," *IEEE ISSCC*, pp. 384–385, Feb. 2010.
- [6] M. Ramella, I. Fabiano, D. Manstretta, R. Castello, "A SAW-Less 2.4-GHz Receiver Front-End With 2.4-mA Battery Current for SoC Coexistence," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2292–2305, Sep. 2017.
- [7] C. Yu et al. "A SAW-Less GSM/GPRS/EDGE Receiver Embedded in 65-nm SoC," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3047–3060, Dec. 2011.
- [8] T. -Liu, A. Liscidini. "A 1.92mW Filtering Transimpedance Amplifier for RF Current Passive Mixers," *ISSCC Dig. Tech. Papers*, pp. 358–359, Feb. 2016.
- [9] D. Murphy *et al.*, "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications," in *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943-2963, Dec. 2012.
- [10] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, R. Castello, "A 2-dB Noise Figure 900-MHz Differential CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1444–1452, Oct. 2001.
- [11] D. Leenaerts and W. Readman-White, "1/f noise in passive CMOS mixers for low and zero IF receivers," in *Proc. Eur. Solid-State Circuits Conf.*, pp. 41–44, 2001.
- [12] S. Zhou and M. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE JSSC*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [13] M. Sosio, A. Liscidini, R. Rinaldo, "An Intuitive Current-Driven Passive Mixer Model Based on Switched-Capacitor Theory," *IEEE TCAS. II, EXPRESS BRIEFS*, vol. 60, no. 2, pp. 66–70, Feb. 2013.
- [14] T.-K. Nguyen, N.-J. Oh, V.-H. Le, and S.-G. Lee. "A Low-power CMOS Direct Conversion Receiver with 3-dB NF and 30-kHz Flick-Noise Corner for 915-MHz Band IEEE 802.15.4 ZigBee Standard," *IEEE Tran. Microw. Theory Tech.*, Vol. 54, No. 2, pp. 735-741, Feb. 2006.
- [15] C. Bryant and H. Sjöland, "A 65nm CMOS 282uW 915MHz Direct Conversion Receiver Front-end," *IEEE ESSCIRC*, 2011
- [16] Omar Elsayed, et al., "A 540 μW RF Wireless Receiver Assisted by RF Blocker Energy Harvesting for IoT Applications with +18 dBm OB-IIP3," *IEEE RFIC*, 2016.
- [17] C. Yeh, H. Hsieh, P. Xu, S. Chakraborty. "Multi-band, multi-mode, low-power cmos receiver front-end for sub-ghz ism/srd band with narrow channel spacing" *IEEE CICC*, 2012.
- [18] R. Srinivasan, Wei-Gi Ho, T. Forbes, R. Gharpurey. "A 2-stage recursive receiver optimized for low flicker noise corner," *IEEE RFIC Symp Dig.*, pp.47-50, June 2014.