Use Asymptotic Waveform Evaluation Method on Transistor-Level Timing Analysis

Zhong Wang

Electrical and Computer Engineering
University of Toronto

Oct 12, 2001

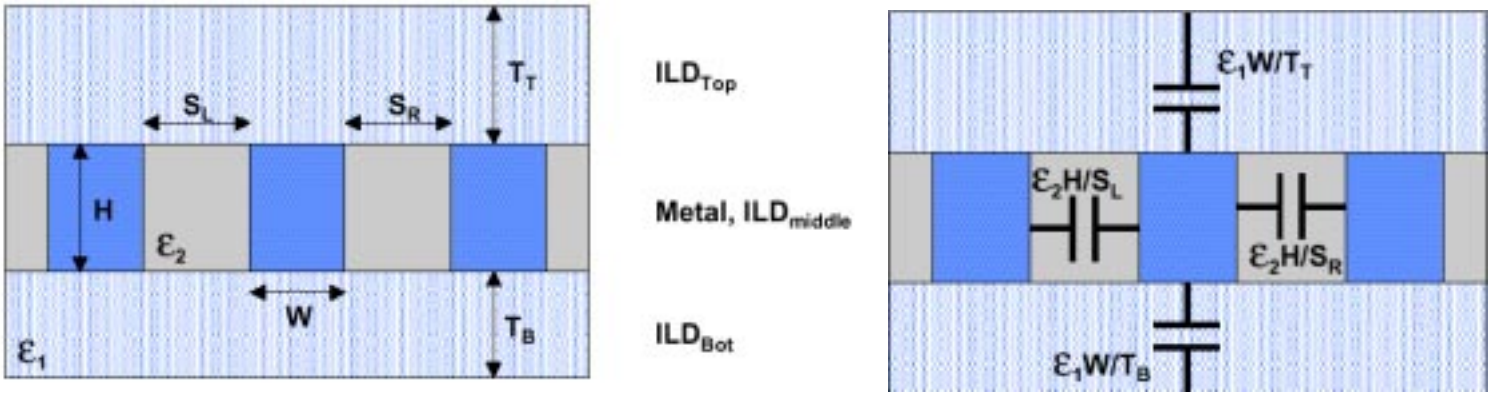
zwang@eecg.toronto.edu
http://www.eecg.toronto.edu/~zwang

Outline

- *Motivation*
- Previous work
- Problems of Spice
- AWE(Asymptotic Waveform Evaluation)
- Results

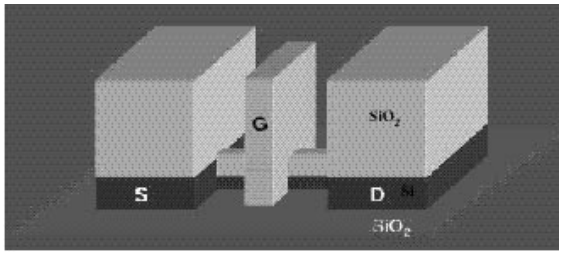
Importance of and Problem with Timing Analysis

- Importance: With shrinking Lambda, interconnect delay becomes the dominant factor rather than transistors
- Problem: Parasitic effect and cross talk(inductance)



Trend in Technology I

- Decreased Feature Size
- Decreased Voltage
- Al $\Longrightarrow$ Cu
- Increased Clock Frequency
- Improved Physical Structure



Trend in Technology II: Transistor Scaling

Depend on whether scale voltage, there is full scaling(scale all by a factor of $S, S > 1$) and fixed-voltage scaling(only scale geometries but not voltage).

Table 1: Scaling Scenarios for Short-Channel Devices

Parameter	Full Scaling	Fixed-Voltage Scaling
W, L, t_{ox}	$1/S$	$1/S$
VDD, V_T	$1/S$	1
$Area$	$1/S^2$	$1/S^2$
C_{ox}	S	S
C_{gate}	$1/S$	$1/S$
k_n, k_p	S	S
$IntrinsicDelay$	$1/S$	$1/S$

Trend in Technology III: Interconnect Scaling

Depending on whether scale height of wire, there is ideal scaling(scale all by a factor of $S, S > 1$) and "Constant Resistance" scaling(keep the height unchanged).

Table 2: Scaling Scenarios for Interconnect

Parameter	Local Wire	Constant Length	Global Wire
W, t_{ox}	$1/S$	$1/S$	$1/S$
H	1	1	1
L	$1/S$	1	$1/S_C$
C	ε_c/S	ε_c	ε_c/S
R	1	S	S/S_C
RC	ε_c/S	$\varepsilon_c S$	$\varepsilon_c S/S_C$

Use Different Metals for Different Purposes

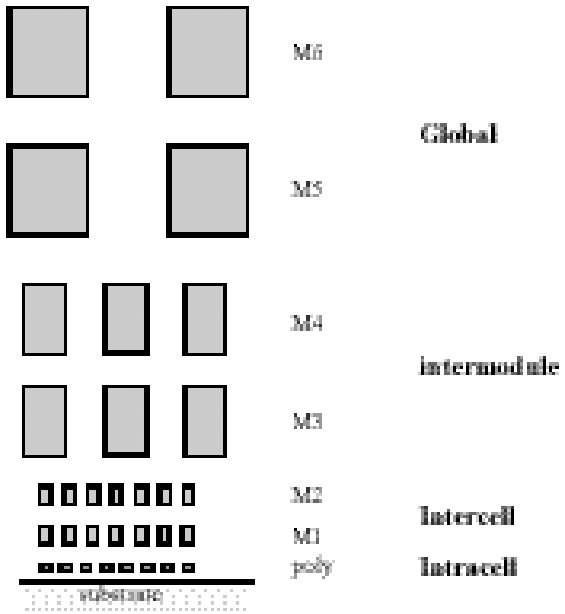


Figure 1: Functionality of Different Metals Layers

Problem of Spice in Timing Analysis

- Overuse: prohibitive long run time
- Dynamic timing analysis: need test pattern
- Accurate spice model of DSM technology
- Not easy to be embedded.

Static and Dynamic Timing Analysis

- Static
  - No test pattern
  - Fix critical path
  - Pros: fast.
  - Cons: pessimistic. Hard to implement. Not suitable for full chip timing analysis
- Dynamic
  - Require test pattern.
  - Analysis result has dependency on test pattern used
  - Pros: Accurate; can target specific test pattern
  - Cons: Need to generate enough test patterns and possibly large run time to get accurate result. Need to build look-up table for all kinds of blocks with different technologies

Approach

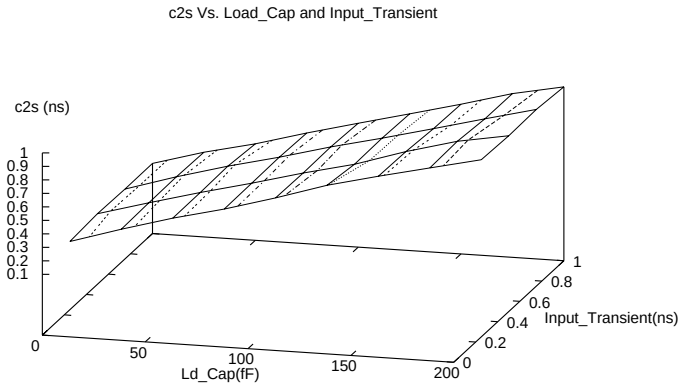
- Static: model the whole circuit as a RC tree(an acyclic network)
- Dynamic: Extract circuit into blocks(gates) connected by interconnects.

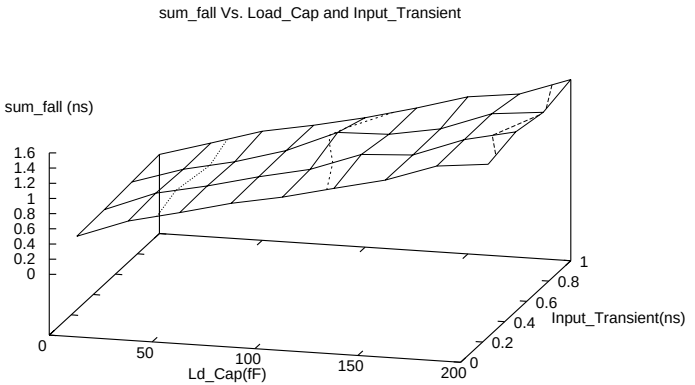
$$Delay = F(input\_slope, output\_load)$$

  - Solve it by table lookup method.
  - The table should have two axes at least: Input Slope and Output Load.

Table Build Up

Here are some examples of data table, which are based on a datapath library simulated with cmosp35 technology.





Dynamic Timing Analysis

We can do dynamic timing analysis in a way like Domino Cards.

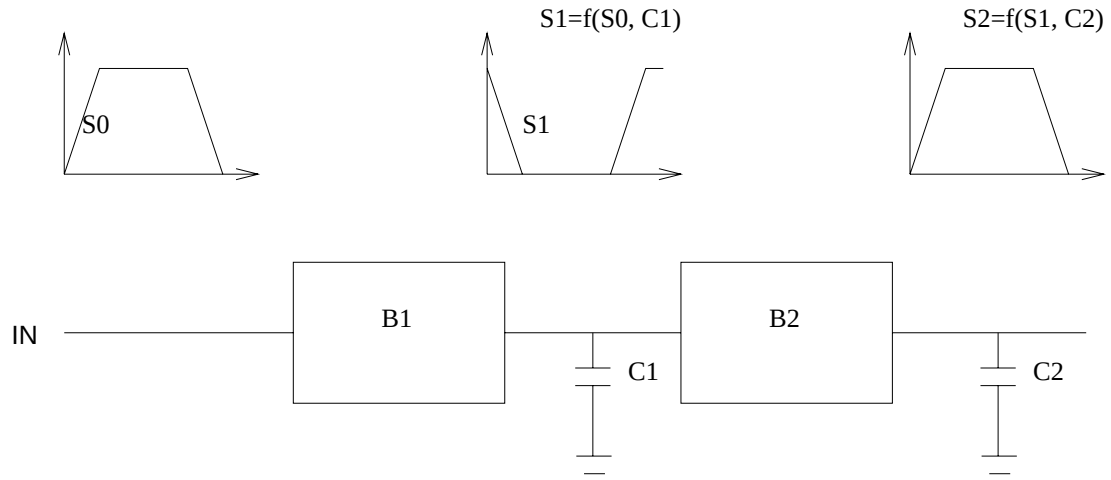


Figure 2: Use Recursive Method for Dynamic Timing Analysis

Use AWE(Asymptotic Waveform Evaluation) Method for STA

- "Asymptotic Waveform Evaluation for Timing Analysis", Pillage, L.T. and Rohrer, R.A. IEEE Transaction on CAD,April, 1990.
- For Interconnect delay analysis
- 1000 times faster than Spice but maintain an accuracy of with 10% of Spice
- Limit: mid frequency; linear RLC: floating capacitors, grounded resistors, inductors and linear controlled source.

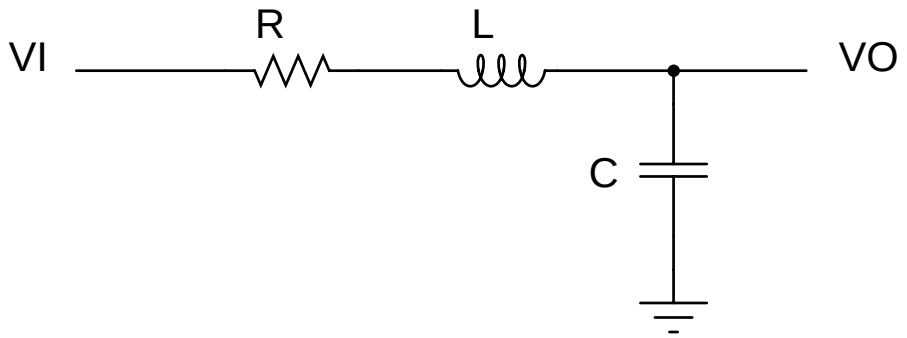
Transfer Function I

- Transfer function can help us come out with output easily. It is defined as:

$$H = \frac{Y}{X}$$

- We usually do Laplace transformation to a system since it is hard to derive transfer function at time domain especially RLC network:

$$\frac{VI}{VO} = \frac{\frac{1}{sC}}{R + sL + \frac{1}{sC}}$$



Transfer Function II

- We can derive from transfer fuction the characteristics of the system in time domain.
  - Bode Diagram
  - Nyquist Diagram
- Change the function into poles and residues format.

$$H(s) = k_\infty + \sum_{k=0}^{\infty} \frac{r_k}{s - p_k}$$

- If all poles are in the left hand side. The system is stable, otherwise it is not stable.

Time Domain to Frequency Domain

For linear circuit, if C and G stands for capacitor(and inductor) and admittance matrix respectively, there is:

$$\begin{cases} C\boldsymbol{X'} = -G\boldsymbol{X} + bu \\ \boldsymbol{Y} = 1^T \boldsymbol{X} \end{cases}$$

Do Laplace transformation and define

$$\begin{aligned} H(s) &= \boldsymbol{Y}(s)/U(s) = k_\infty + \textstyle\sum_{j=1} \frac{k_j}{s-p-j} \\ &= \mathbf{1^T(I + sA + s^2A^2 + \ldots)r} \\ &= \textstyle\sum_{k=0}^{\infty} m_k s^k \end{aligned}$$

as the transfer function. p_j are the poles. Continue to do Taylor expansion.

Moment Matching

- Moment is defined as the coefficients in the above equation

$$H(s) = \sum_{k=0}^{\infty} m_k s^k$$

- First order is actually Elmore delay model
- AWE or PVL method use matrix manipulation to match these moments.
- Poles at right hand side should be handled properly.

Back to Time Domain

- Since $L^{-1}(\frac{k}{s-p}) = ke^{pt}$, if all the k_j and p_j are derived, we can reconstruct the H in time domain.
- $H(s)$ equals to $Y(s)$ under the condition of pulse input.
- Actually, we don't need to generate moments explicitly while still get the targeted waveform. The moments are matched implicitly

MATLAB Simulation Result

In the RC tree below, besides lumped C, there are two bridging capacitors too.

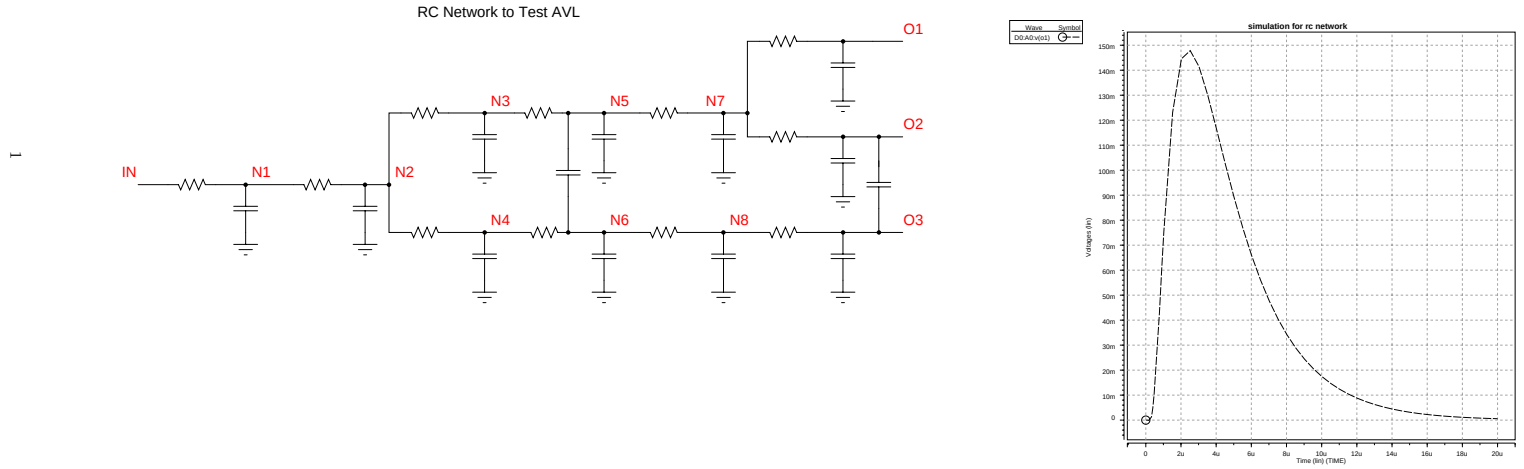
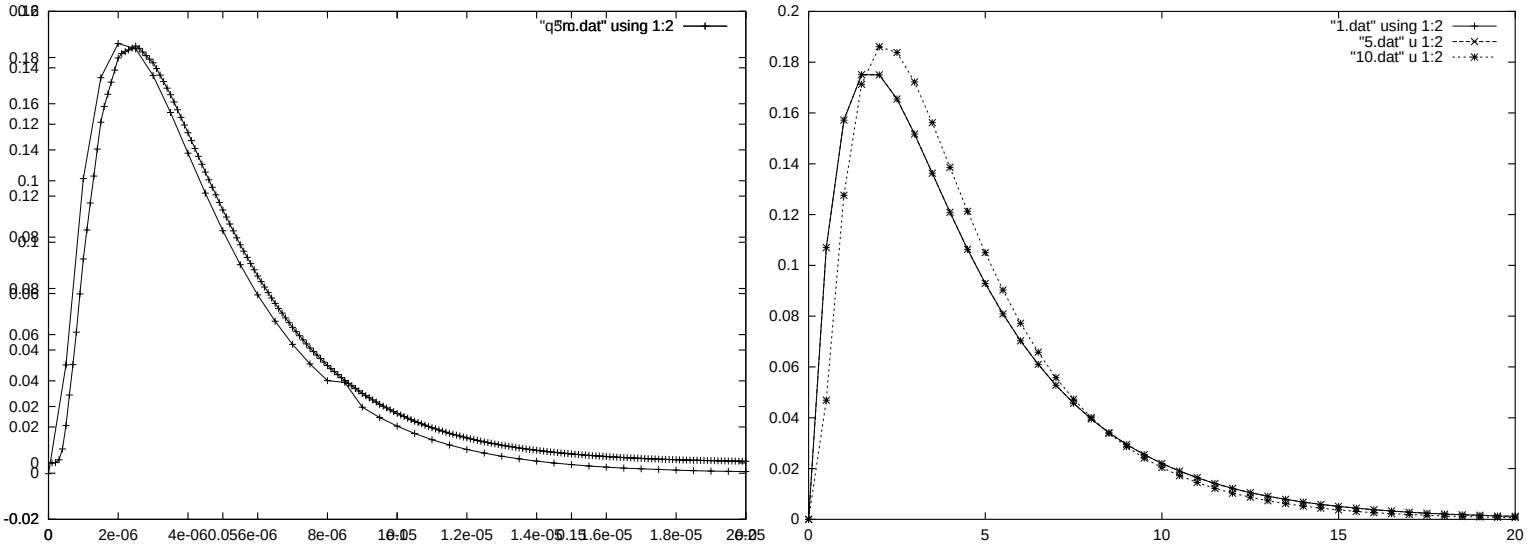


Figure 3: Spice Simulation of Pulse Response of a Simple RC Tree

AWE and PVL Simulation Result

Figure 4: AWE(3 and 5 iterations) and PVL(5 and 10 iterations)



Problem with AWE

- Poles at right hand side
- Usually cannot just increase iteration number to get better result
- Use PVL(Pade Approximation via the Lanczos Process)
  - More accurate higher order approximation
  - Not sensitive to poles at right hand side
  - Does not increase complexity
- Hurwitz Table Method
  - Incremental and Hierarchical

Practical Problem

- Extraction of DSM technology layout
- Passivity and Stability
- Hierarchical and Incremental
- Matrix Manipulation
  - Moment Preserving Modeling Reduction
  - Model Reduction based on Frequency