Automatic Design Scaling

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Outline

- Motivation
- Scaling Methodology
- Analysis and Results
- Conclusion

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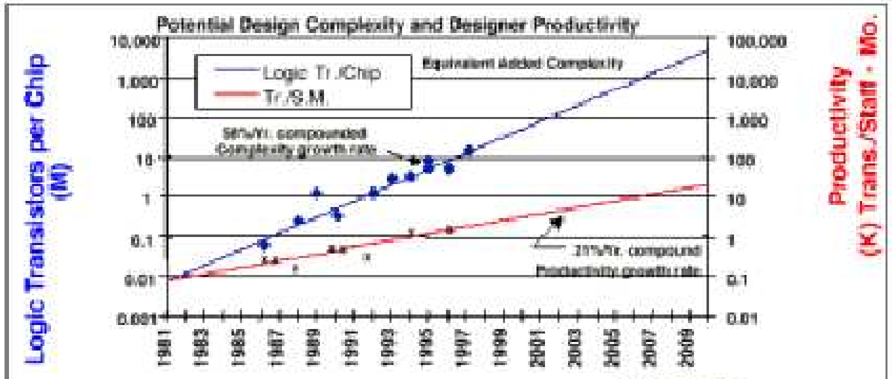
Motivation

- Fast progress towards small feature size in CMOS technology
- Re-design complex systems is expensive
- Develop a methodology to convert exsiting designs for use in the latest technology



Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

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Automatic Design Scaling

- A tool which the designer can use to create a new layout that conforms to the new target design rules from the existing design
- Translate an ARM8 microprocessor from 0.6 to 0.2 micron technology
- The method is implemented in Cadence Skill code

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Scaling Methodology (1)—Scaling Factor

- different rules scale differently between technologies
- scaling factor determines how much we can shrink

Rule Name	Scaling To:					
	0.25	0.3	0.35	0.4	0.45	0.5
Active Spacing	*	*				
Poly-Active Spacing	*	*	*			
N+/P+ Implant Spacing	*	*	*	*	*	
Contact Width	*					
Contact Spacing	*	*				
Contact-Active Spacing	*					
Via1 Width	*	*	*			
Via1 Spacing	*	*	*			
Via2 Width	*	*	*			
Via2 Spacing	*	*	*			

Figure 1: Design Rule Violations For Different Scaling Factors

(Violations are denoted by an asterisk and a shaded box)

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Scaling Process

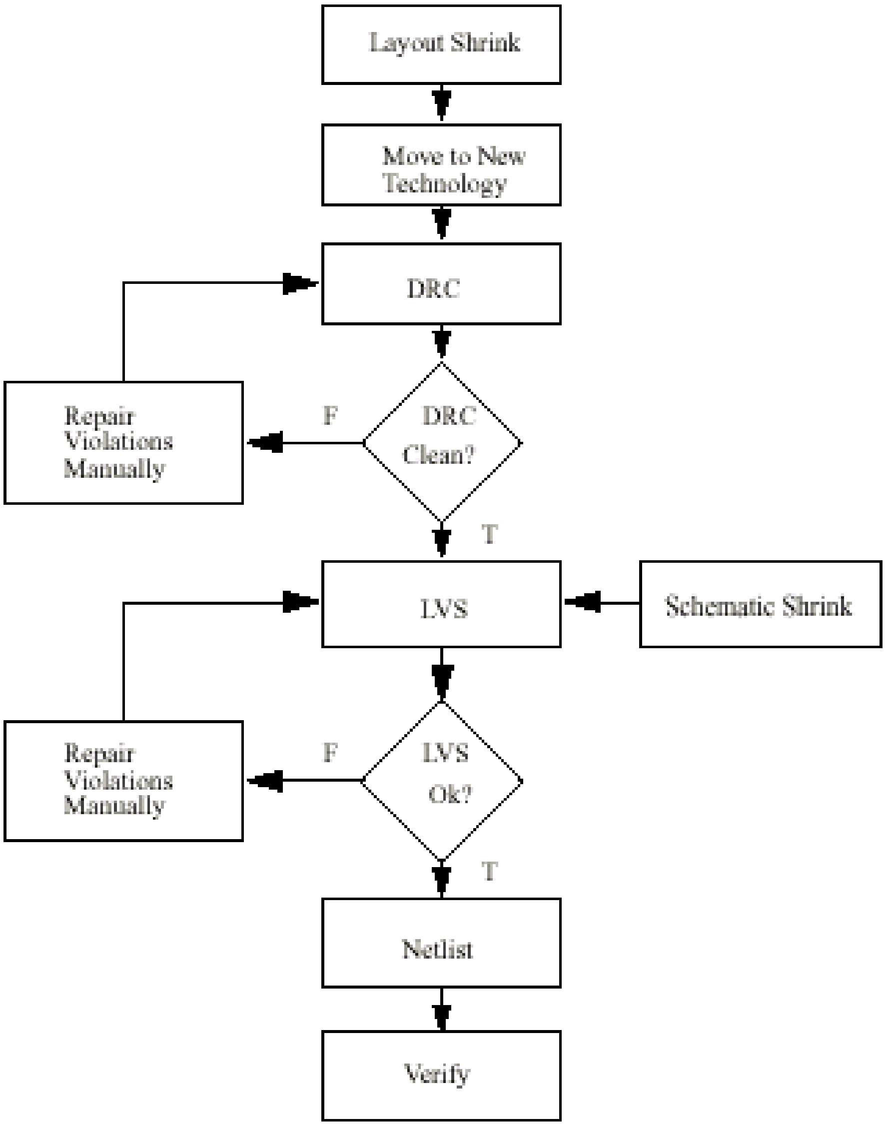

Figure 2: The scaling process

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Layout Scaling

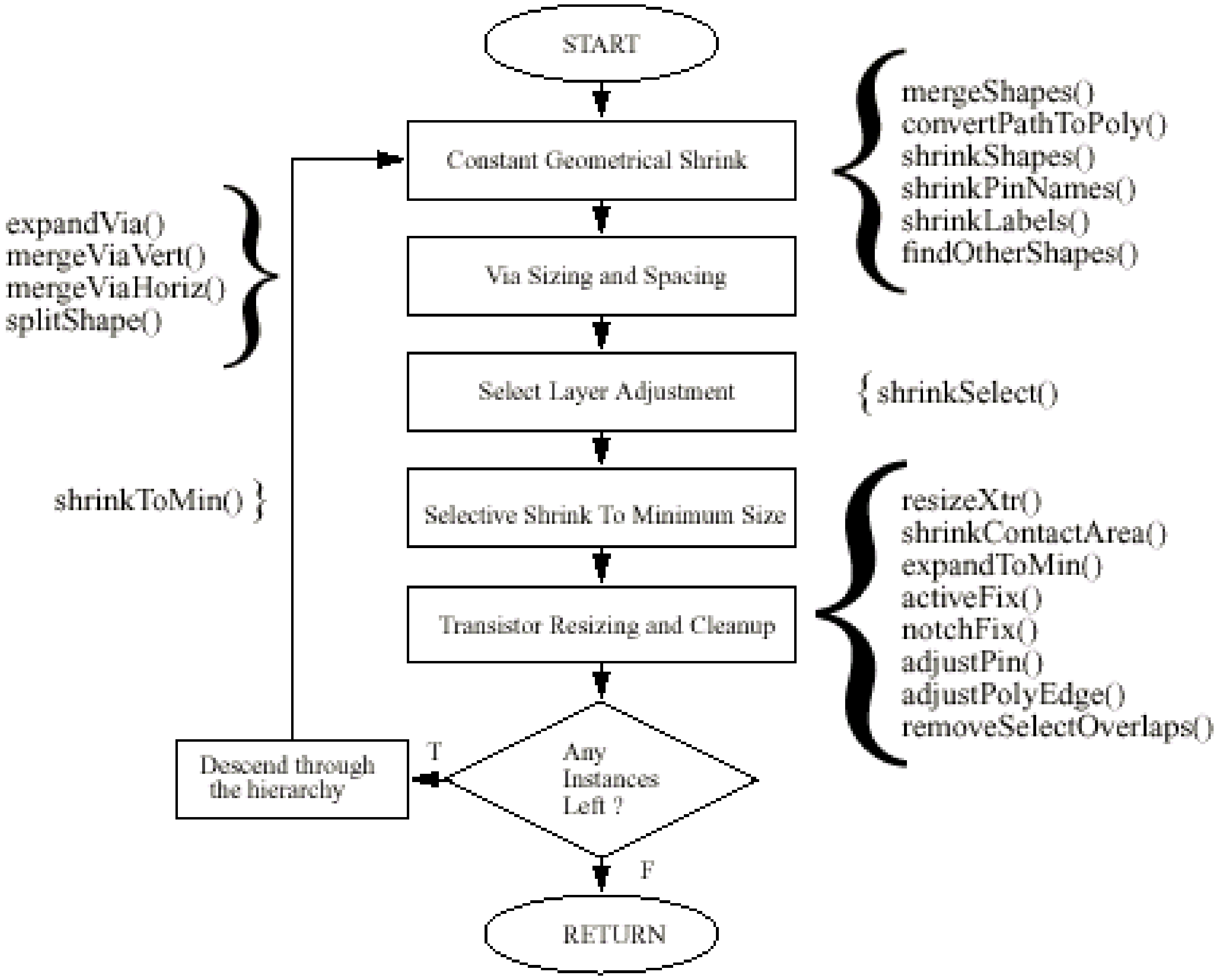

Figure 3: Layout scaling process

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Constant Geometrical Shrink

- Merge all overlapping shapes from same layer
- Shrink all rectangles
- Shrink all polygons
- Shrink all labels
- Report any other shape encountered

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Via Sizing and Spacing

- Problem: Direct scaling results in vias smaller than required minimum sizes
- Solution: expand vias to the correct sizes

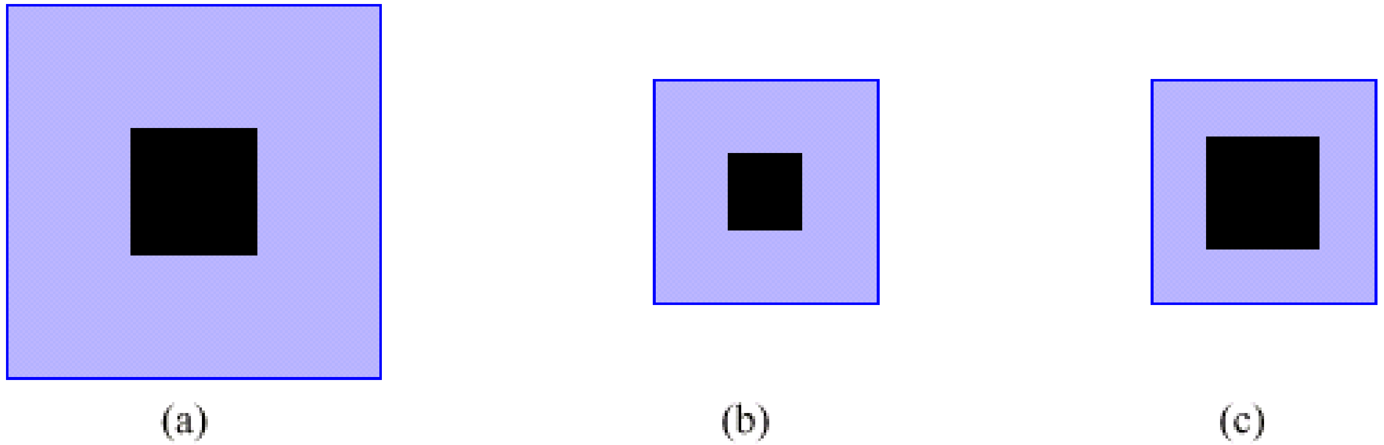

Figure 4: Via Scaling (a) Original 0.6 micron via (b) After linearly scaling to 0.35 micron and (c) after expanding the via to its correct size

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Via Array Spacing

- Problem: Expansion creates spacing violation
- Solution: merge vertically and merge horizontally

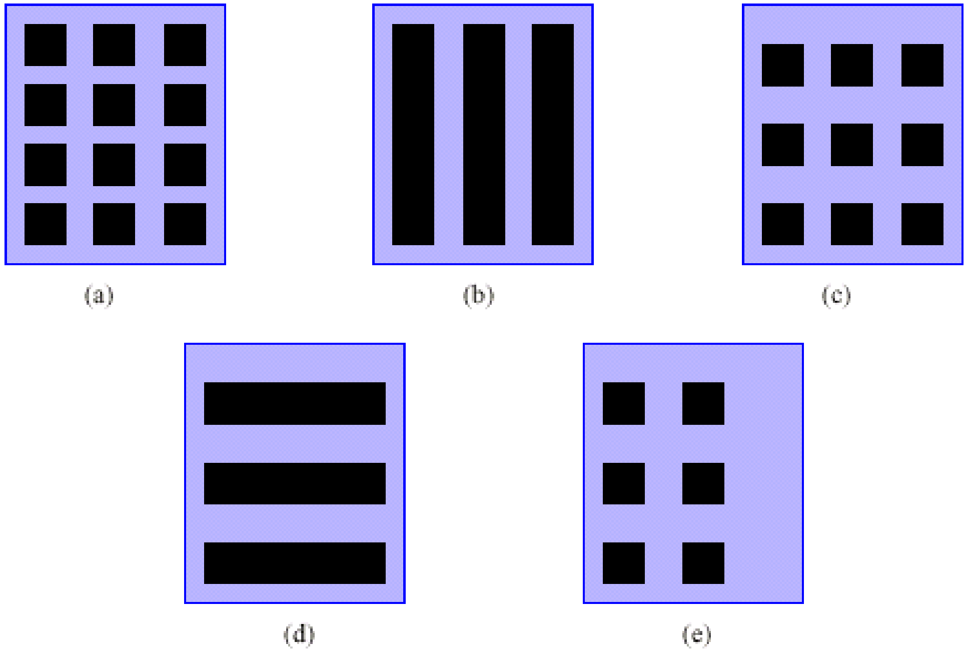

Figure 5: Via Array Spacing. (a) Original via array with the vias spaced too close to each other (b) Vias merged vertically (c) vias spaced vertically (d) Vias merged horizontally (e) Final horizontal spacing

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Select Layer Adjustment

- Problem: Select Layer spacing violation
- Solution: Move all select layers inwards to create adequate spacing

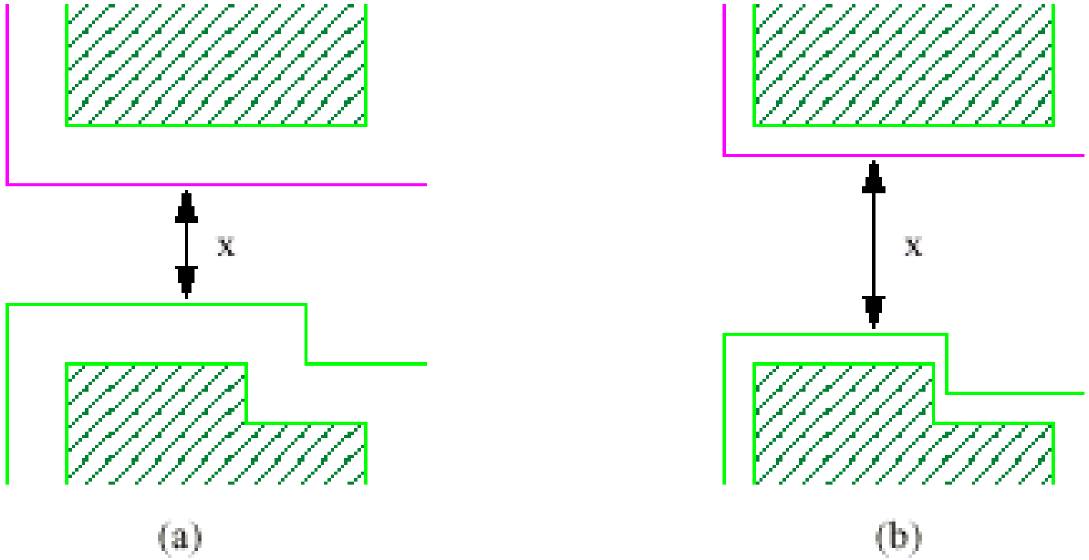

Figure 6: Select Layer Adjustment. (a) Before the adjustment, x is less than minimum spacing (b) The adjustment removes the spacing violation

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Selective shrink to Minimum Size

- Trace layers with minimum size in the original 0.6 micron layout
- Further shrink to minimum size in 0.25 micron layout
- Problem: Minimum design grid is violated
- Solution: Increase the width of lines and places them on grid

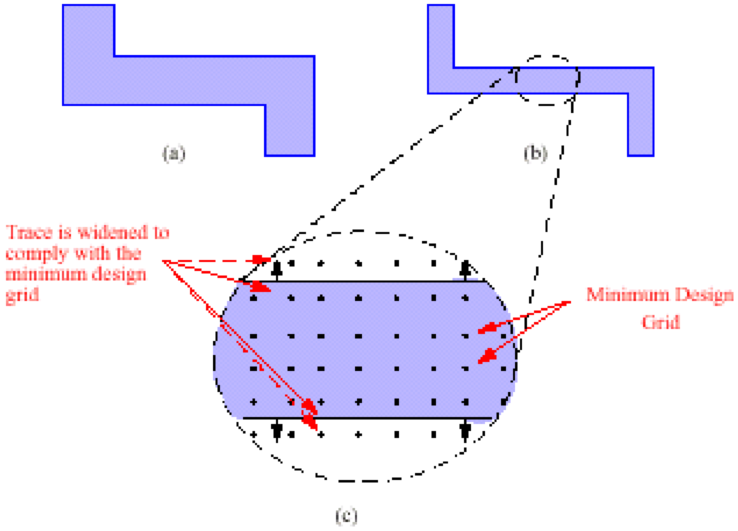

Figure 7: Grid Adjustment.

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Transistor Resizing

- Problem: Width of transistors should be adjusted according to poly shrinking
- Solution: Identify transistors and chop active layers so that W/L ratio is maintained
- Problem: Minimum design grid is violated
- Solution: increase the width of lines and places them on grid

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Transistor Resizing (cont'd)

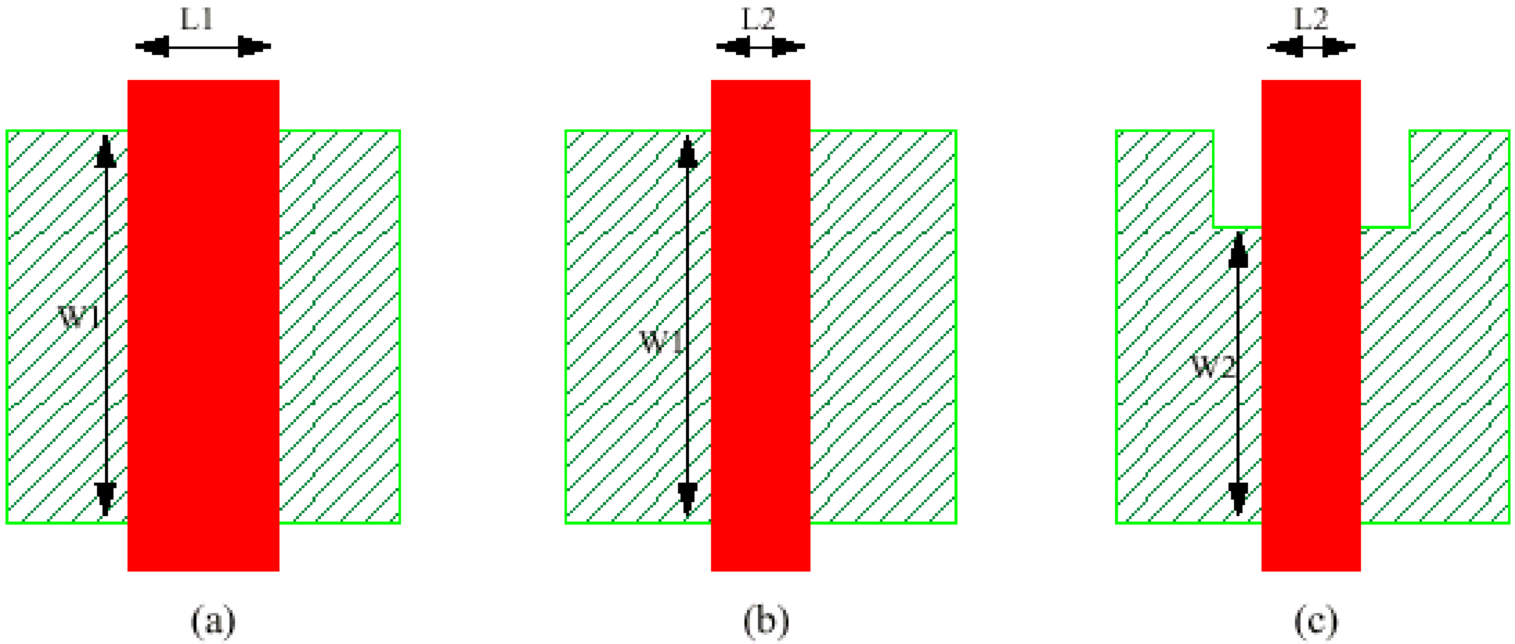

Figure 8: Adjusting Minimum Sized Transistors

(a)transistors scaled to 0.35 microns (b)poly width reduced to minimum size (c)width adjusted appropriately

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Cleanup

- Problem:
  - Many shrink and expand actions resulted in notched figures
  - Pin layers were left untouched while underlying layers wre altered
- Solution:
  - Trace through each cell and fix any notches by filling them or trimming them
  - Adjust pin layers to correspond with underlying drawing layers

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Cleanup (cont'd)

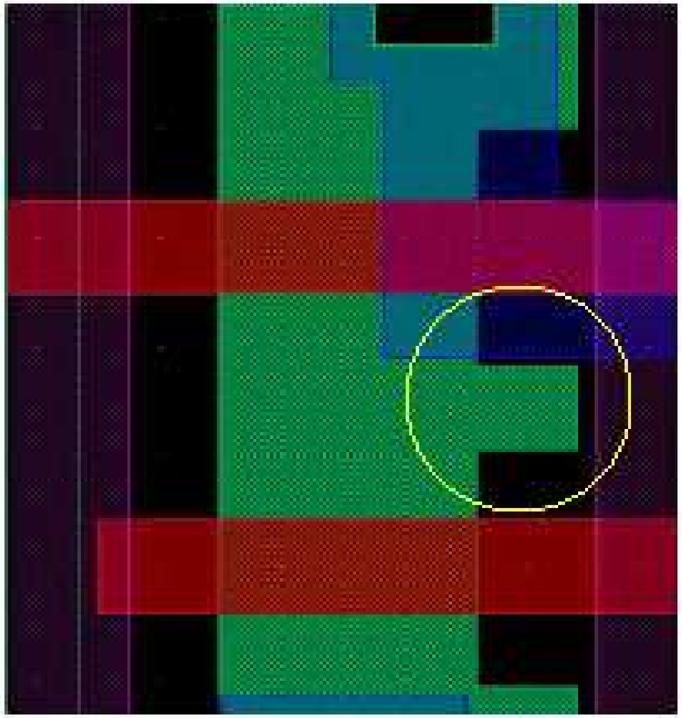

Figure 9: Notch Removal

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Hierarchy Scaling

- Background: Most complex layout keeps hierarchy structure
- Method: Using a recursive algorithm, scaling procedure described before are repeated for each cell in the design
- Problem: Adjacent cells may produce spacing or other rule violations
- Solution:
  - Make a copy of each layer from child cell in the parent cell
  - Create patches in parent cells where violations occur

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Schematic Scaling Procedure

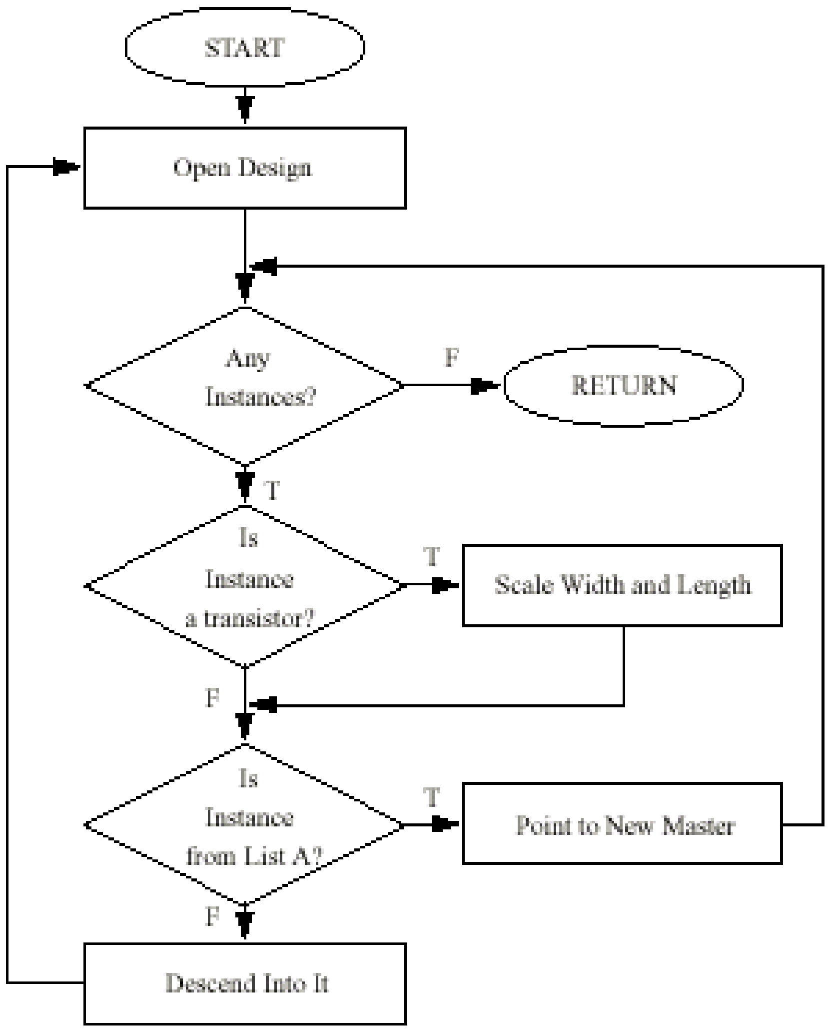

Figure 10: Schematic Scaling Process. (List A refers to all transistors, I/O pins, VDD , Gnd, and any parametrized instance)

Moving to New Technology

- problem: layout hasn't been pointed to the new technology
- solution: stream out layout to GDSII format and then stream them into Cadence database using new technology layer numbers

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Verification

- Run DRC
- Correct further violations manually
- Run LVS

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Analysis—Area

- ARM scaling to 0.25 micron produce a five fold area savings

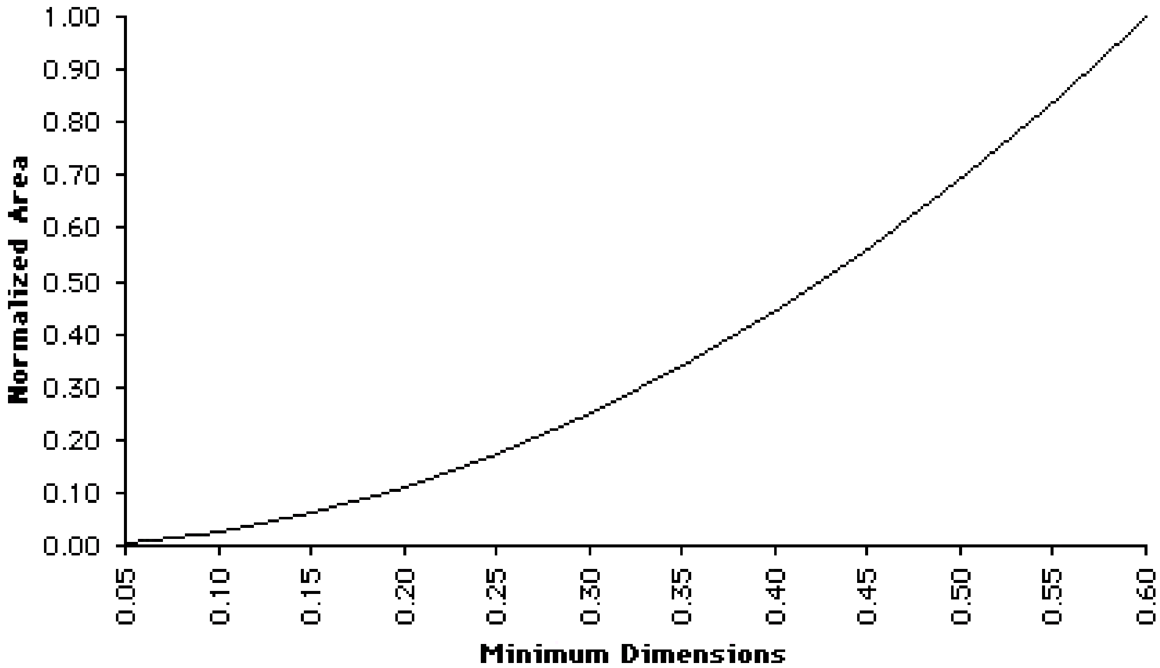

Figure 11: Design Area

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Analysis—Capacitance

- gate capacitance comparison

$$C_G = W \times L \times C_{OX} = L \times 1.5L \times \frac{\varepsilon_{OX}}{T_{OX}}$$

$$C_{RATIO} = \frac{C_{Gnew}}{C_{Gold}} = \frac{L_{new}^2 \times T_{OXold}}{L_{old}^2 \times T_{OXnew}} = \frac{L_{new}^2 \times 94}{0.6^2 \times 50}$$

Gate Length [µm]	C_{RATIO}
0.25	0.33
0.30	0.47
0.35	0.64
0.40	0.84
0.45	1.06
0.50	1.31
0.55	1.58
0.60	1.88

Figure 12: Gate Capacitance Ratio for Different Gate Lengths

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Analysis—Capacitance (cont'd)

- Interconnection capacitance comparison

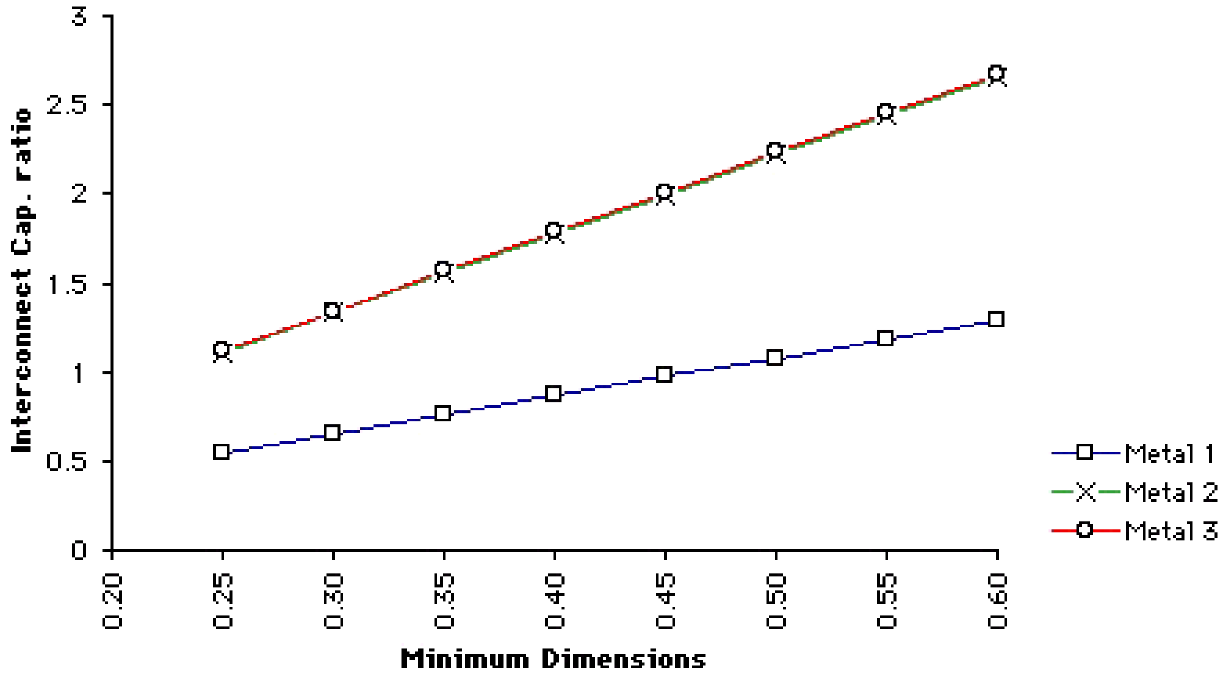

Figure 13: Interconnect Capacitance Ratio

Layer	Capacitance per Length [fF/mm]	
	0.6 micron technology	0.25 micron technology
Metal 1	72.3	93.7
Metal 2	28.1	74.7
Metal 3	24.6	65.9

Figure 14: Interconnect Capacitance per Unit Length

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Delay

- Compare propagation delay of a transitor with gate capacitance as load and interconnect capacitance as load

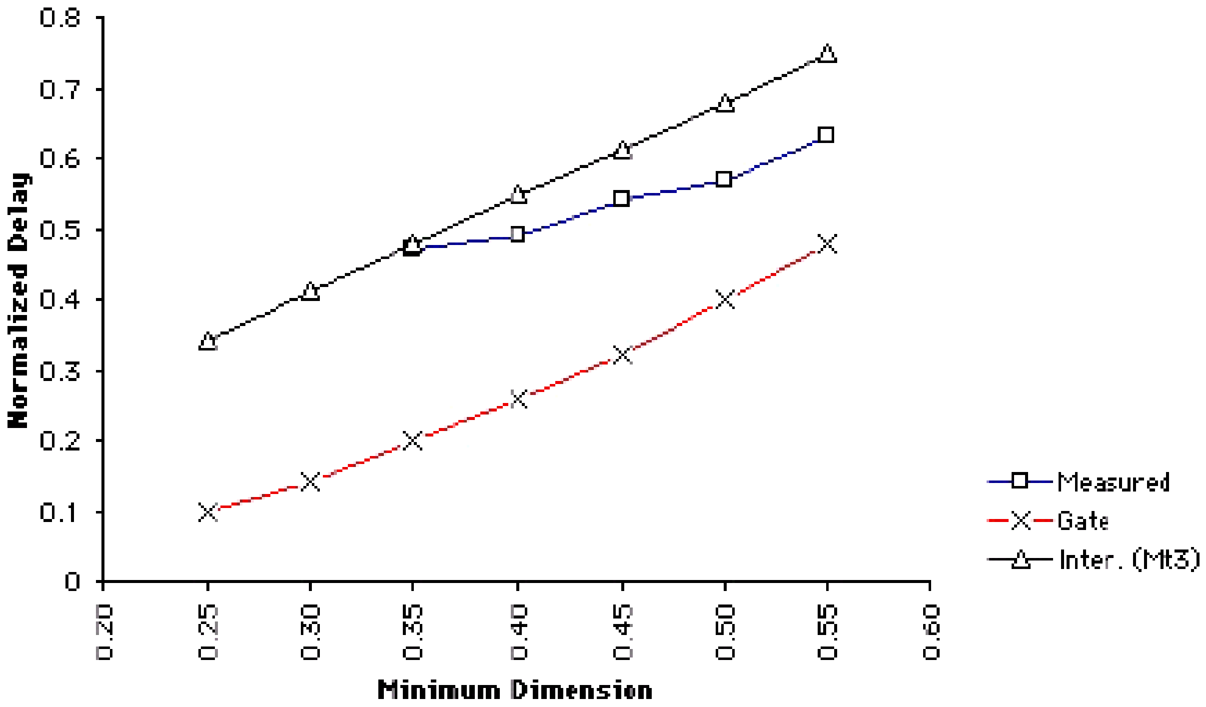

Figure 15: Circuit Delay

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Final Verification

- Run DRC
- Run LVS
- Clock Skew

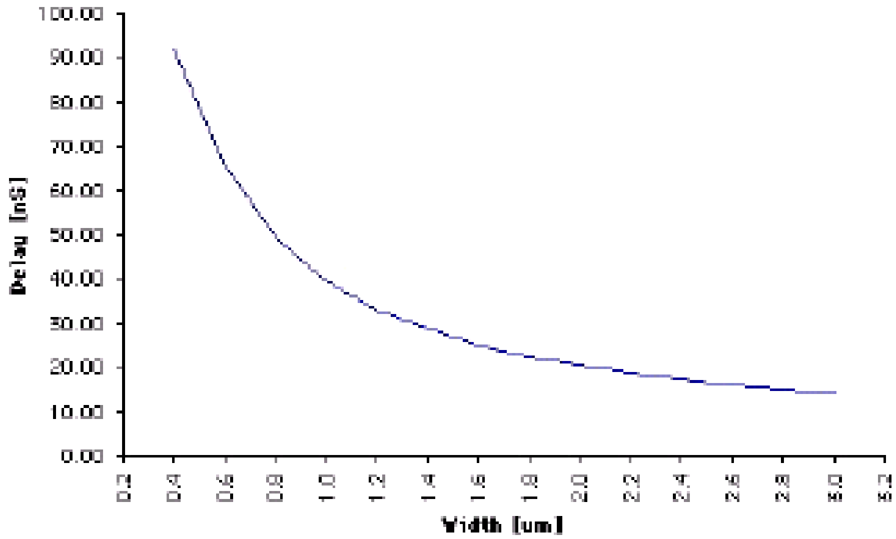

Figure 16: Clock Line Delay

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Conclusion

- Advantage:
  - short amount of time it needs to convert the design to new technology
- Disadvantage:
  - scaling to 0.35 micron instead of 0.25 micron
  - increase power and area compared to the ideal conversion
  - the design is limited to the same number of layers as the original one
- A good use of the method
  - scaling standard cell libraries

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Thanks!

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