A 900 MHz CMOS Wide Tuning Range Voltage-Controlled Ring Oscillator

Fang Fang, Zhi-Gong Wang

Abstract: The paper presents a 900MHz voltage controlled ring oscillator implemented in a standard 0.35 μm CMOS technology. The VCO has a wide operating frequency range from 184MHz to 1.422GHz with an average VCO gain (K_{vco}) of 0.77GHz/V. At 984MHz, the phase noise of single ended signal is −87.7 dBc/ Hz at 100 kHz frequency offset. The chip area is 0.16mm^2. The VCO core consumes about 2.44mW from a 3.3 V supply.

Key words: oscillators, VCO, ring oscillators, voltage-controlled oscillators, phase noise, RF circuit.

1.Introduction

The explosive growth in mobile communications has driven the need for integrated low power frequency synthesizers that provide precise reference frequencies for modulation and demodulation of RF signals. For system on chip solutions, integrated CMOS frequency synthesizers offer the advantage of high speed, low power and low cost. Because of the increased interests in fully integrated CMOS frequency synthesizer, voltage-controlled oscillator, which is one of its key building blocks, has become an active research area.

In recent years, integrated LC oscillator has been commonly used due to its good phase noise performance. However, the phase noise depends on the quality of the inductor. As it is very difficult to construct high-Q (>10) on-chip inductors in today's CMOS technology, low phase noise is not guaranteed for integrated CMOS LC oscillators. A second concern stems from the fact that process variations may significantly shift the center frequency of a VCO. Wide tuning range is therefore desired to compensate such kind of frequency offset. Due to the narrow tuning range of the varactor, which is routinely used as the tuning element, typical tuning range of an LC-tank VCO is limited to10-20%. In some cases, it becomes extremely difficult, if not impossible, to tune the VCO to the right working frequency[1]. Finally, on-chip inductor occupies a lot of chip area, which is undesirable for cost considerations.

On the other hand, ring oscillators do not need any on-chip inductors and can be easily implemented. It occupies a much smaller chip area than LC-tank VCO. Moreover, ring oscillators have a wide tuning range, which makes it easier for designers to tune the center frequency accurately in spite of process variations.

2. Circuit Structure

A ring oscillator is a closed-loop chain of identical inverters (or amplifiers), as shown in Fig.1 with a negative DC feedback to provide oscillation.

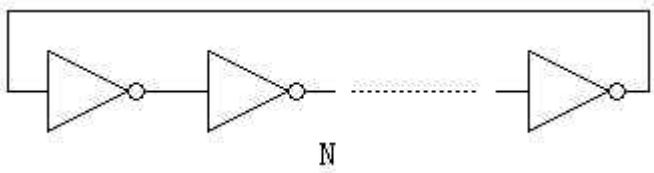

Fig. 1 Ring Oscillators

The gain stages in a ring oscillator can be realized in various forms. A commonly used form is the CMOS inverter (shown in Fig.2 (a)) that is often implemented to monitor the gate delay in a specific process. However, as

the output swing of an inverter goes all the way from Vdd to ground, it suffers from power supply and substrate coupled noise when the oscillator is implemented on the same silicon substrate with digital circuits. As a result, fully differential oscillators are preferred when phase noise is a critical specification.

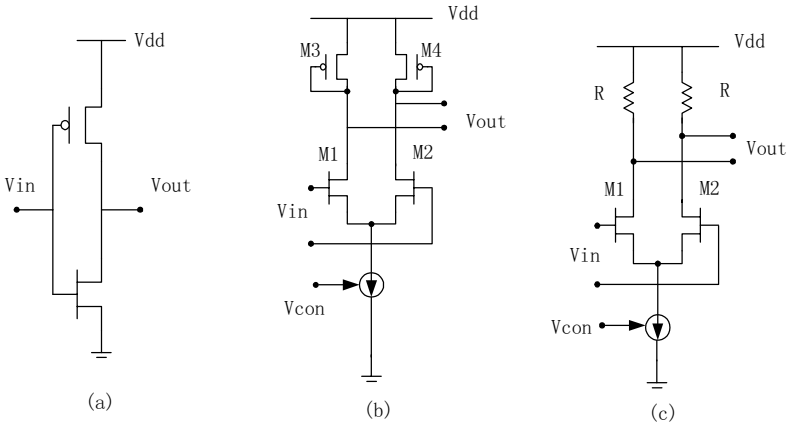

Fig. 2 Simple gain stages

Fig.2 (b) and Fig.2 (c) show two simple differential stages. The frequency of oscillators with such differential buffer stages can be approximately expressed by[2]

$$f = \frac{I_{dd}}{2NC_L V_s} \tag{1}$$

where N is the number of stages, I_{dd} is the tail current of the differential pair, $C_L$is the total load capacitance and V_s is the maximum single-ended voltage swing. The frequency can be adjusted by tuning I_{dd}, which is controlled by V_{con}. Fig.2 (b) is a differential stage with diode-connected pMOS loads. Considering the body effect of CMOS transistors, the voltage gain of the stage is

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_3}}\frac{1}{1+\eta} \tag{2}$$

Where $\eta=g_{mb3}/g_{m1}$, g_{m1} and g_{mb3} are the gate and body transconductances of transistors M1 and M3, respectively. If the variation of η with the output voltage is neglected, the gain is independent of the bias current and voltages (so long as M1 and M2 stay in saturation). Thus, V_{con} can vary in a wide range while providing enough voltage gain to ensure oscillation. So a wide tuning range can be achieved with this circuit strcture. The gain of the diffenential pair with resistive load (as shown in Fig.2 (c)) is approximately expressed by

$$A_v = -g_m R \tag{3}$$

where the value of g_m drops as V_{con} decreases. If V_{con} is below a certain level, A_v will be too small to sustain oscillation. Generally, this structure offers a narrower tuning range than the one with diode-connected load if they are of the same size. Moreover, the resistor value varies considerably from run to run, which causes discrepancies in the oscillation frequency.

3. Phase Noise

The Hajimiri phase noise model predicts the upconversion of thermal and 1/f device noise into close-in phase noise using the impulse sensitivity function (ISF) [3] ISF accounts for the time-variant sensitivity of an

oscillator's output to its noise sources and is a function of waveform. According to this theory, the single sideband phase noise is given by

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{\frac{\bar{i}_n^2}{\Delta f}\Gamma_{rms}^2}{8q_{\max}^2 \Delta\omega^2} \right) \quad (4)$$

where $\bar{i}_n^2 / \Delta f$ is the total noise contribution from all sources at the output node, Γ_{rms} is the rms value of the ISF function and q_{max} is the maximum charge displacement across the load capacitance. The $1/f^3$ corner frequency is given by

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \quad (5)$$

Where Γ_{dc} is the DC value of ISF function and $f_{1/f}$ is the 1/f corner frequency of the device. Equation (5) shows that it is desirable to minimize the DC value of the ISF in order to reduce phase noise in the $1/f^3$ region. As Γ_{dc} is closely related to certain symmetry properties of the oscillation waveform, the waveform should be optimized to have symmetrical rising and falling time.

Taking the differential pair shown in Fig.2 (b) as the gain stage, we designed a five-stage ring VCO. Fig.3 shows the transient simulation result of the output. The waveform exhibits approximately equal rising and falling time, which suggests that the upconversion of low frequency noise can be reduced.

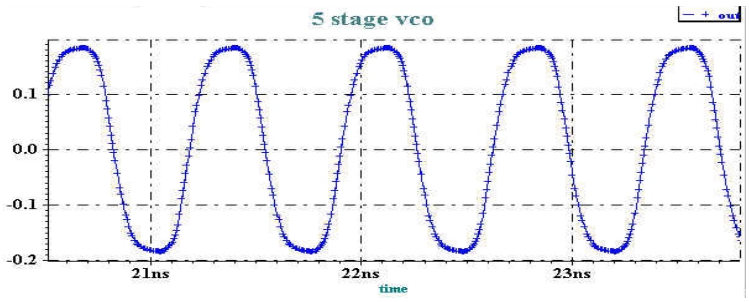

Fig. 3 Transient simulation result of VCO

4. Simulation and Measurement Results

The circuit is simulated using SmartSpice™ of Silvaco. The chip is fabricated in TMSC 0.35μm CMOS process via MOSIS. Fig.4 shows the photo of the chip. The area is 0.16mm^2.

The circuit is designed to operate under 3.3V power supply. The measured and simulated oscillating frequencies are plotted against the control voltage in Fig.5. The chip turns out to have a wide tuning range from 184MHz to 1.422GHz as the control voltage changes from 1.7V to 3.3V.

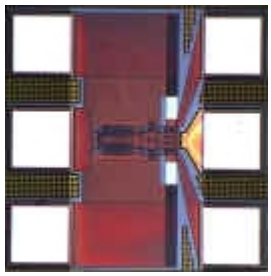

Fig. 4 Microphotograph of VCO: differential delay buffer cell with diode-connected loads

The parasitic capacitance on the key node of the circuit has significant effects on the oscillating frequency as can been seen from equation (1). These parasitics have been extracted from the layout and backannotate to the netlist for an accurate simulation. The measurement shows good agreement with the simulation.

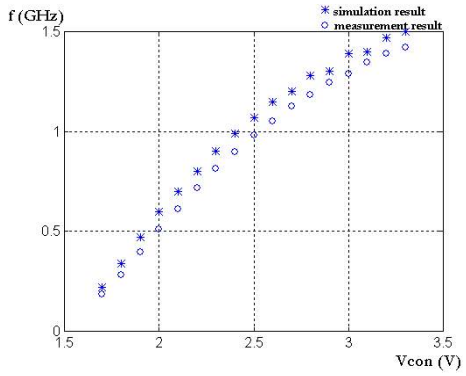

Fig. 5 Oscillating frequency vs Controlled Voltage

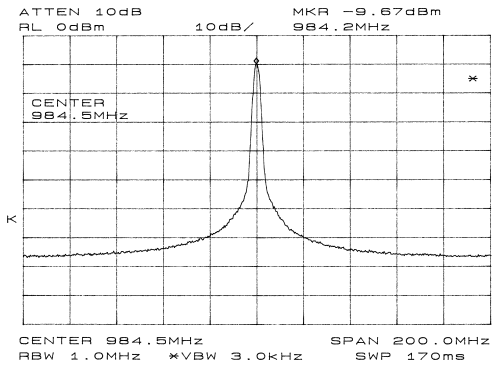

Fig. 6 The frequency spectrum of single ended output

Fig.6 shows the frequency spectrum of a single ended output. At 984 MHz the phase noise is –87.7 dBc/Hz at 100 kHz offset. Limited by test facilities, phase noise measurement can only be done for single-ended signals. The phase noise performance of the differential output is expected to be better than this figure because the differential structure has good rejection of supply and substrate noise. The power consumption of the chip is lower than 28.8mW while most power is consumed by buffers designed to drive the 50 Ω load. The VCO core without driving buffers has a low power consumption of about 2.44mW.

5. Conclusion

A 900MHz 3.3V five-stage CMOS ring VCO is implemented in a 0.35μm CMOS process. A wide tuning range is obtained using the differential structure with diode-connected load. Good phase noise performance is achieved by optimizing the rising and falling time of the oscillating waveform.

6. Acknowledgments

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7. References

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