Alpha Power Law Model and Its Application on Delay Analysis for Series-Connect MOSFETs

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Part I

- *Motivation*
- Previous work: Classical Manual Analysis Model
- Alpha-Power Law Model
- Application on Series-Connect MOSFETs
- Conclusion

Device Model

- Manual Analysis
  - Level 1: square law long channel model
- Models for CAD Tools
  - Level 2: geometry based. less accurate than level 3 and 4
  - Level 3: semi-empirical
  - Level 4: BSIM(Berkeley Short Channel IGFET Model). Based on experiment. Most popular spice model
  - Other Models: from SPICE vendor or semiconductor manufacturers
- This talk focuses on a special field: model for timing analysis: especially on SCMs with DSM technology.

All models in this presentation are for common digital circuits, not for RF circuits. BSIM models are not verified for frequency above 500MHz.

  

Demand for Model from Timing Analysis

- Simple: level 3 and 4 are too complex and require to integration and differentiation
- Accurate: level 1 doesn't consider short channel effect
- However, they are still useful
  - Need to compare our model with Spice simulation(BSIM) to test accuracy
  - Manual analysis model provides insight into the device.
  - Improve manual analysis model: including short channel effects proves to be feasible

Part II

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Long Channel Sqaure Law Model

- Also called Shichman-Hodges model

$$I_D = \begin{cases} \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS}) & V_{DS} > V_{GS}-V_T \\ \mu C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right] & V_{DS} < V_{GS}-V_T \\ 0 & V_{GS} < V_T \end{cases}$$

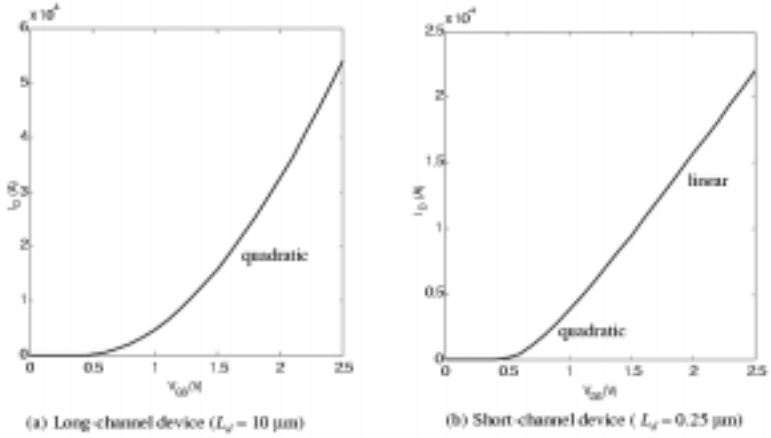
  with $V_T = V_{T0} + \gamma(\sqrt{-2\phi_F - V_{SB}} - \sqrt{-2\phi_F})$ for body effect

- Linear Region: $I_{DS} \propto V_{DS}$
- Saturation Region: $I_{DS} \propto V_{GS}^2$

Short Channel Effects

- Threshold deviation
- DIBL: Drain induced barrier lowering
- Mobility degradation
- Velocity saturation

Short Channel Effects: I_{DS} vs. V_{GS}



(a) Long-channel device (L_g = 10 μm) (b) Short-channel device (L_g = 0.25 μm)

Figure 1: I_D and V_{GS} relations in long and short channel transistors

Velocity Saturation Effect

- Electrical field strength can easily reach the level $\xi_C = 10^6 V/m$, making velocity of carrier saturate
- If $\xi > \xi_C$, the electrons will collide with each other: scattering effect.

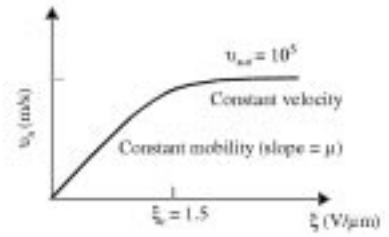


Figure 3: Relations between Electron Velocity and Electrical Field

Threshold Variation in Short Channel Device

- In short channel devices, the channel length and depletion region length is comparable. Increase Vd will enlarge the depletion region of drain junction.

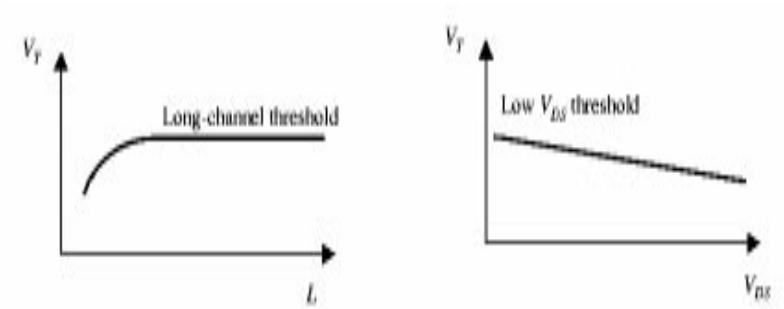


Figure 2: Threshold's Relation with(left) Length and DIBL(right)

Mobility Degradation

- In long channel devices, mobility is a constant or say velocity is proportional to electrical field

$$\upsilon = \mu\xi$$

- In short channel devices, above relation does not hold any more. Mobility μ decreases with increase of V_{GS}
- Mobility degradation differs from velocity saturation in that V_{GS} is perpendicular to the direction of I, V_{GS} tends to pull the electron to the surface and reduce surface mobility.

Impact and Ways Out

- I_D displays a linear relation with V_{GS} and such that it does not suffer so much from decreasing V_{DD}
- V_{DSAT} is smaller than $V_{GS} - V_T$. There are some different ways addressing this problem.
- Short channel devices are more likely to work under saturated region.
- SCM structure can alleviate this problem since the series connected transistors' V_{DS} share the V_{DD}.

Part IV

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- Previous work: Classical Manual Analysis Model
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Alpha-Power Law Model

- "Alpha-Power Law MOSFET Model and its Application to CMOS Inverter Delay and Other Formulas", Takayasu Sakurai and Richard Newton, IEEE Journal of Solid-State Circuits, April 1990
- "A Simple MOSFET Model for Circuit Analysis ", Takayasu Sakurai and Richard Newton, IEEE Transactions on Electron Devices, April 1991
- "Delay Analysis of Series-Connected MOSFET Circuits", Takayasu Sakurai and Richard Newton, IEEE Journal of Solid-State Circuits, February 1991

Short-Channel MOSFET Model

$$\begin{cases} V_{TH} = V_{T0} - \gamma V_{BS} & \\ V_{DSAT} = K(V_{GS} - V_{TH})^m & \\ I_D = I_{DSAT} = \frac{W_{EFF}}{L_{EFF}} B (V_{GS} - V_{TH})^n & \text{if} \quad V_{DS} \geq V_{DSAT} \\ I_D = I_{DSAT}(2 - \frac{V_{DS}}{V_{DSAT}}) \frac{V_{DS}}{V_{DSAT}} & \text{if} \quad V_{DS} < V_{DSAT} \\ I_D = 0 & \text{if} \quad V_{GS} < V_{TH} \end{cases}$$

Some Points from Short Channel Model

- $V_{TH} = V_{T0} - \gamma V_{BS}$ is accurate enough to capture the body effect while making a linear relation between V_{BS} and threshold. Body effect is more prevalent in SCM than in an inverter.
- K and m are combined to describe that threshold voltage is affected by the ratio of depletion region width to channel length and V_{DS}.
- n is to address the carrier velocity saturation effect. The value of n for NMOS with $1\mu m$ technology is 1.2, and for $0.5\mu m$ technology it is 1. n usually comes from curve fitting.
- If assign m and K to 1, n to 2, respectively, the short channel model reduces to long channel model. So actually short channel model factorizes some constant in long channel model.

Part V

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Critical Transient Time

- Usually gate delay can be expressed as

$$t_T = k_1 t_{in} + k_2 C_O$$

- Define a critical input transition time t_{T0}:

$$t_{T0} = \frac{C_O V_{DD}}{2 I_{D0}} \frac{(n+1)(1-v_T)^n}{(1-v_T)^{n+1} - (u_V - v_T)^{n+1}}$$

  the delay behaves differently with input transient above or below t_{T0}. If $t_{in} > t_{T0}$, input transient plays a more important role.

- I_{D0} is observed when $V_{DS} = V_{GS} = V_{DD}$. V_{D0} is defined as the saturation voltage when $V_{GS} = V_{DD}$.
- v_T is defined as V_{T0}/V_{DD}. $v_V = V_{INV}/V_{DD}$, logic threshold voltage is the gate input voltage, which makes the output voltage equal to half V_{DD}

Delay Formula

- As last slide, there are two cases
  - if $t_T \le t_{T0}$, fast input

$$\begin{cases} t_d = t_T \left[\frac{1}{2} - \frac{1-v_T}{n+1} + \frac{(v_V - v_T)^{n+1}}{(n+1)(1-v_T)^n} \right] + \frac{C_O V_{DD}}{I_{D0}} \\ t_{TOUT} = \frac{C_O V_{DD}}{0.7 I_{D0}} \frac{4 v_{D0}^2}{(4 v_{D0} - 1)} \end{cases}$$

  - if $t_T \ge t_{T0}$, slow input

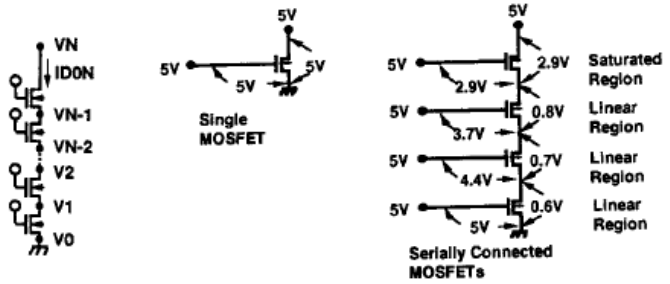
$$\begin{cases} t_d = t_T \left[v_T - \frac{1}{2} + \left\{ (v_V - v_T)^{n+1} + \frac{(n+1)(1-v_T)^n}{2 t_T I_{D0} / C_O V_{DD}} \right\}^{1/n+1} \right] \\ t_{TOUT} = \frac{C_O V_{DD}}{0.7 I_{D0}} \left(\frac{1-v_T}{t_d/t_T + 1/2 - v_T} \right)^n \end{cases}$$

Delay Formula Continue

- $v_{D0} = V_{D0}/V_{DD}$ in delay formula. V_{D0}, I_{D0} and logic threshold V_{INV} can be derived from simulation. n is critical.
- Application of the delay formula displays noticeable advantage of short channel devices than the long channel devices
- t_{OUT} is output transient time. It can be used to calculate the input transient of next stage.

Delay Degradation Factor II

- In SCM as the figure below, except the transistor at top, all others are working in linear region.



Delay Degradation Factor

- Define delay degradation factor as the ratio of the delay of SCM to the delay of a single MOSFET:
- For step input, or, when large output capacitance dominates t_d, F_D can be calculated from I_{D0}/I_{D0N}, there is:

$$\begin{aligned} F_D &= \frac{\text{delay(SCMS)}}{\text{delay(inverter)}} \\ &= 1 + \frac{1}{2}\frac{v_{D0}}{1-v_T}(1+\gamma)(N-1)n \end{aligned}$$

- F_D is always larger than one, but we hope it is as small as possible

Part VI

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Delay Degradation Factor III

- If plug in the long channel parameters and do not consider body effect, we can get these relations:

$$I_{D0} = NI_{D0N} \quad \text{or} \quad F_D = N$$

  so there is no improvement in terms of delay
- However, for short channel devices, n and v_{D0} is much smaller. F_D can approach $N/2$. This is because SCM structure mitigate the velocity saturation problem born with short channel devices. Although SCM suffers from body effect, SCM structure is still favorable for DSM technology

Conclusion

- A close form formula for delay calculation is derived based on short channel device model
- Apply this formula on SCM to get the conclusion that SCM has better delay performance in DSM region.
- Velocity saturation effect may request to reconsider some design/optimization criteria with DSM technology