Use Asymptotic Waveform Evaluation Methos on Transistor-Level Timing Analysis

Zhong Wang

Electrical and Computer Engineering University of Toronto

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zwang@eecg.toronto.edu
http://www.eecg.toronto.edu/~zwang

Synthesis Reading Group

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Outline

- Motivation
- Previous work
- Problems of Spice
- AWE(Asymptotic Waveform Evaluation
- Results



Importance of and Problem with Timing Analysis

- Importance: Determine how fast a circuit can run
 - Setup time, hold time of FF
 - Clock Frequency

Problem

- With shrinking Lambda, interconnect delay becomes the dominant factor rather than transistors
- Parasitic and coupling effect(cross talk) kick in



Trend in Technology I

- Decreased Feature Size
- Decreased Voltage
- $\blacksquare Al \Longrightarrow Cu$
- Increased Clock Frequency
- Improved Physical Structure





Trend in Technology II

Depend on whether scale voltage, there is full scaling(scale all by a factor of S, S > 1) and fixed-voltage scaling(only scale geometries but not voltage). There is

Table 1: Scaling Scenarios for Short-Channel Devices

Parameter	Full Scaling	Fixed-Voltage Scaling
W, L, t_{ox}	1/S	1/ <i>S</i>
VDD, V_T	1/k	1
Area	$1/S^{2}$	$1/S^{2}$
C[ox]	S	S
C_{gate}	1/S	1/S
k_n, k_p	S	S
IntrinsicDelay	1/S	1/S

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Probelm of Spice in timing analysis

- Prohibitive Long Run Time
- Dynamic Timing Analysis: Need Test Pattern
- Accurate Spice of DSM technology
- We need an embedded timing analysis engine



Static and Dynamic Timing Analysis

Static

- No Test Pattern
- Fix Critical Path
- Pros: Fast.
- Cons: Could be less accurate than Dynamic if models are not good.

Dynamic

- Require Test Pattern
- Analysis Result Has Dependency on Tets Pattern used
- Pros: Accurate; Can target specific test pattern
- Cons: Need to generate enough test patterns and possibly large run time to get accurate result. Hard if there are a large number of inputs

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Approach

Model the whole circuit as a RC tree(an acyclic network)

Extract circuit to blocks(gates) connected by interconnects.

 $Delay = F(input_slope, output_load)$





Time Domain to Frequency Domain

from Teveqnif Theory



Moment Matching

• Moment is defined as



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Back to Time Domain

Get the time domain waveform



MATLAB Simulation

From MATLAB simulation results



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Hurdles

Extraction of DSM technology



Problem with AWE

poles at right hand side



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FEM method in layout extraction



Data Flow

