Jin Hee Kim

1705 – 386 Yonge St., Toronto, ON M5B 0A5
(647) 607 - 0115 |kimjin14@ece.utoronto.ca

PERSONAL STATEMENT

I am a graduate student researching in the field of reconfigurable computing devices. Specifically, my research focus is to study the architecture to maximize the utilization of field programmable gate arrays (FPGAs) to achieve the high efficiency designs. I am interested in investigating how these devices can be used to accelerate various applications, such as very low precision convolutional neural networks (CNNs).

EDUCATION

University of Toronto
Doctor of Philosophy in Computer Engineering **Sep 2015 – Present**

- Advisor: Jason H. Anderson

University of Toronto
Master of Applied Science in Computer Engineering **Sep 2013 – Jan 2016**

- Thesis Title: Synthesizable FPGA Fabrics
- Advisor: Jason H. Anderson

University of Toronto
Bachelor of Applied Science and Engineering (Honours) in Electrical Engineering **Sep 2008 – Jun 2013**

- GPA: 3.94 out of 4.0

PEER-REVIEWED JOURNAL PUBLICATIONS

J. Kim, J.H. Anderson, “Synthesizable standard-cell FPGA fabrics targetable by the Verilog-to-Routing (VTR) CAD flow,” in the *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 10(2):11, April 2017.

PEER-REVIEWED CONFERENCE PUBLICATIONS

J. Kim, B. Grady, R. Lian, J. Brothers, J.H. Anderson, “FPGA-Based CNN Inference Accelerator Synthesized from Multi-Threaded C Software” in the *IEEE International System-on-Chip Conference (SOCC),* pp. 268–273, Munich, Germany, September 2017.

S. A. Chin, N. Sakamoto, A. Rui, J. Zhao, **J. Kim**, Y. Hara-Azumi, J.H. Anderson, "CGRA-ME: A unified framework for CGRA modelling and exploration." In the *IEEE International Conference on Application-specific Systems,* 2017.

J. Kim, J. H. Anderson, “Synthesizable FPGA fabrics targetable by the Verilog-to-Routing (VTR) CAD flow,” in the *IEEE International Conference on Field Programmable Logic and Applications (FPL),* pp. 1–8, London, UK, September 2015.

L.A. Fernandes, J.R. Grenier, **J. Kim**, P.R. Herman, J.S. Aitchison, P.V.S. Marques, "Femtosecond laser direct fabrication of integrated optical wave plates in fused silica," in the *Conference on Lasers and Electro-Optics (CLEO)*, Baltimore, MD, May 2011.

INDUSTRY EXPERIENCE

Advanced Processor Lab Intern, Samsung Research America **Jun 2016 – Aug 2016**

- Used LegUp high-level synthesis (HLS) tool to synthesize a CNN accelerator
- Investigated the implementation of low precision CNN
- Implemented and tested system-level design; using an ARM processor and an FPGA
- Integrated designs on the physical FPGA board (Arria 10 Development Board)

Device Characterization and Timing Intern, Microsemi SoC **Jul 2011 – Aug 2012**

- Created HDL designs for characterization of DSP and RAM block in the FPGA using Libero
- Simulated designs in ModelSim to test for functionality
- Extended simulation to generate test vectors for a tester
- Wrote scripts to automate characterization of SRAM
- Characterized SRAM maximum frequency across temperature and voltage

RESEARCH/PROJECT EXPERIENCE

M.A.Sc Research, University of Toronto **Sep 2013 – Jan 2016**

- Established a flow to generate and synthesize FPGA
- Extended VTR (Verilog-to-Routing) tool to automatically generate synthesizable Verilog and bitstream
- Designed and completed layout of a custom FPGA-specific 16-to-1 MUX cell
- Incorporated the custom cell into the standard cell library

Final Year Design Project, University of Toronto **Sep 2012 – Apr 2013**

- Created a system to directly translate human arm movement to robotic arm movement
- Debugged the analog circuit which filtered and amplified the EMG signals
- EMG signals were translated to digital signal using thresholds and averaging method on Virtex-5 FPGA
- Using ISE and Chipscope Pro, programmed and debugged the system on the FPGA

Summer Research Student, Photonics Research Group **May - Aug 2010**

- Assisted graduate students with fabrication of optical devices in a femtosecond laser lab
- Characterized optical devices by coupling optical fibre or focused open beam to the waveguide and measuring the power losses
- Analyzed the data using python in Spyder environment and presented the graphs and microscope images to the group bi-weekly

PROFESSIONAL AFFILIATIONS AND ACTIVITIES

Volunteer Coordinator, International Solid-State Circuit Conference, IEEE **Sep 2014 - Present**

- Interviewed and selected a group of 16 graduate students for volunteer positions
- Trained and assisted the student volunteer group to coordinate conference presentations
- Assisted in registration of presenters and committee members
- Advised the session chairs and presenters how to use the A/V equipment

Teaching Assistant, University of Toronto **Sep 2013 - Present**

- ECE241 (Digital Systems): introduced Verilog to students using DE2 board
- ECE297 (Communication and Design): mentored 5 groups of students in their software engineering projects to create an interactive mapping tool

GRADUATE COURSES

Algorithms and Data Structures (ECE1762)	Dec 2013
CAD for Digital Circuit Synthesis and Layout (ECE1387)	Dec 2013
Reconfigurable Computing and FPGA Architecture (ECE1756)	Apr 2014
Introduction to Machine Learning (CSC2515)	Dec 2015
Digital Design for Systems-on-Chip (ECE1373)	Apr 2016
Creative Applications for Mobile Devices (ECE1778)	Apr 2016

TECHNICAL SKILLS

Programming Languages: C, C++, Verilog, Assembly, Perl, Python (Numpy)
Applications: Synopsys Design Compiler, Synopsys Primetime, Cadence Encounter, Cadence Virtuoso, VTR (Verilog-to-Routing), Xilinx ISE, Altera Quartus II, Mentor ModelSim