



DESIGN, AUTOMATION & TEST IN EUROPE

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The European Event for Electronic
System Design & Test

Quantifying Error: Extending Static Timing Analysis with Probabilistic Transitions

Kevin E. Murray, Andrea Suardi, Vaughn Betz and George Constantinides

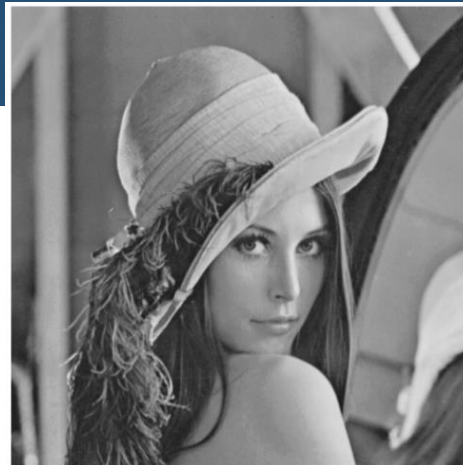


UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE
& ENGINEERING

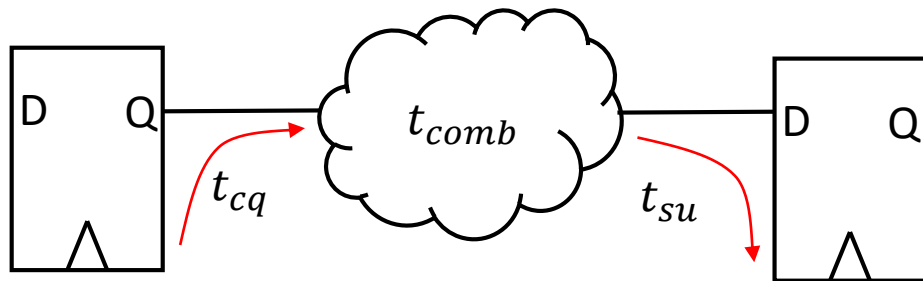
Imperial College
London

Error Tolerance

- **Error tolerant applications**
 - **Errors correctable: Iterative algorithms**
 - **Inherently noisy: Sensor readings**
 - **Errors acceptable: Image processing**



Timing Errors

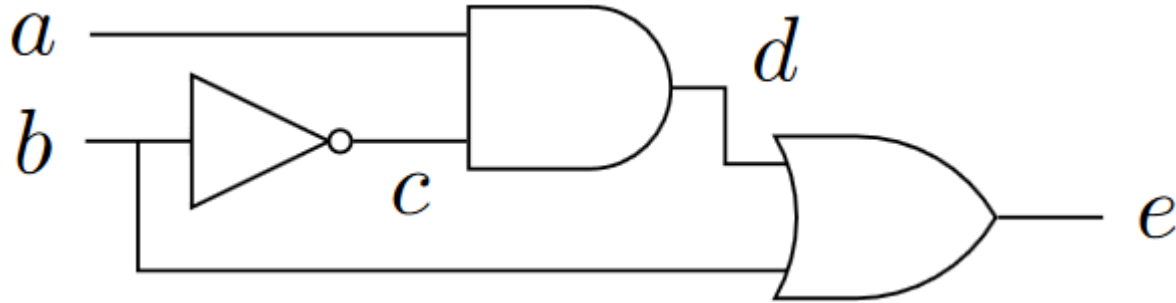


$$t_{cq} + t_{comb} + t_{su} \leq \frac{1}{f_{max}}$$

- Running system beyond f_{max} may cause errors
- But critical path not always exercised

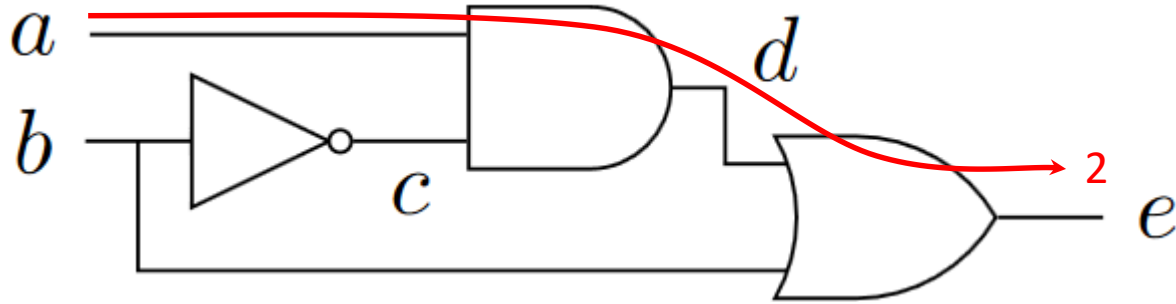
Analysis Capability Gap

- How often do timing errors occur?
 - How likely are timing paths to be exercised?



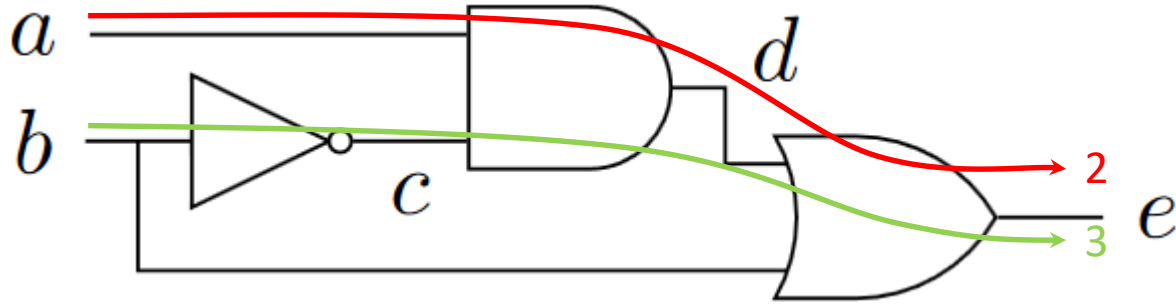
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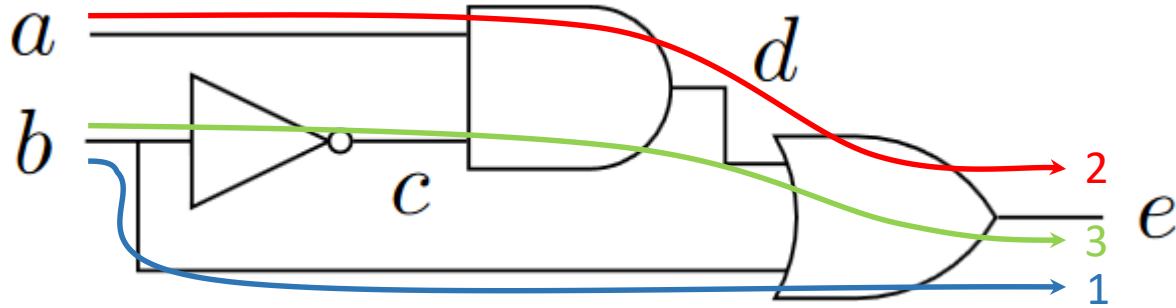
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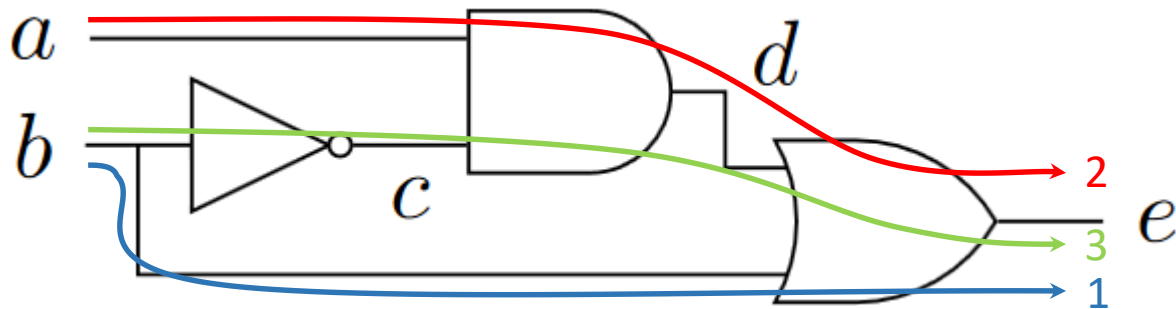
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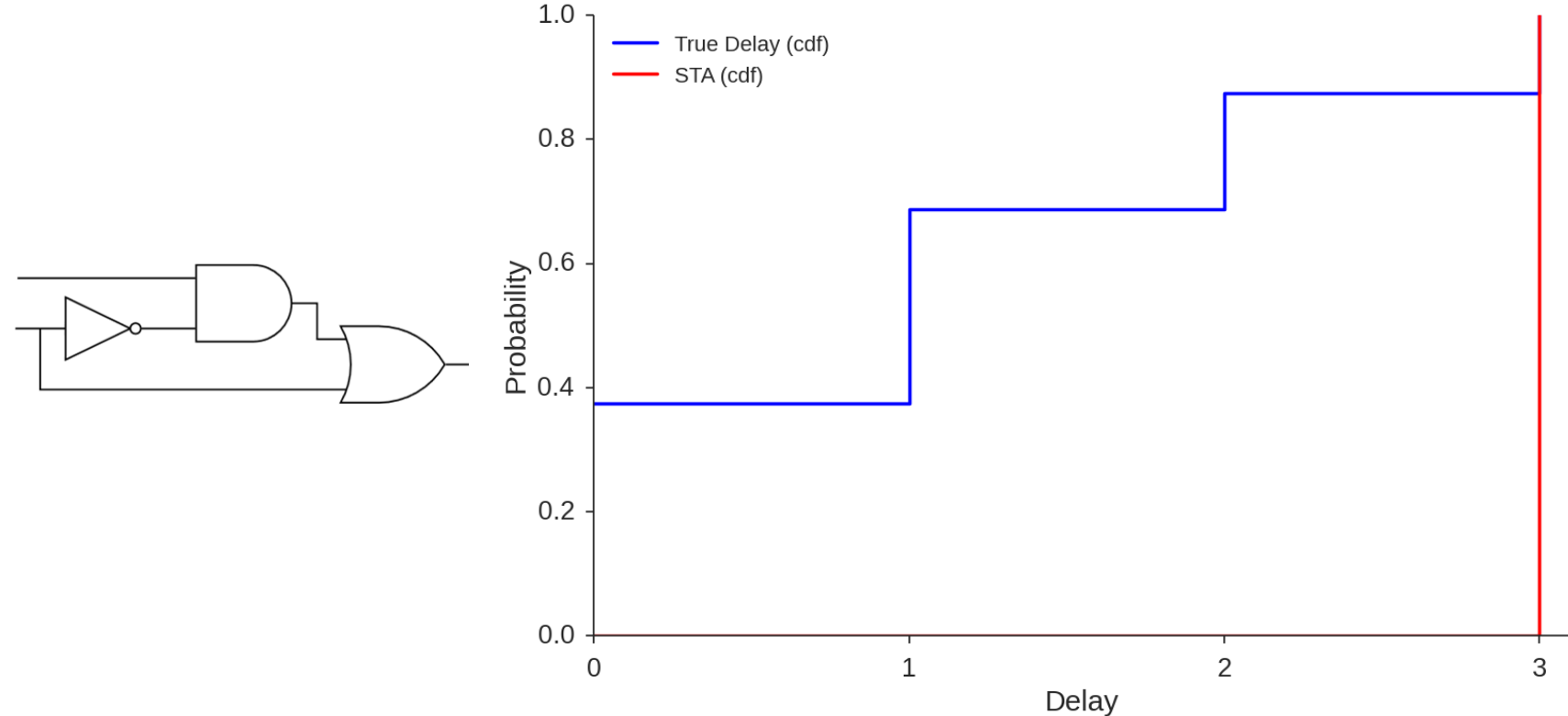
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 - How likely are timing paths to be exercised?



- Probability depends on:
 - Circuit logic
 - Input data
- Traditional Static Timing Analysis (STA) does not answer this!

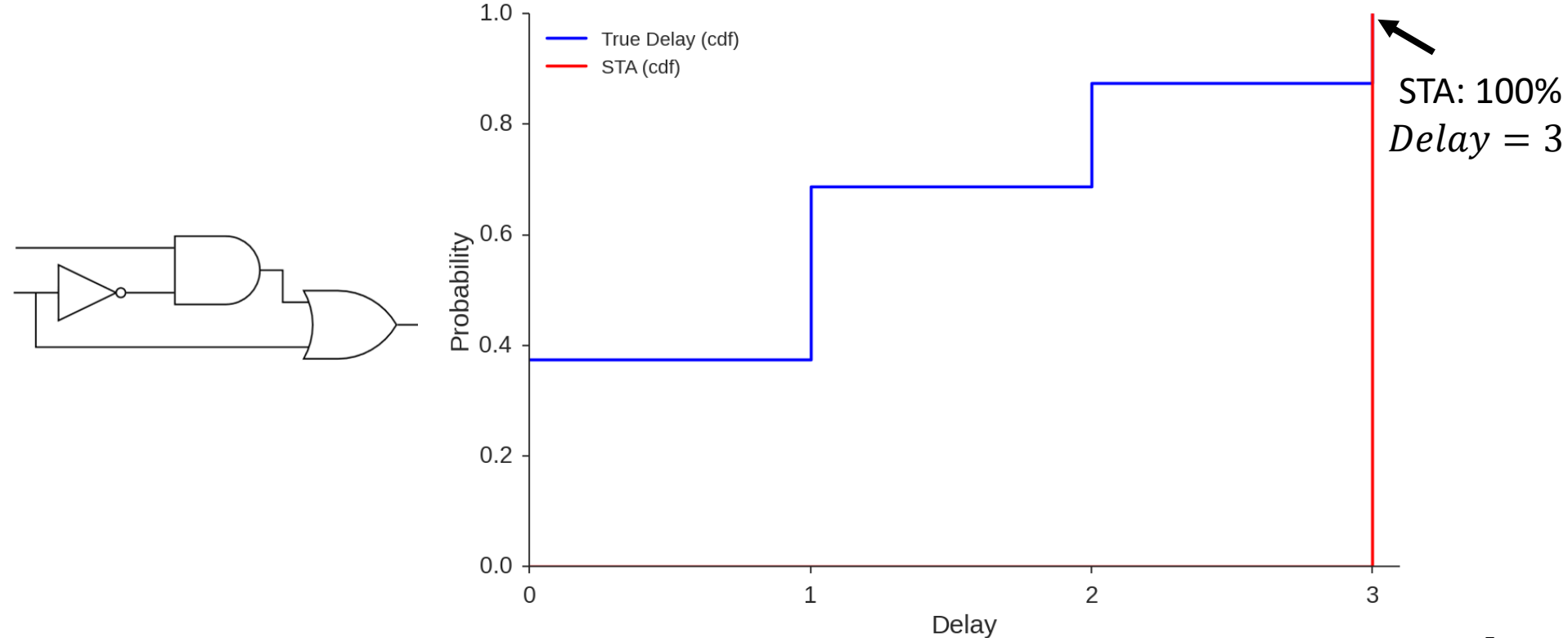
Extended Static Timing Analysis (ESTA)

- **Goal: Calculate probability timing paths are exercised**



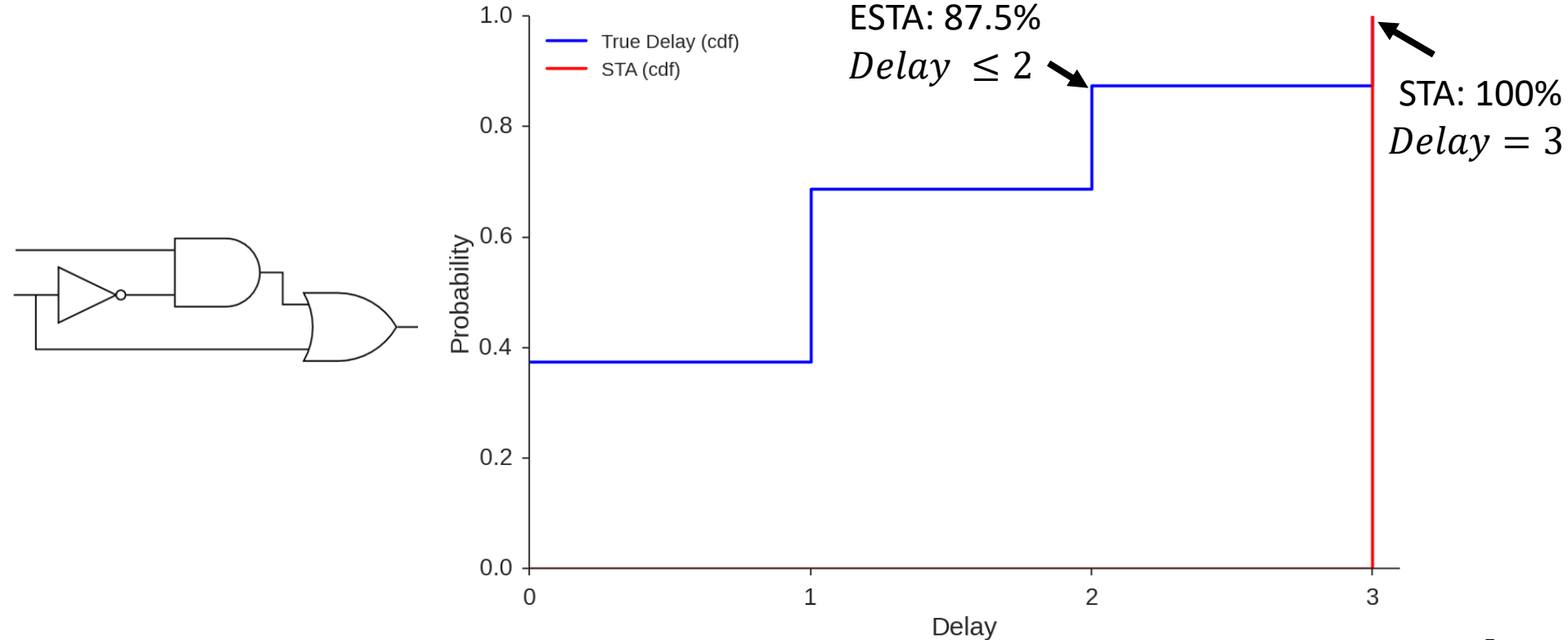
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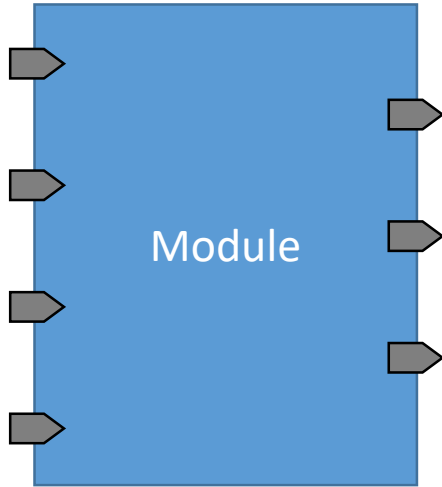


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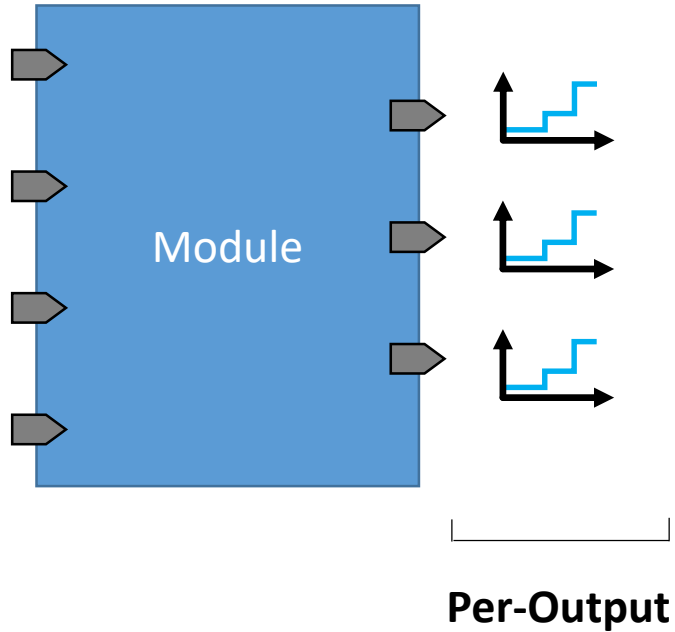
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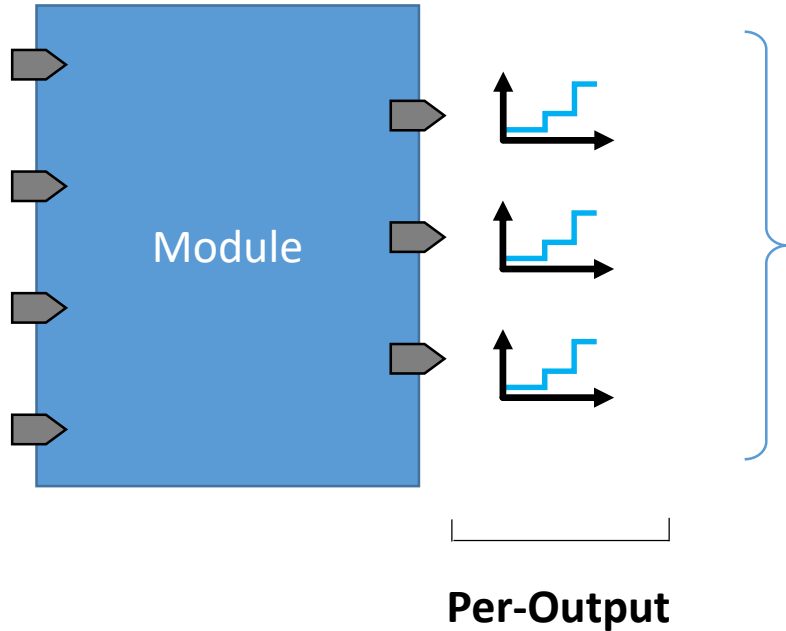
Multiple Outputs



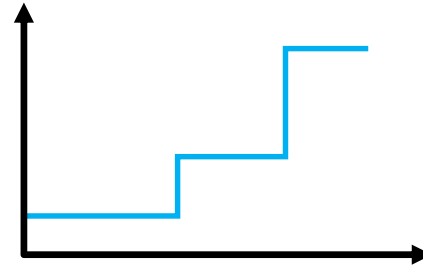
Multiple Outputs



Multiple Outputs



Maximum over all outputs



- **Composite module-level error**
 - Analogous to critical path delay

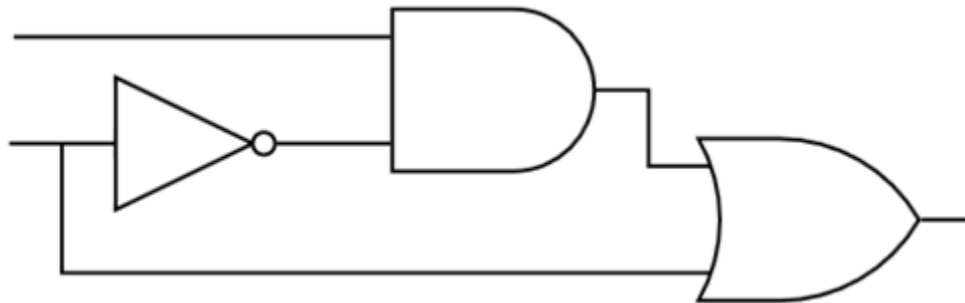
What about Statistical STA (SSTA)?

- **SSTA**

- Models *delay* uncertainty
- Still assumes all paths switch

- **ESTA**

- Models *input* uncertainty



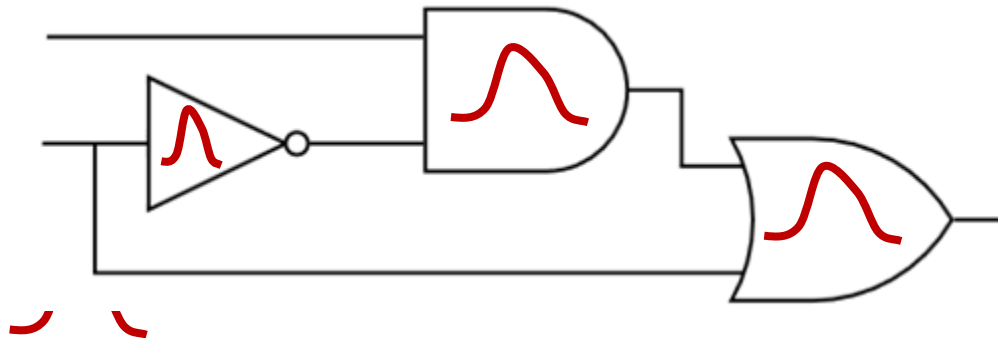
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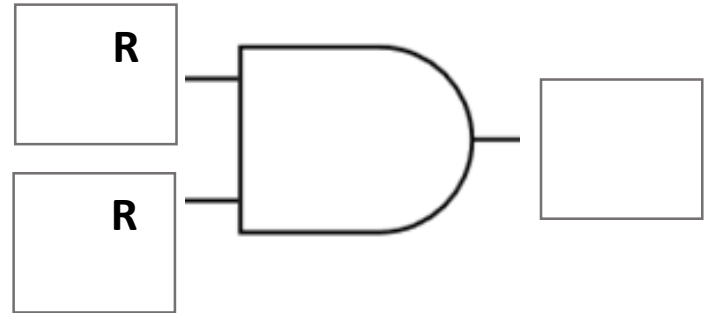
Outline

- Introduction
- **Extended STA Formulation**
- **Evaluation Framework**
- **Experimental Results**
- **Conclusion and Future Work**

ESTA Transition & Delay Modeling

- Model four transitions:

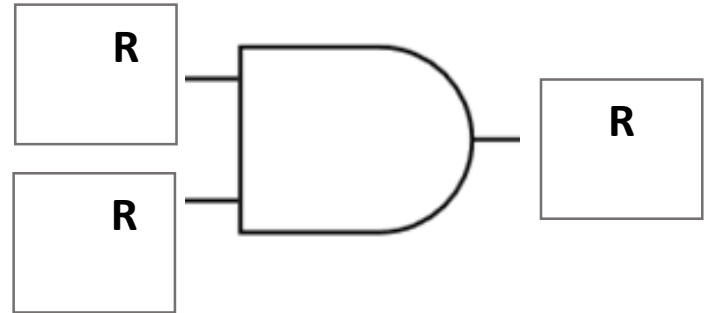
Symbol	Meaning
R	Rising
F	Falling
H	High (static)
L	Low (static)



ESTA Transition & Delay Modeling

- Model four transitions:

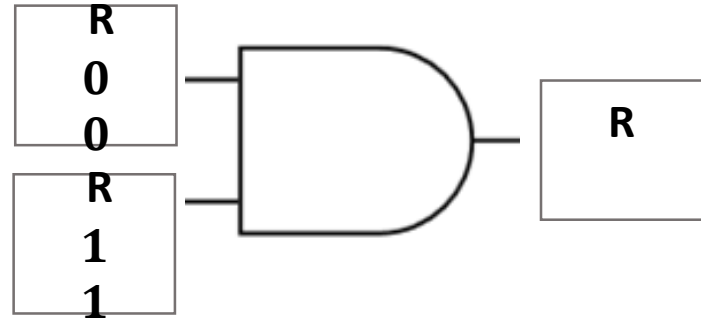
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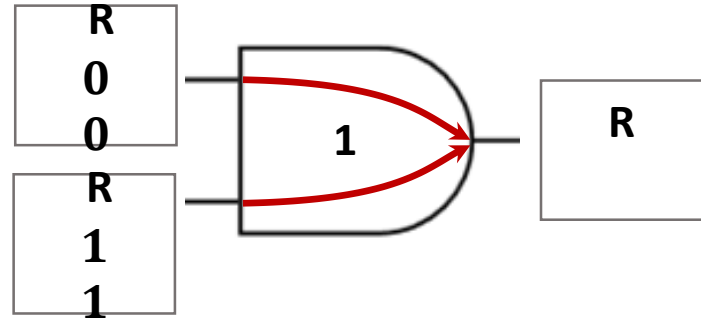
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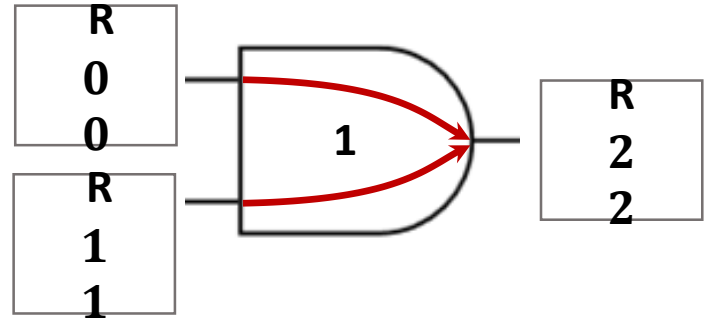
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ESTA Transition & Delay Modeling

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Symbol	Meaning
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Activation Functions

- Let $f \in \mathbb{B}^n \rightarrow \mathbb{B}$ be an *activation function*:
 - Evaluates TRUE when an event occurs
- We can combine activation functions:

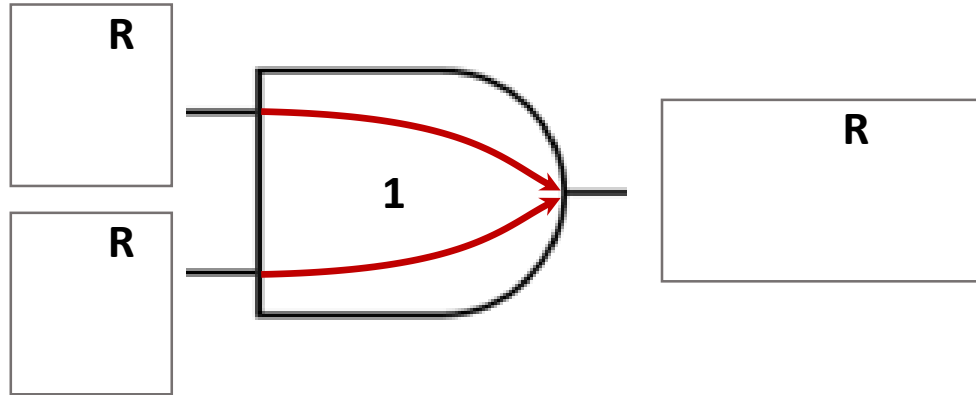
$$A, B \Rightarrow C$$

$$f_C = f_A \wedge f_B$$

Timing Tags

- Define a *timing tag* tuple:

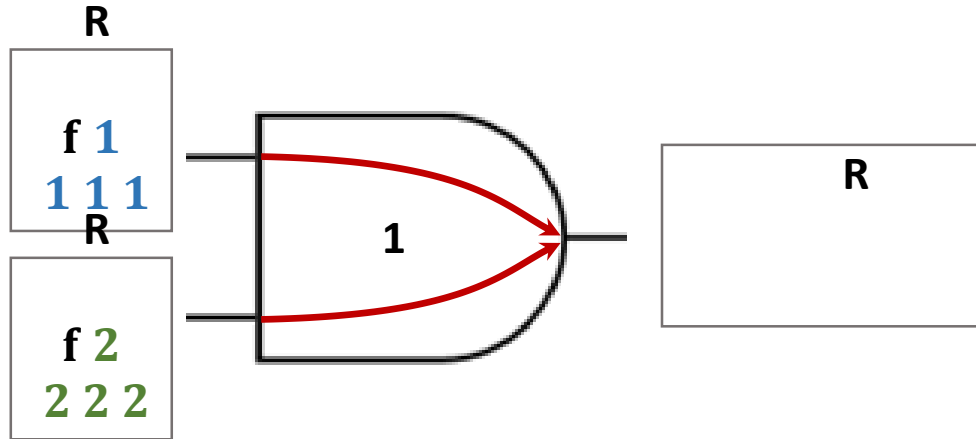
- Transition
- Delay
- Activation Function



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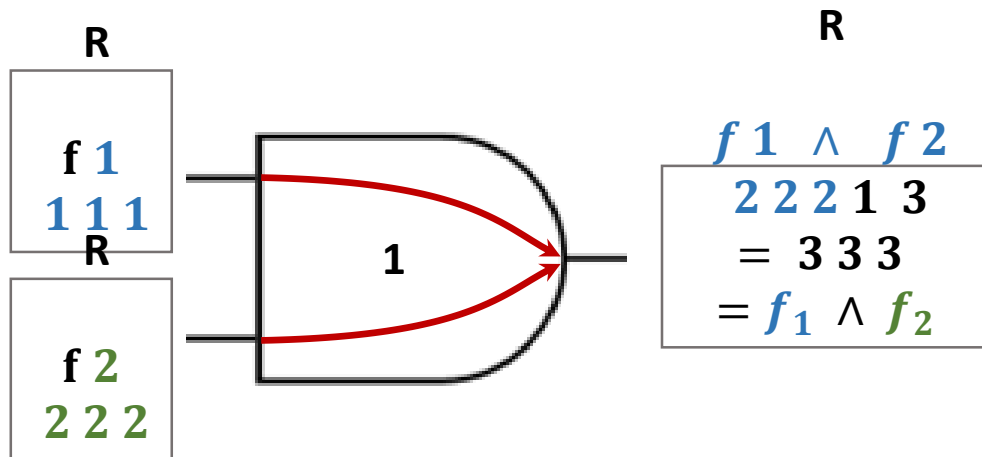
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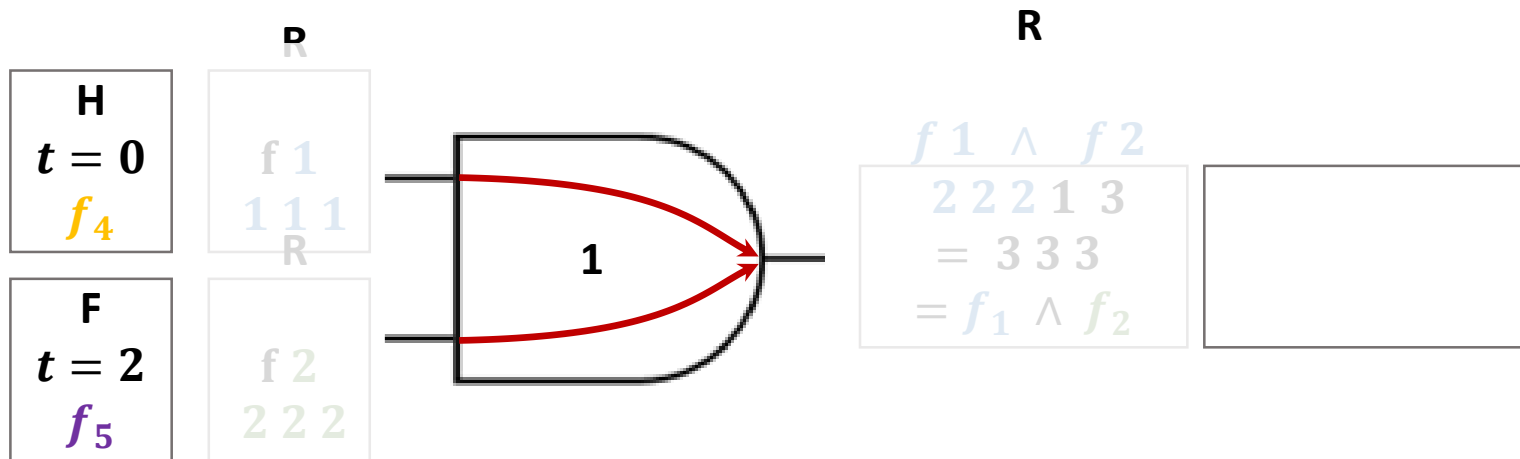
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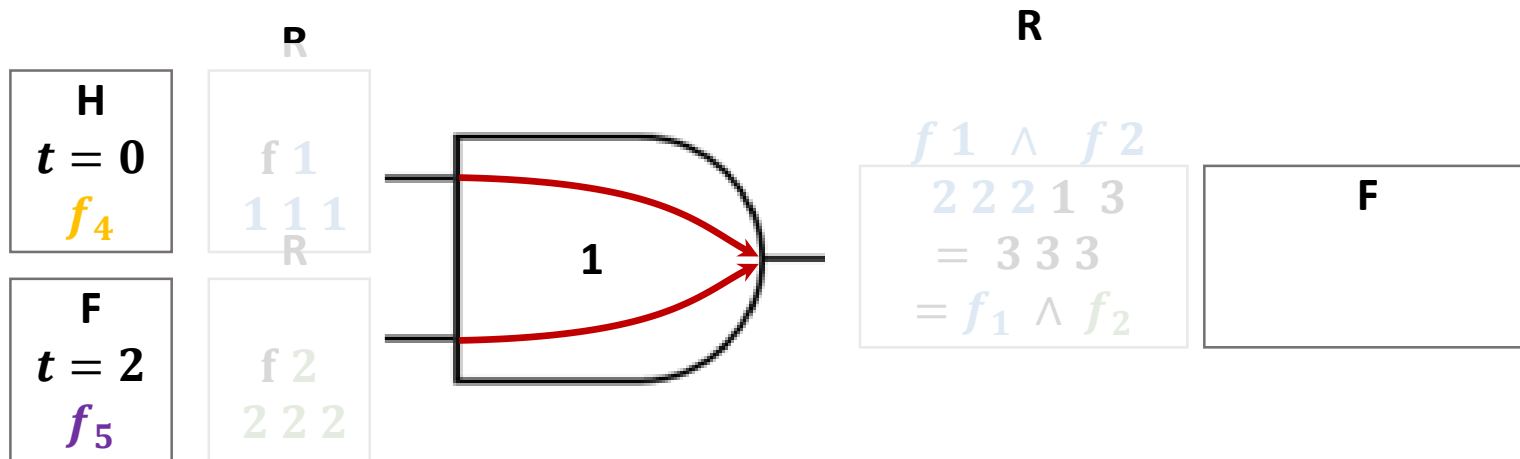
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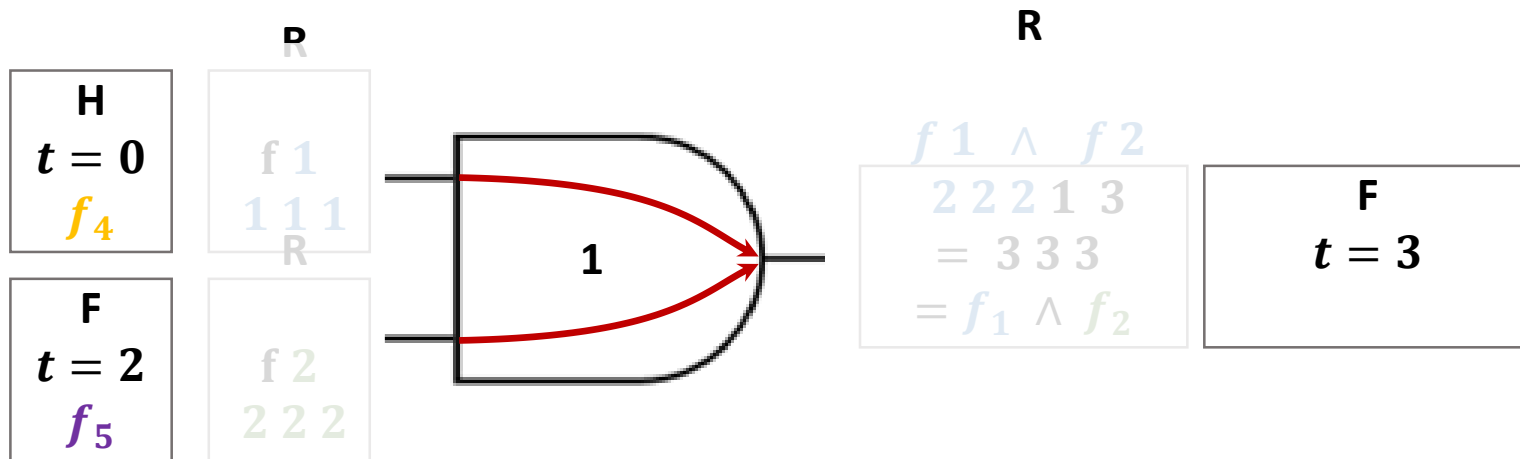
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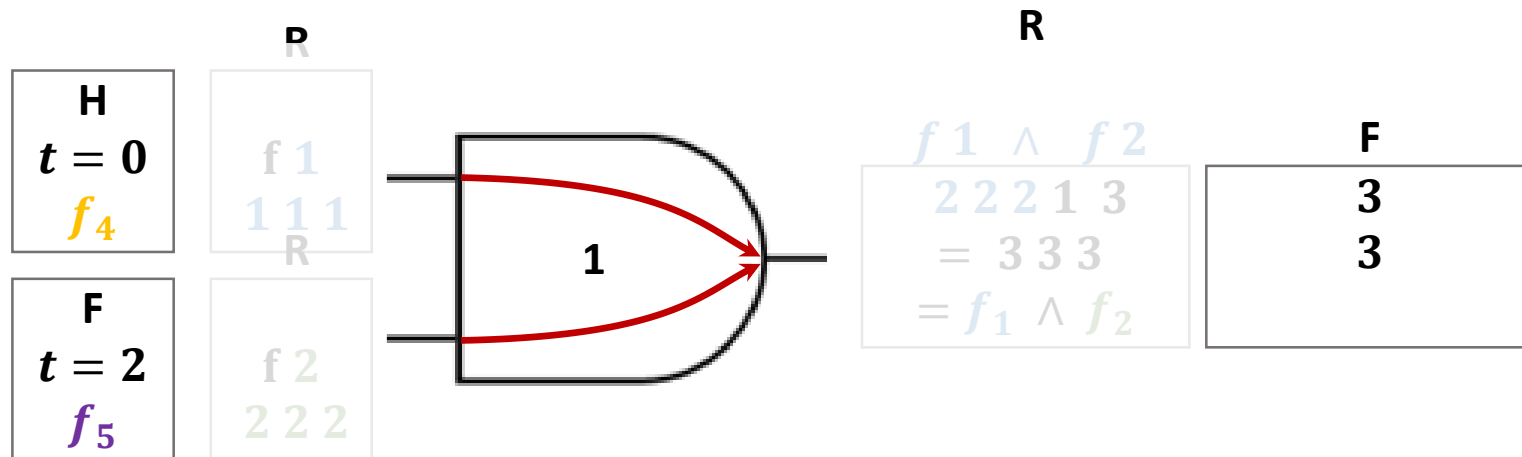
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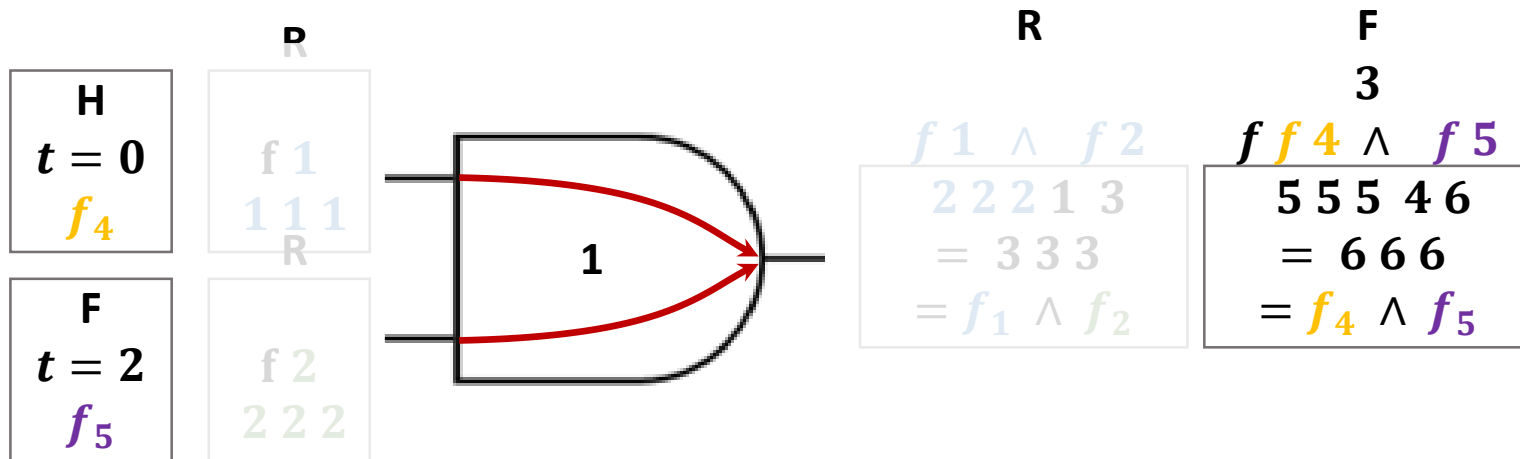
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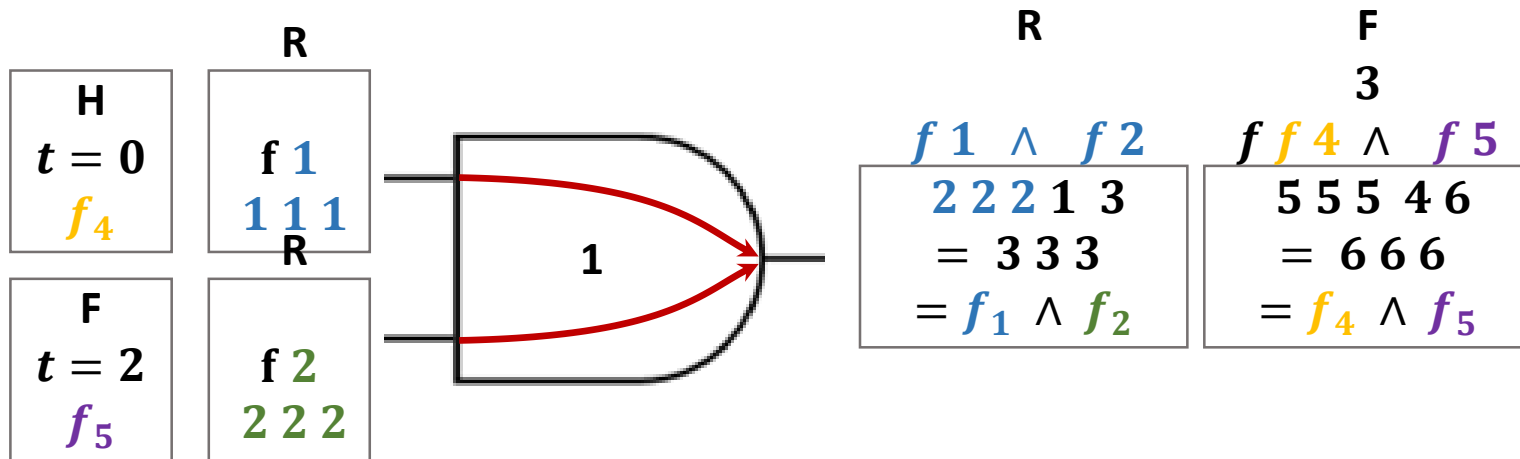
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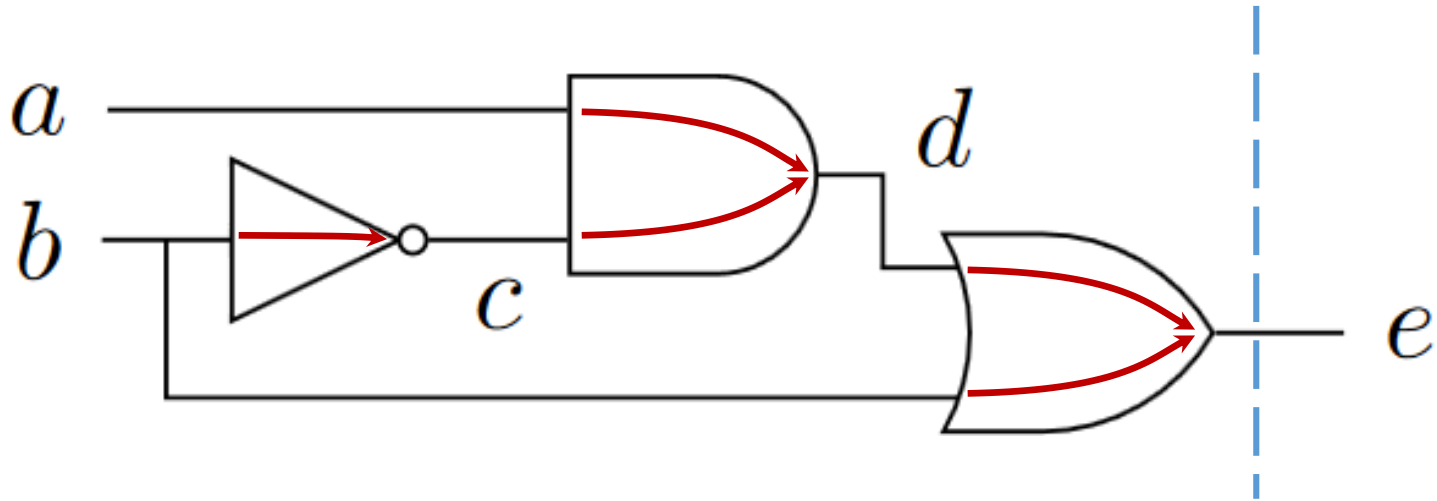
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Timing Tag Propagation

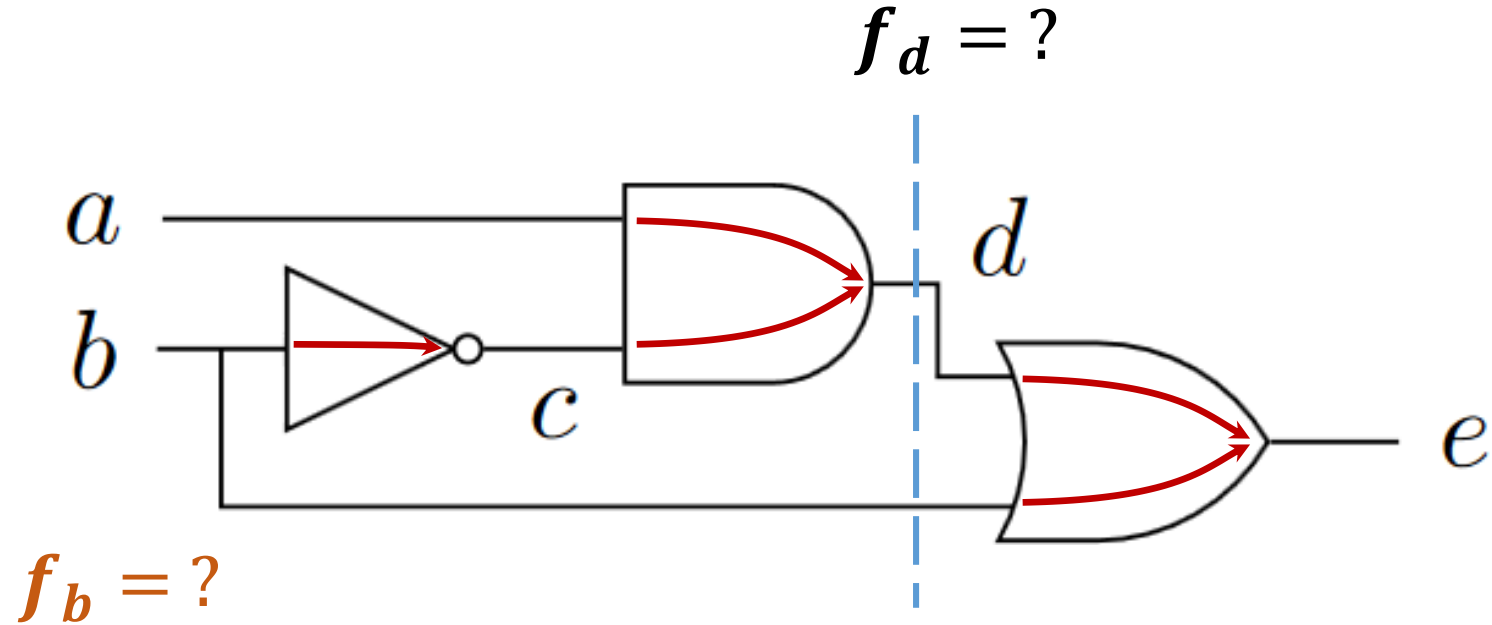
- Propagate timing tags



$$f_e = ?$$

Timing Tag Propagation

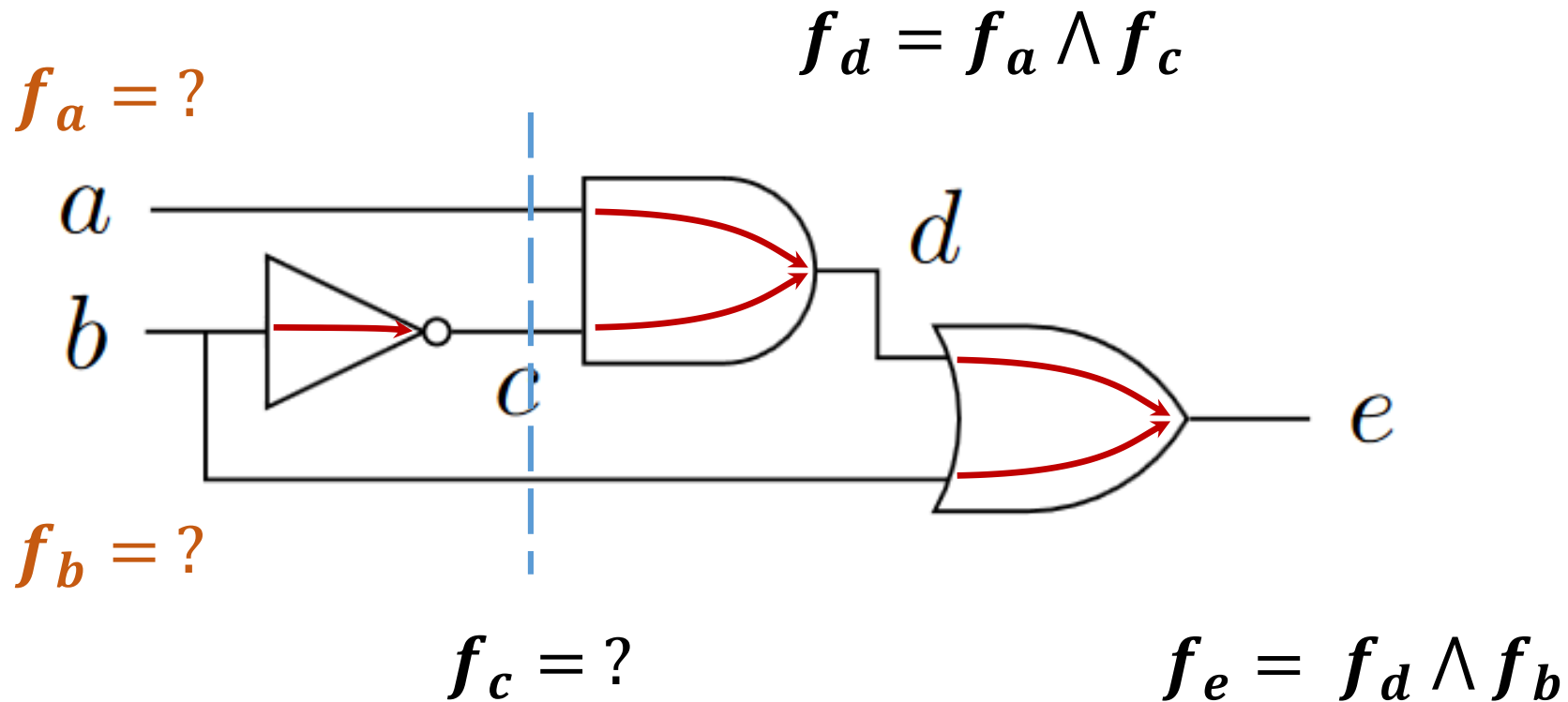
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$$f_e = f_d \wedge f_b$$

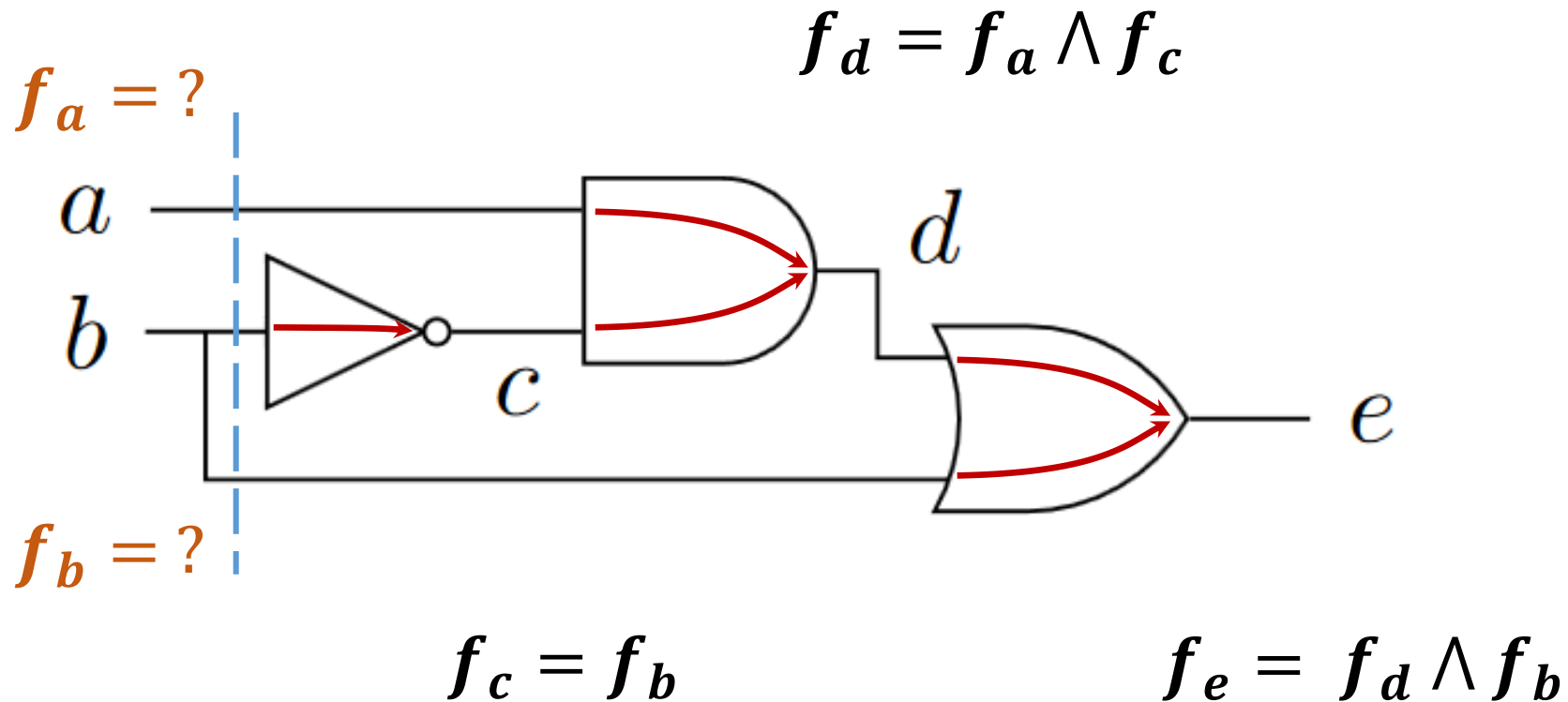
Timing Tag Propagation

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Timing Tag Propagation

- Propagate timing tags



Base Activation Functions

- **Base-case activation functions at Primary Inputs**
- **Two variables per input**

$$f_{rise}^{(a)} = \overline{x_a} \wedge x'_a$$

$$f_{fall}^{(a)} = x_a \wedge \overline{x'_a}$$

$$f_{high}^{(a)} = x_a \wedge x'_a$$

$$f_{low}^{(a)} = \overline{x_a} \wedge \overline{x'_a}$$

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$$f_{rise}^{(a)} = \overline{x_a} \wedge x'_a$$

$$f_{fall}^{(a)} = x_a \wedge \overline{x'_a}$$

Present State

$$f_{high}^{(a)} = x_a \wedge x'_a$$

Next State

$$f_{low}^{(a)} = \overline{x_a} \wedge \overline{x'_a}$$

Calculating Probabilities with #SAT

- Let f be an activation function, and $|f|$ its support size then:

$$p(f) = \frac{\text{\#SAT}(f)}{2^{|f|}}$$

- Assumes uniformly distributed independent variables

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- Assumes uniformly distributed independent variables
 - Assumption can be removed with pre-processing

Probability Example

$$p(f) = \frac{\#\text{SAT}(f)}{2^{|f|}}$$

$$f(x_a, x'_a, x_b, x'_b) = x_a \wedge x'_a \wedge x_b \wedge x'_b$$

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$$\#\text{SAT}(f) = 1$$

$$|f| = 4$$

Probability Example

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$$\#SAT(f) = 1$$

$$|f| = 4$$

$$p f = \frac{1}{2^4} = 0.0625$$

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ESTA Formulation Summary

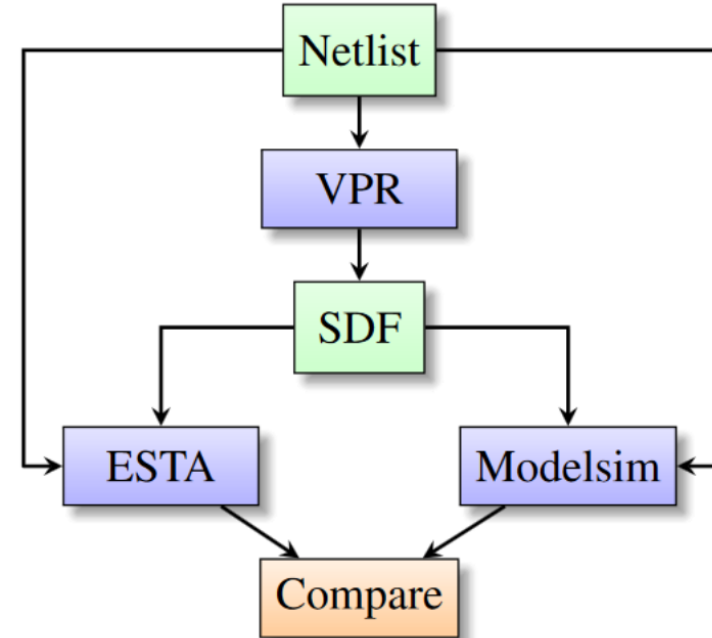
- **Propagate timing tags**
 - Calculate STA-like path-based delay estimates
 - Build activation functions
- **Probability Calculation**
 - Use #SAT to determine path probabilities

ESTA Implementation

- **Activation functions represented with Binary Decision Diagrams (BDDs)**
 - Easy manipulation
 - Efficient #SAT
- **Bound some path-delay combinations**
 - Improves scalability (fewer tags)
 - Adds some pessimism

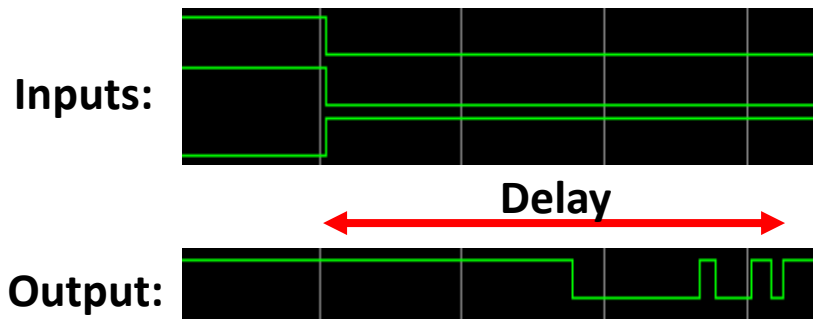
Evaluation Framework

- Determine maximum delay histogram across *all* outputs
- Benchmarks:
 - MCNC20:
 - 554 to 6239 LUTs
 - 8 to 1545 Primary Inputs
 - Post-place-and-route delays from 40nm FPGA
- Comparison:
 - Timing Simulation (Ground Truth)
 - ESTA
 - STA

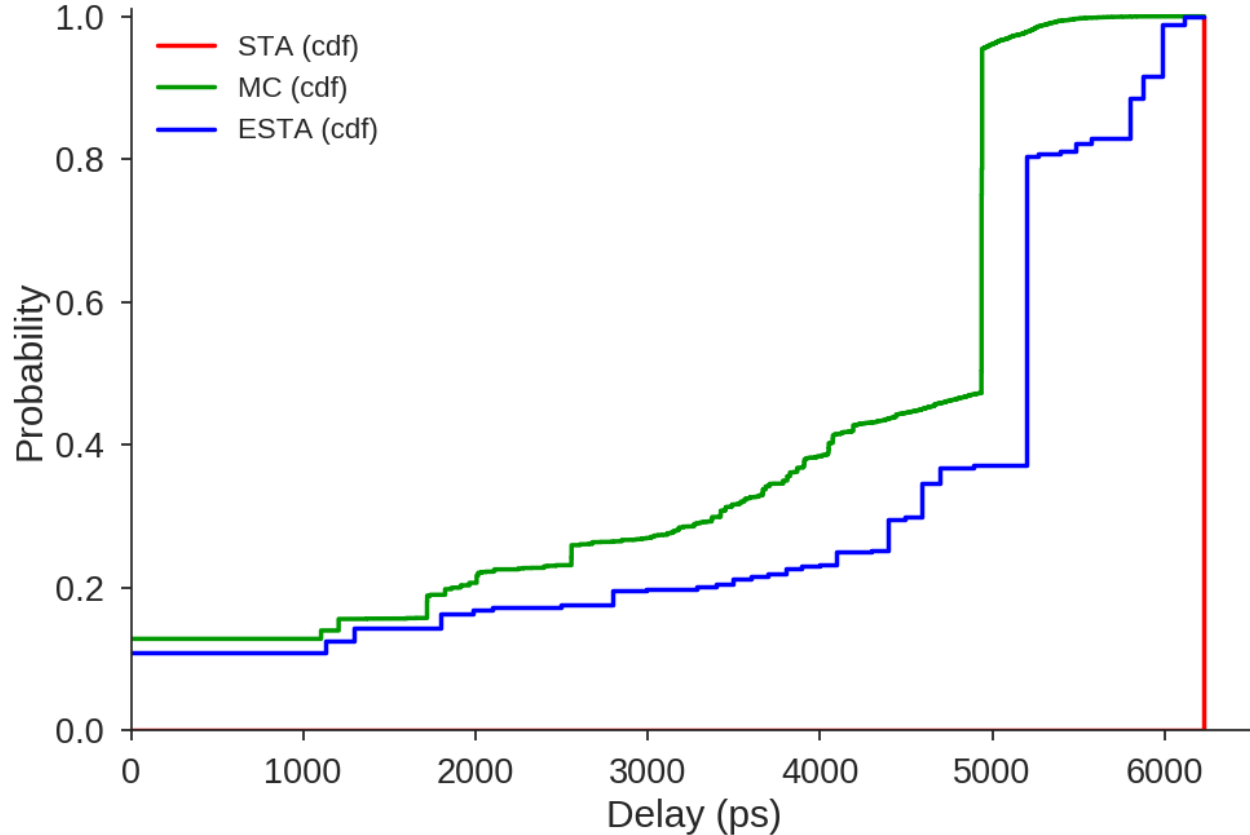


Timing Simulation

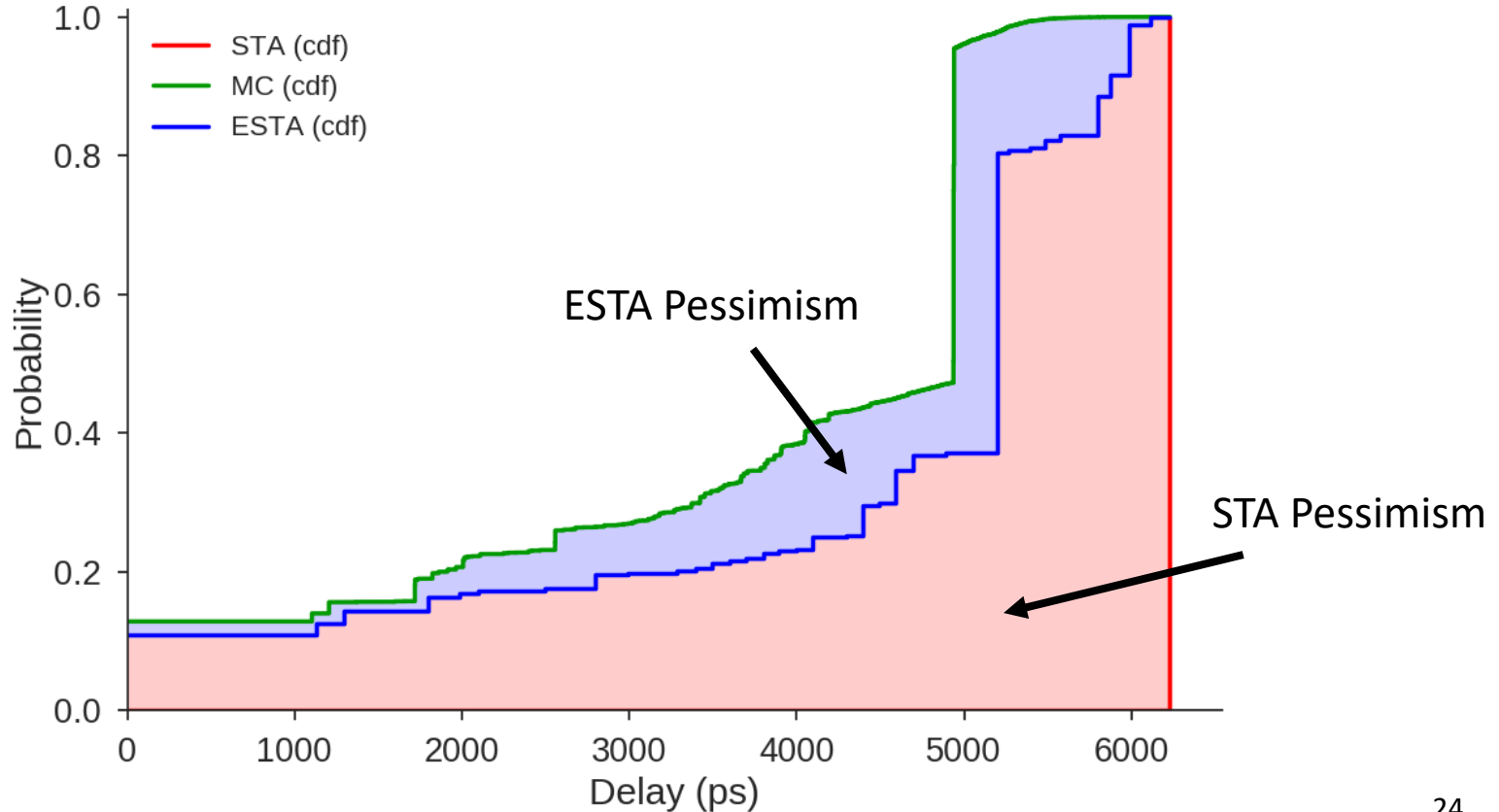
- Simulate primary input transitions
- Determine when primary outputs have stabilized
- Exhaustive Timing Simulation:
 - Test all possible input transitions
 - Impractical!
 - Input space too large
- Monte-Carlo Simulation:
 - Randomly sample input space
 - Detect when maximum delay has converged
 - Assumed ground truth



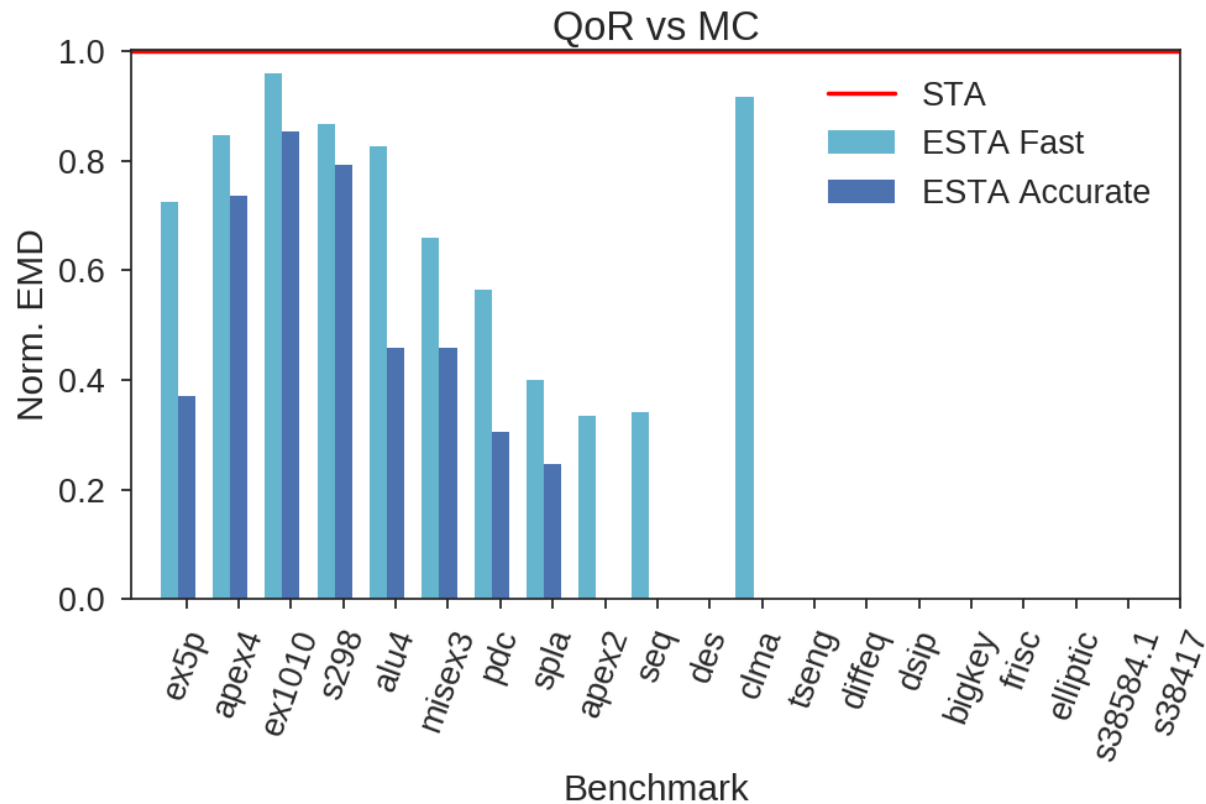
Experimental Results: Accuracy on SPLA



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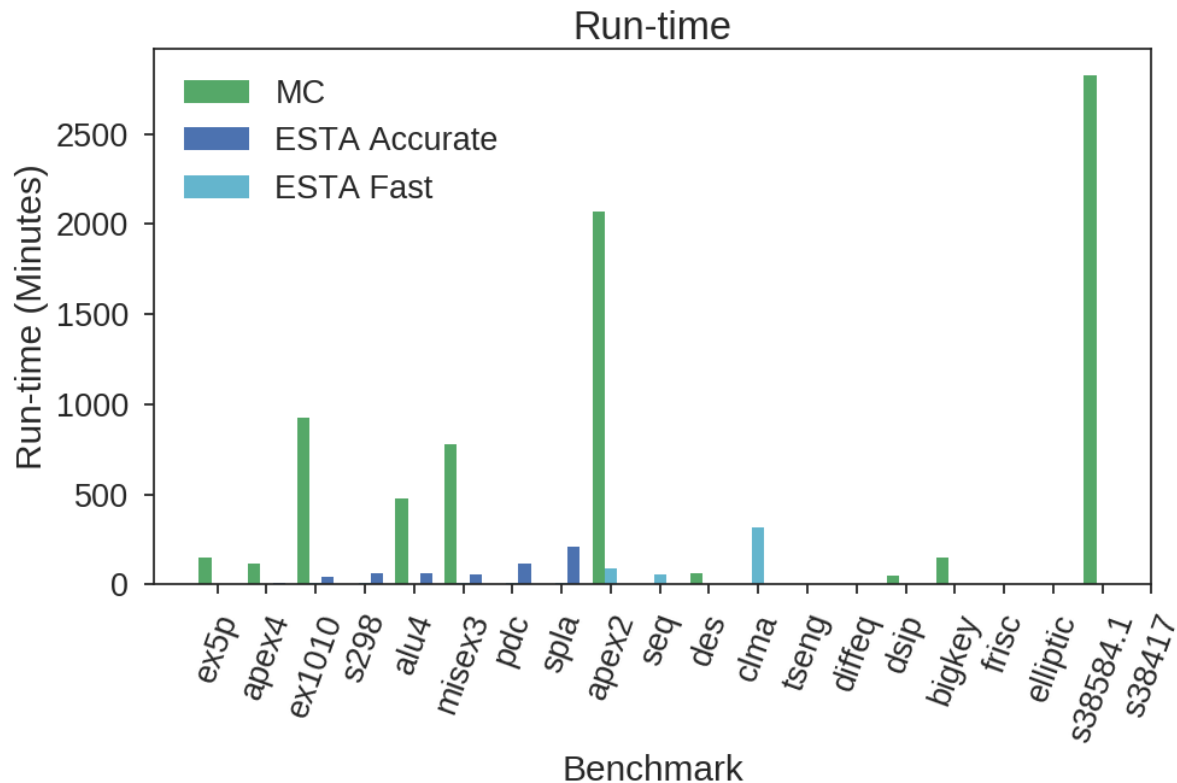
Experimental Results: Quality



- **ESTA:**

- **46% to 32% less pessimistic than STA**

Experimental Results: Run-time



- **48 hour completion:**

- MC: 10
- ESTA: 11

- **ESTA Speed-up:**

- 14.6x to 44.0x

Technique Comparison

	MC	ESTA	STA
Scalable			
Safe Analysis			
Overly Pessimistic			
False Paths			
Statistical Delays		*	

* Future work

Conclusion & Future Work

- **Introduced ESTA method:**
 - Performs timing analysis with non-worst-case switching
 - Calculates timing path activation probabilities using #SAT
- **Described an ESTA implementation:**
 - 46% to 32% less pessimistic than STA
 - 14.6x to 44.0x faster than MC Timing Simulation
- **Future work:**
 - Improve scalability
 - More general input distributions
 - Feedback analysis results to optimization tools (Place & Route)
 - Application studies

Thanks!

Questions?

Backup

Complexity

- Exhaustive Simulation:

$$O(n \cdot 4^I)$$

- ESTA:

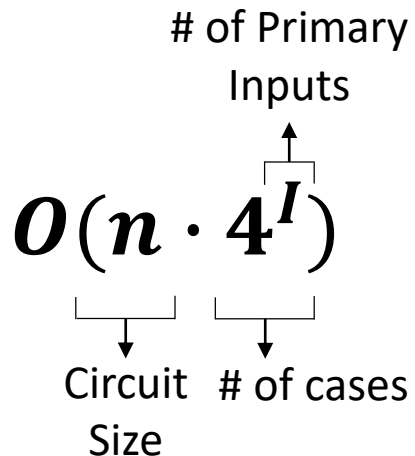
$$O(n \cdot L^K + 4^I)$$

Complexity

- Exhaustive Simulation:

$$O(\underbrace{n}_{\substack{\text{Circuit} \\ \text{Size}}} \cdot \underbrace{4^I}_{\substack{\text{\# of cases}}})$$

of Primary
Inputs



- ESTA:

$$O(n \cdot L^K + 4^I)$$

Complexity

- Exhaustive Simulation:

$$O(n \cdot 4^I)$$

of Primary
Inputs

Circuit # of cases
Size

The diagram illustrates the complexity of Exhaustive Simulation as $O(n \cdot 4^I)$. The variable n represents the Circuit Size, indicated by a bracket underneath. The term 4^I represents the number of cases, also indicated by a bracket underneath. The exponent I is further defined as the number of Primary Inputs, with an arrow pointing from I to this label above the equation.

- ESTA:

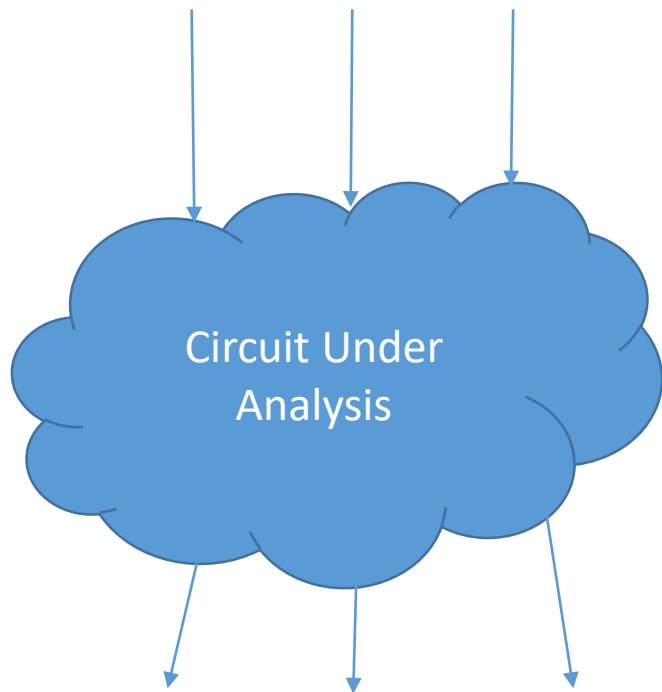
$$O(n \cdot L^K + 4^I)$$

Graph Traversal #SAT

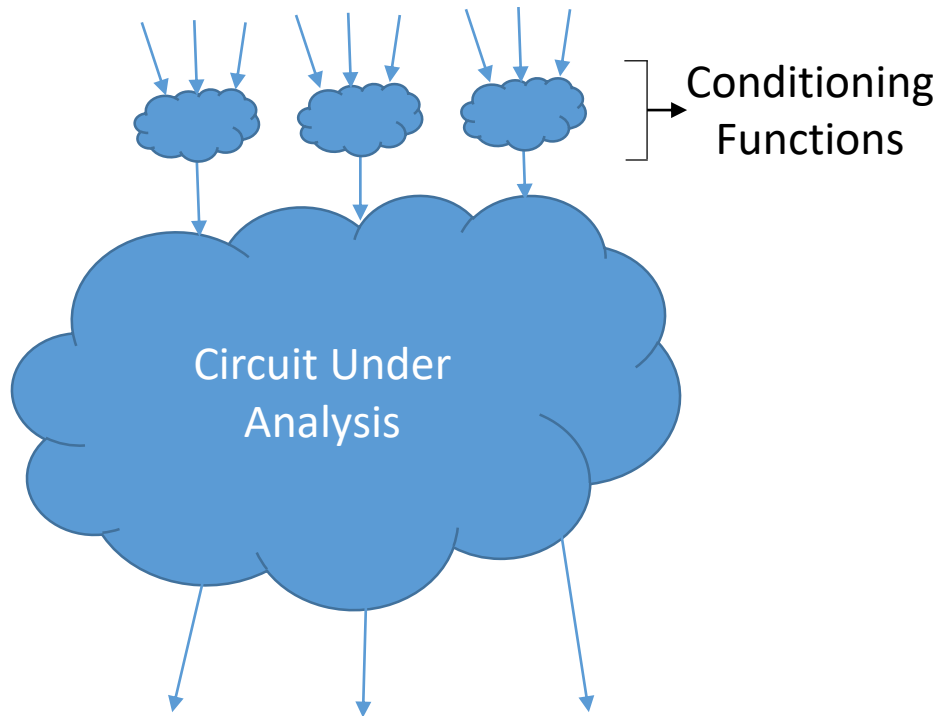
The diagram illustrates the complexity of ESTA as $O(n \cdot L^K + 4^I)$. The term $n \cdot L^K$ represents Graph Traversal, indicated by a bracket underneath. The term 4^I represents the number of SAT problems (#SAT), also indicated by a bracket underneath.

Non-uniform Input Probabilities

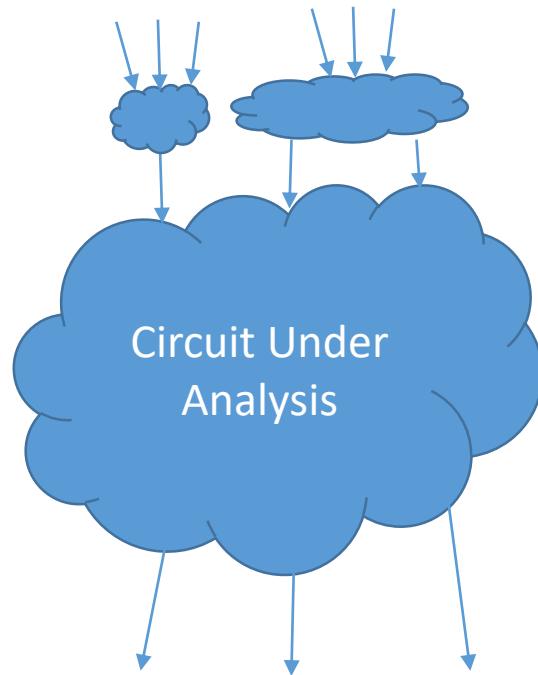
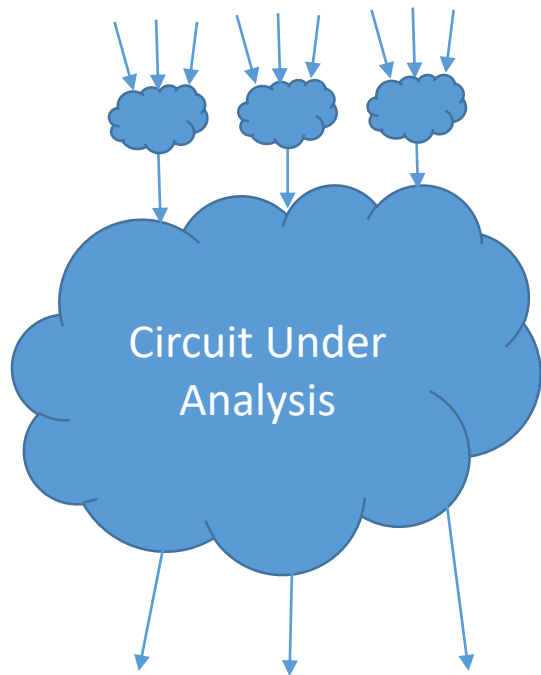
$\{r: 0.25, f: 0.25, h: 0.25, l: 0.25\}$



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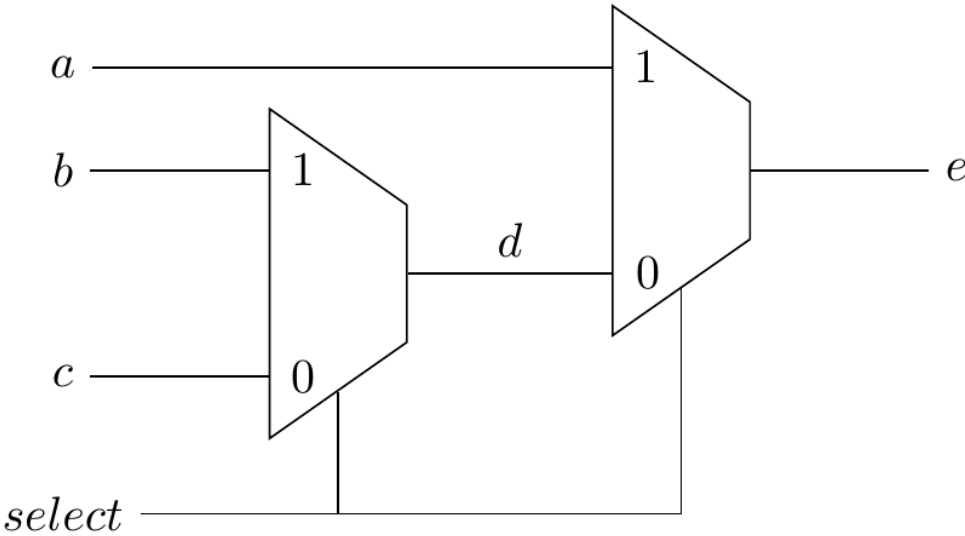


Correlated Input Probabilities



- **Correlation determined by:**
 - Number of shared variables
 - Activation function cover overlaps

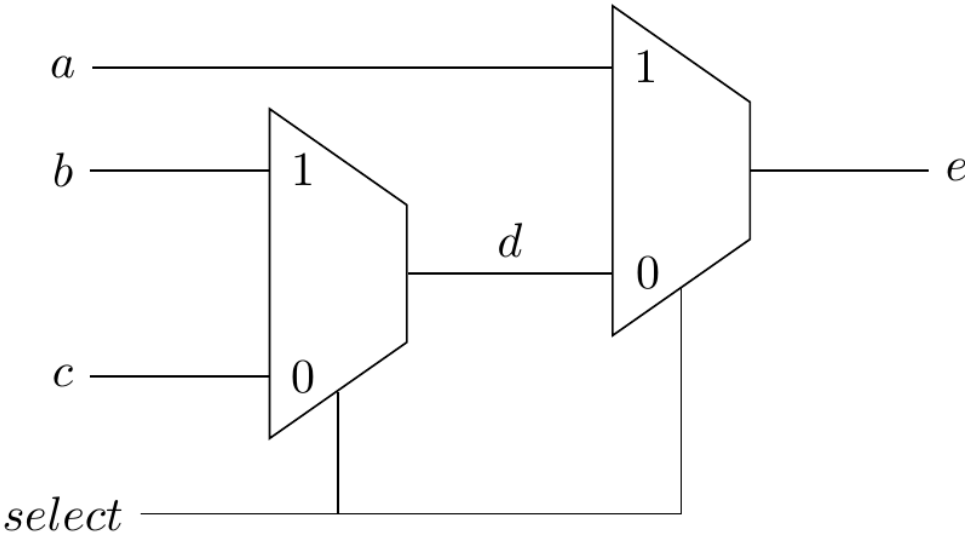
False Paths



- ***b-d-e* is a false path**

	STA	MC	ESTA
s298	1.000	0.981	0.981
clma	1.000	0.959	0.984
frisc	1.000	0.965	0.999
elliptic	1.000	0.974	

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	STA	MC	ESTA	
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clma	1.000	0.959	0.984	
frisc	1.000	0.965	0.999	*
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- **MC underestimates clma worst-case delay**