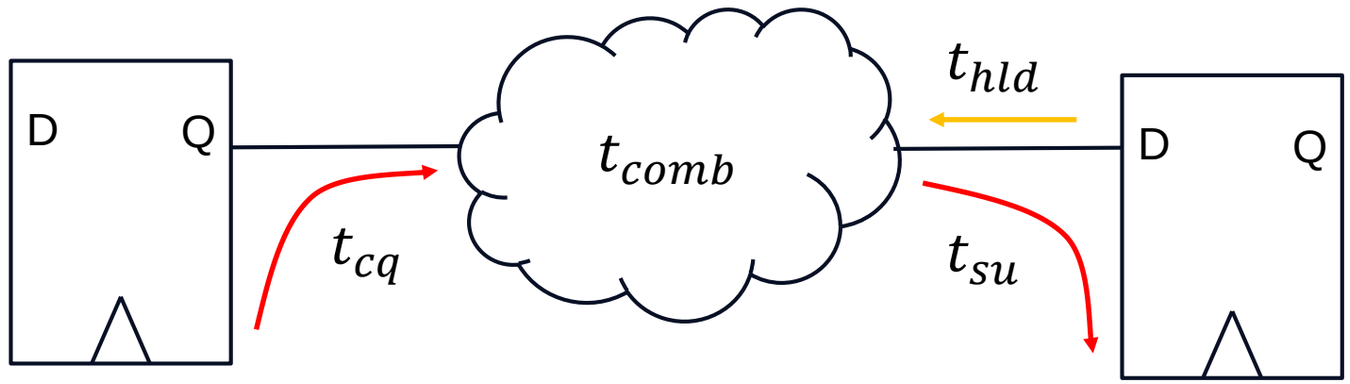
Tatum: Parallel Timing Analysis for Faster Design Cycles and Improved Optimization

Kevin E. Murray and Vaughn Betz

UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE & ENGINEERING

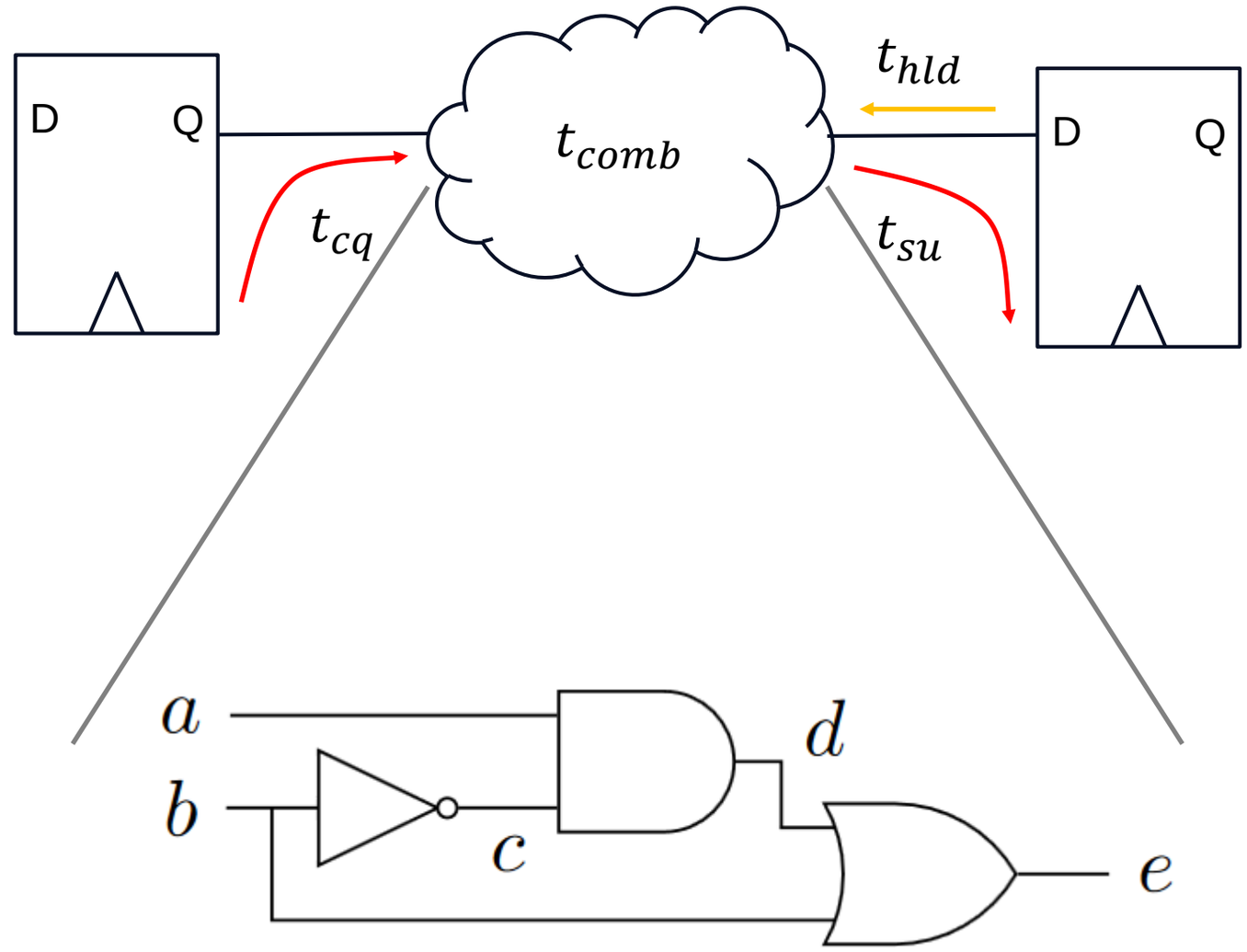
Timing Analysis



$$t_{cq} + t_{comb} + t_{su} \leq \frac{1}{f_{max}}$$

$$t_{cq} + t_{comb} \geq t_{hld}$$

Timing Analysis



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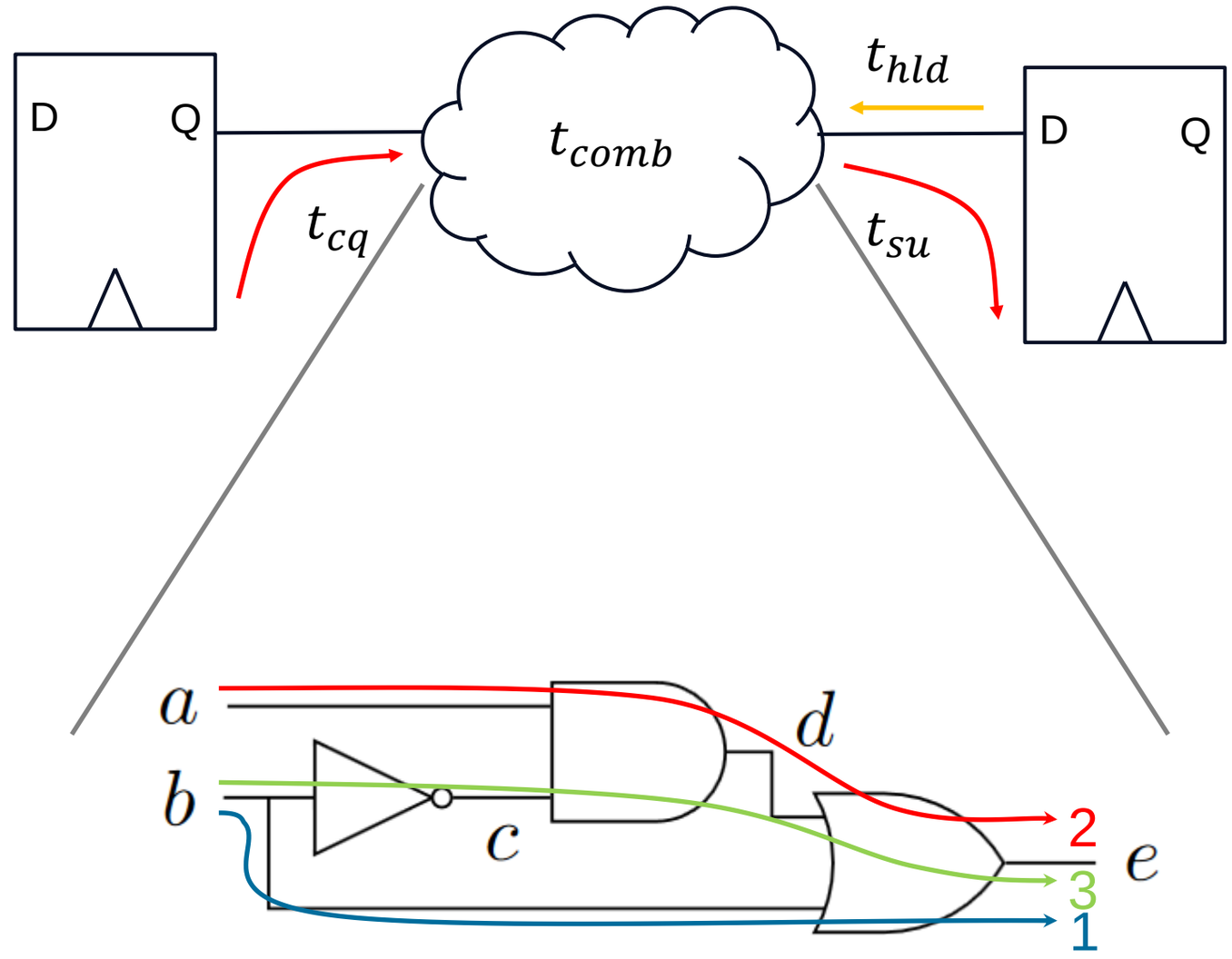

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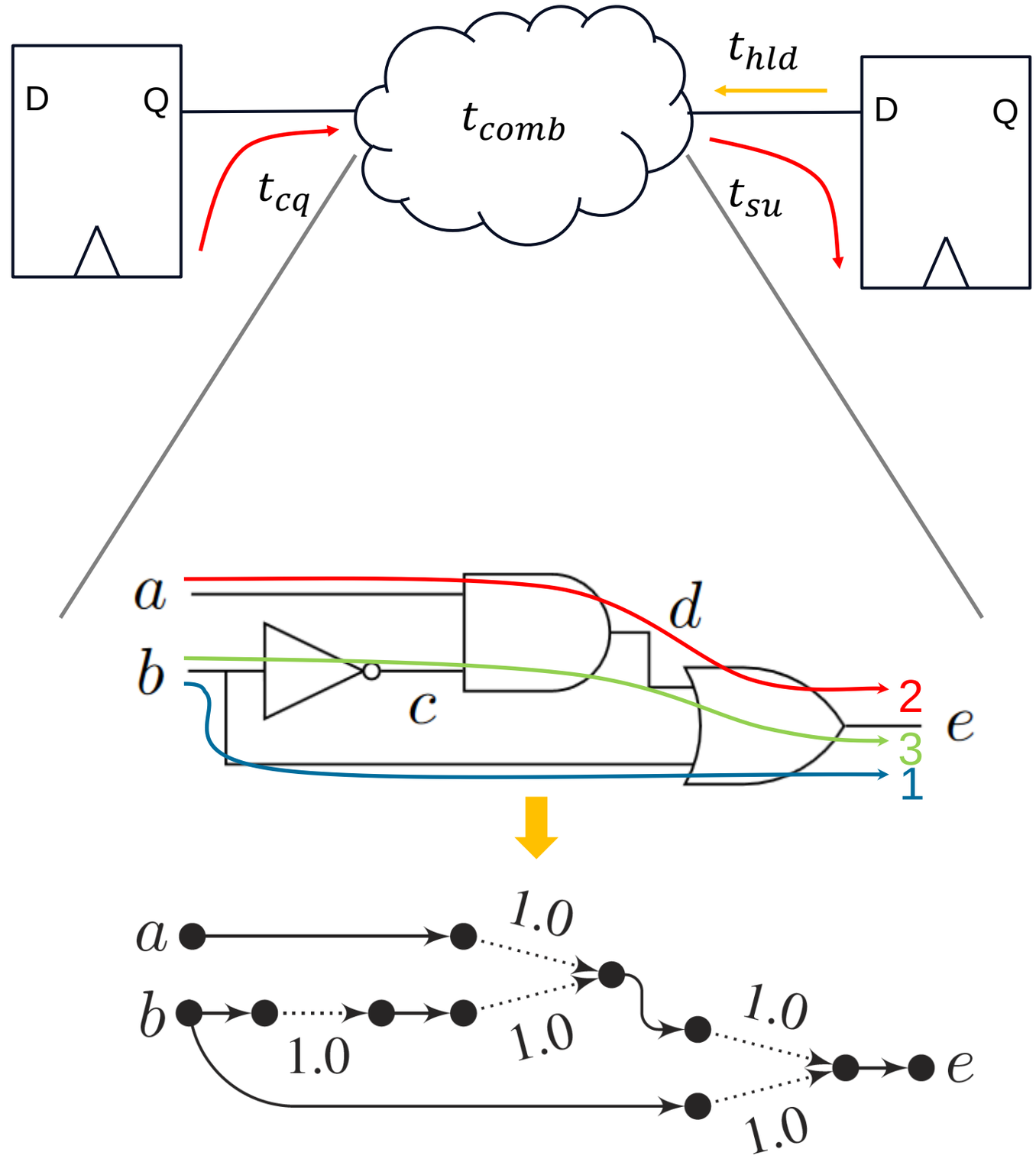

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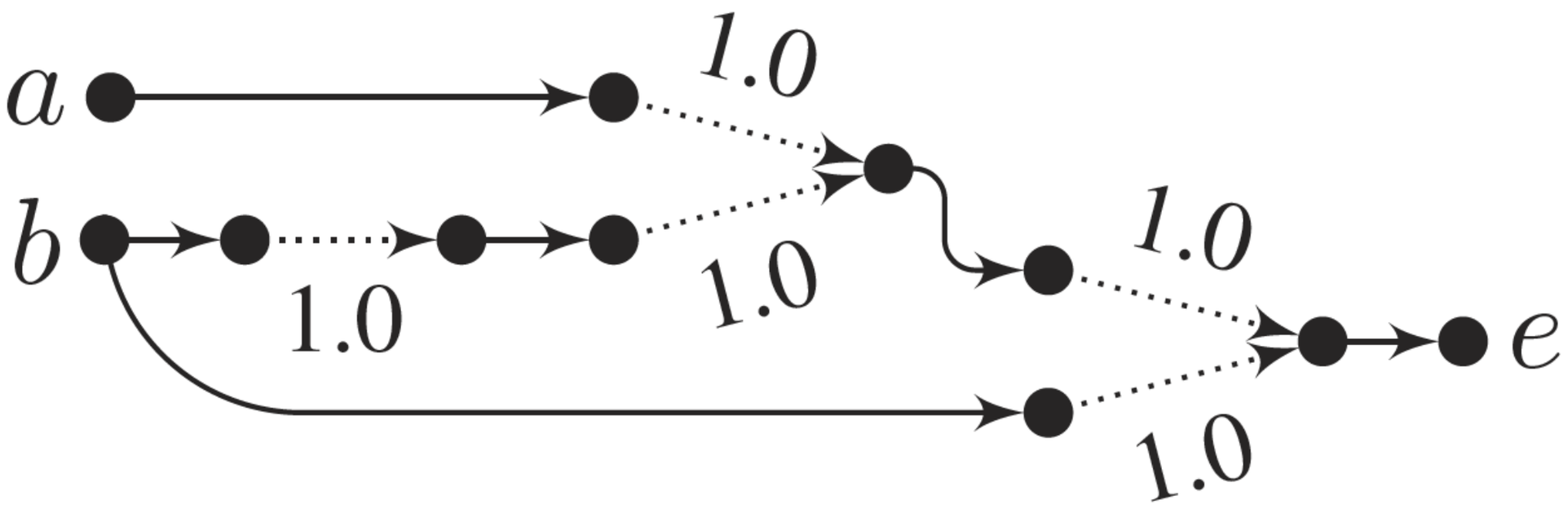

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- Backward: Required Times & Slack
- Linear Time: **O(V+E)**

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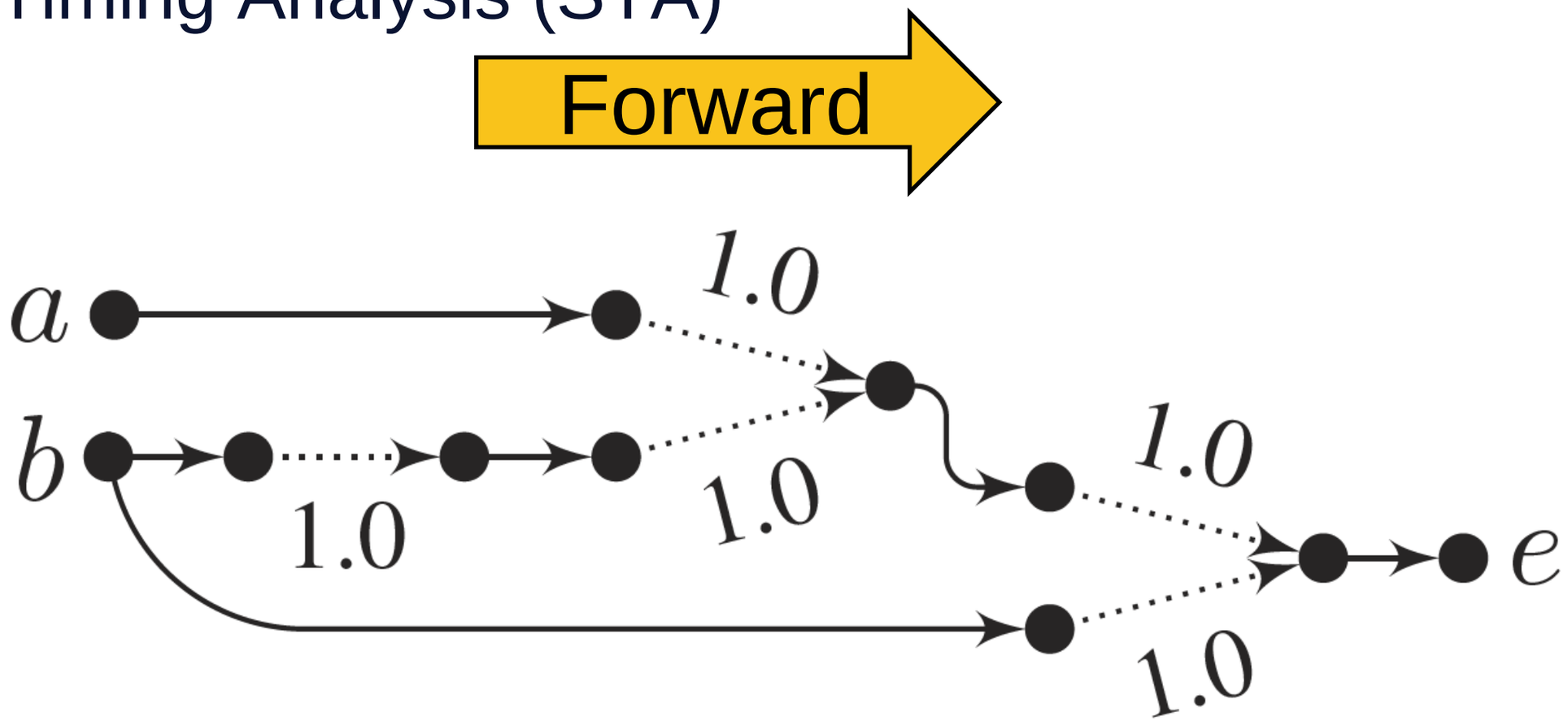

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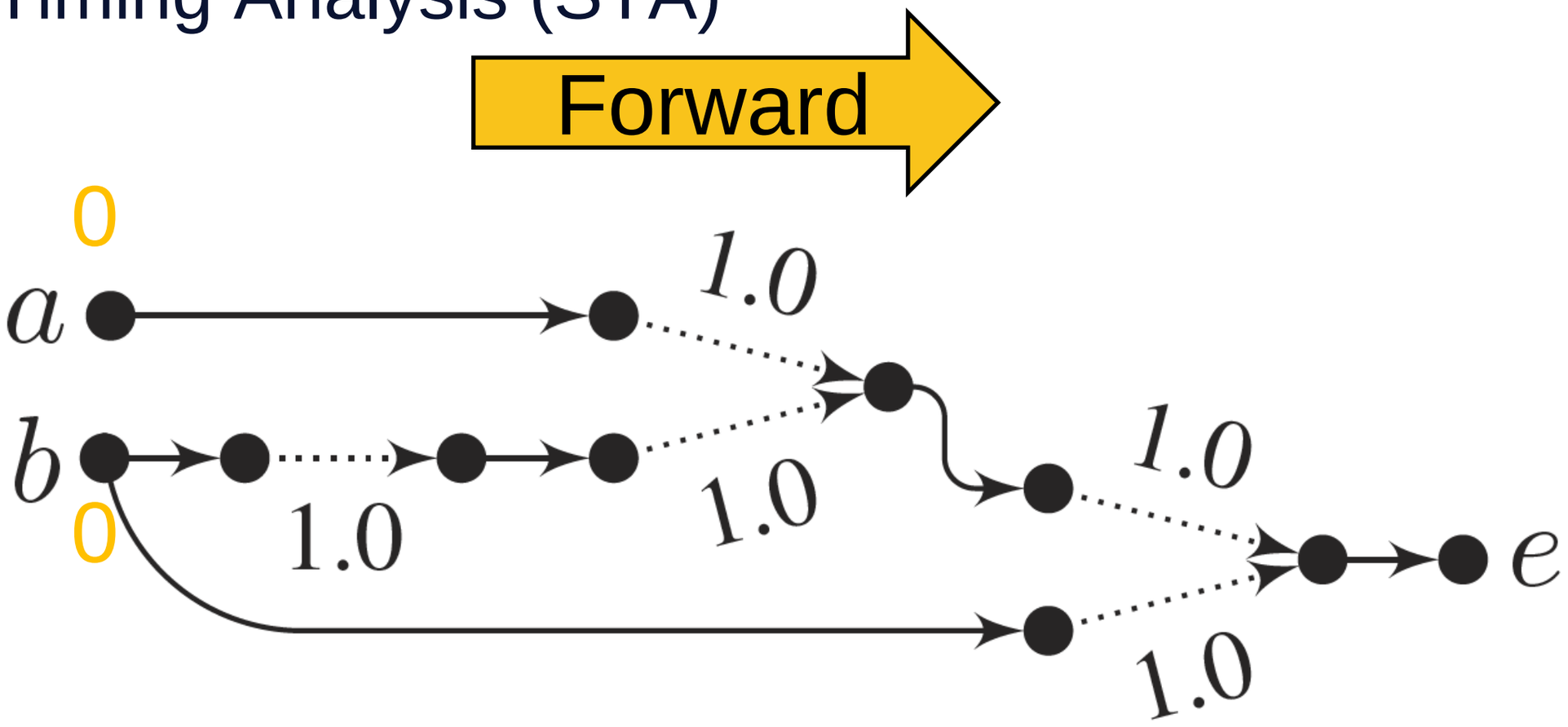

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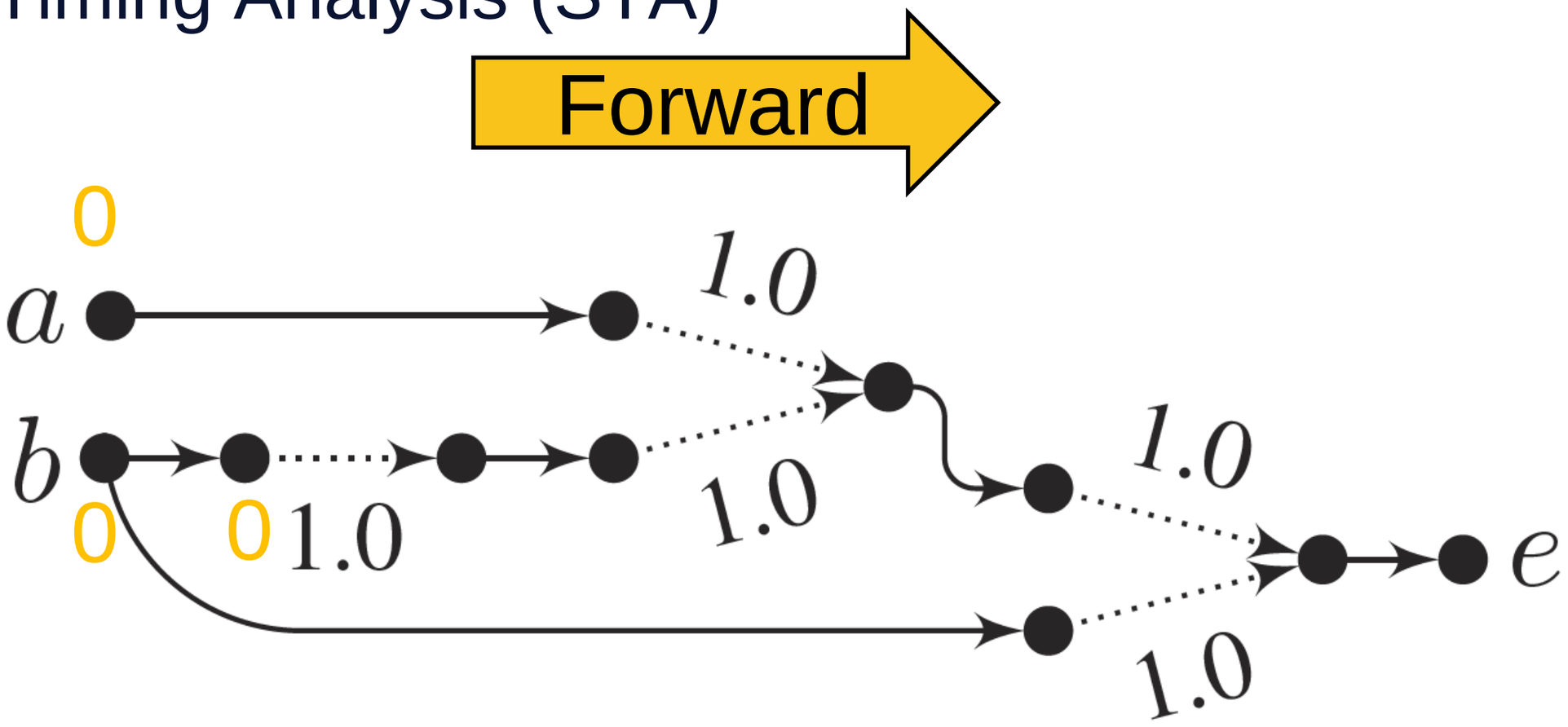

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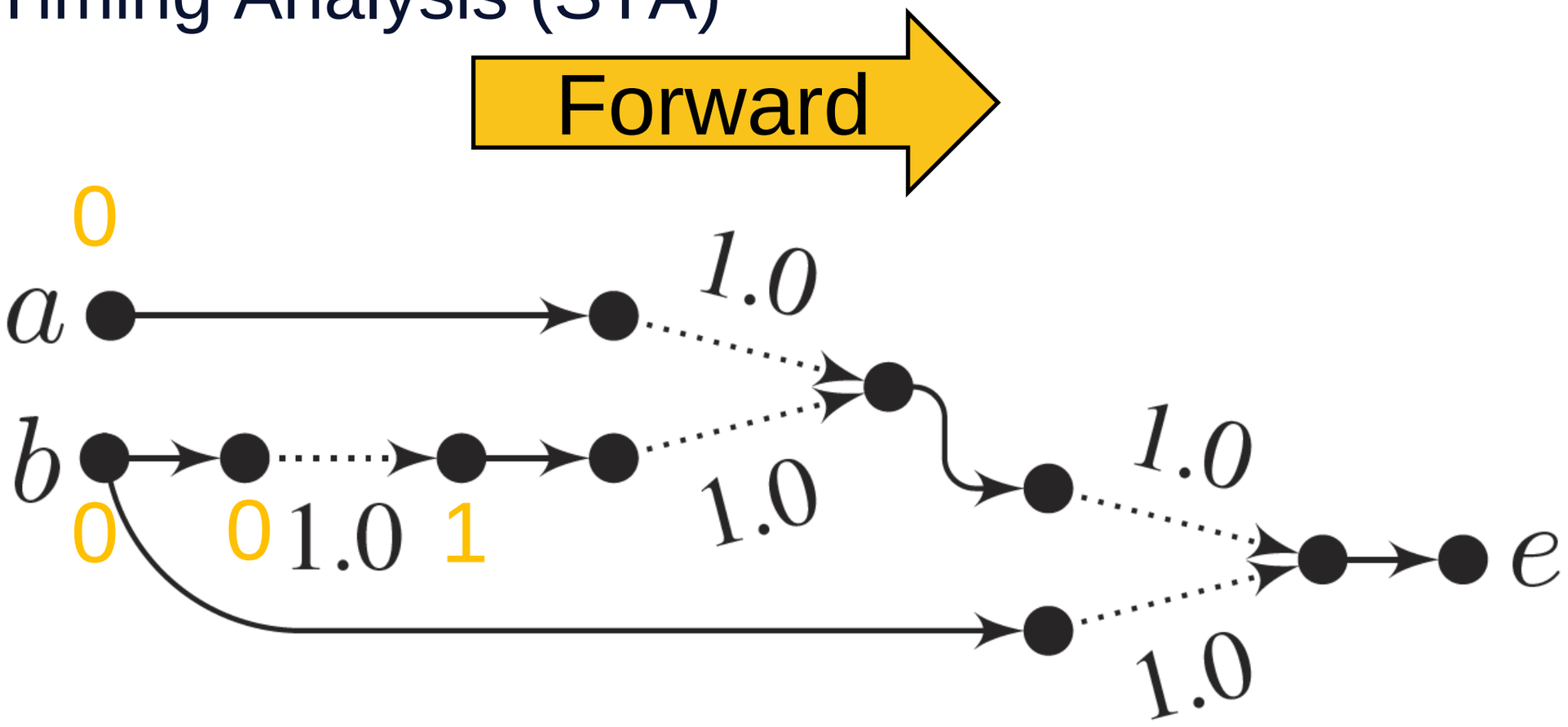

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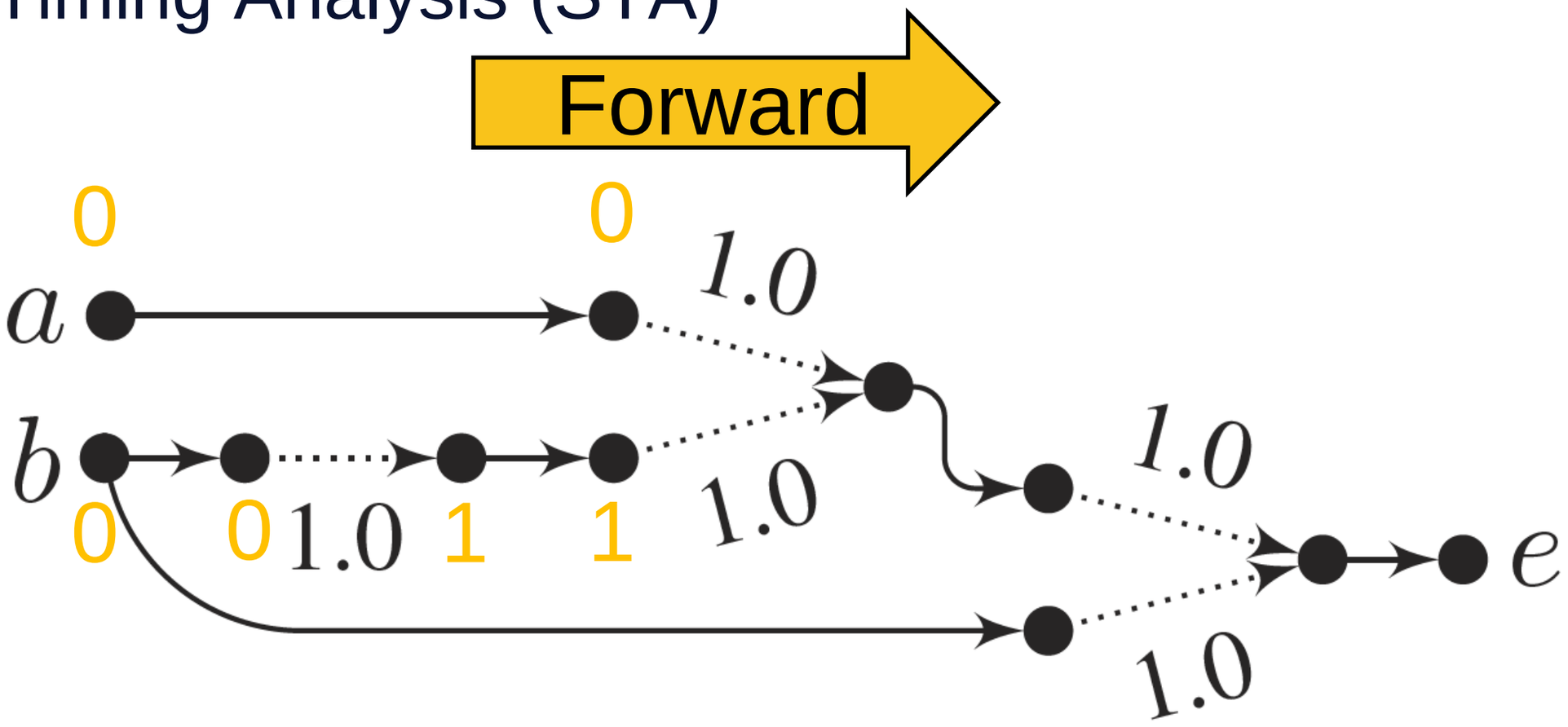

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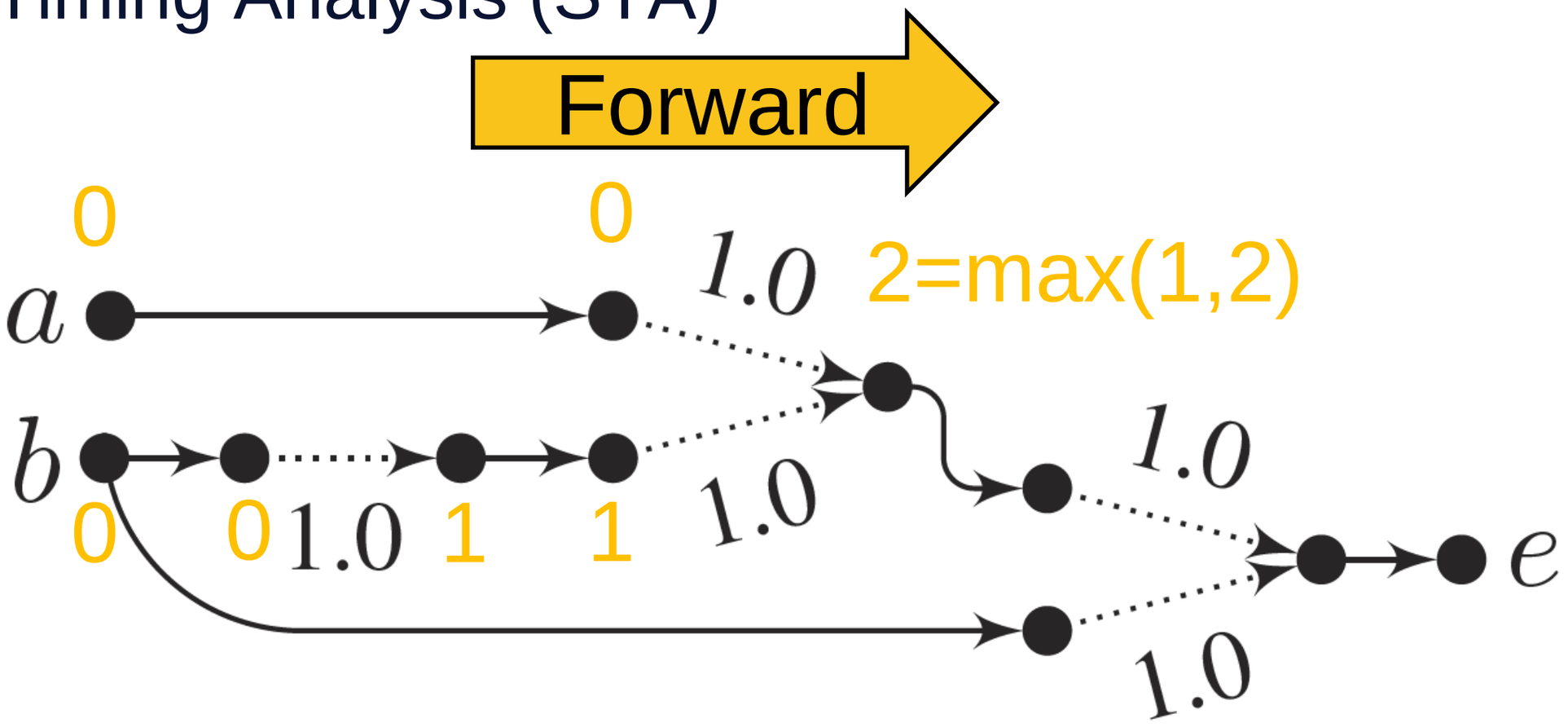

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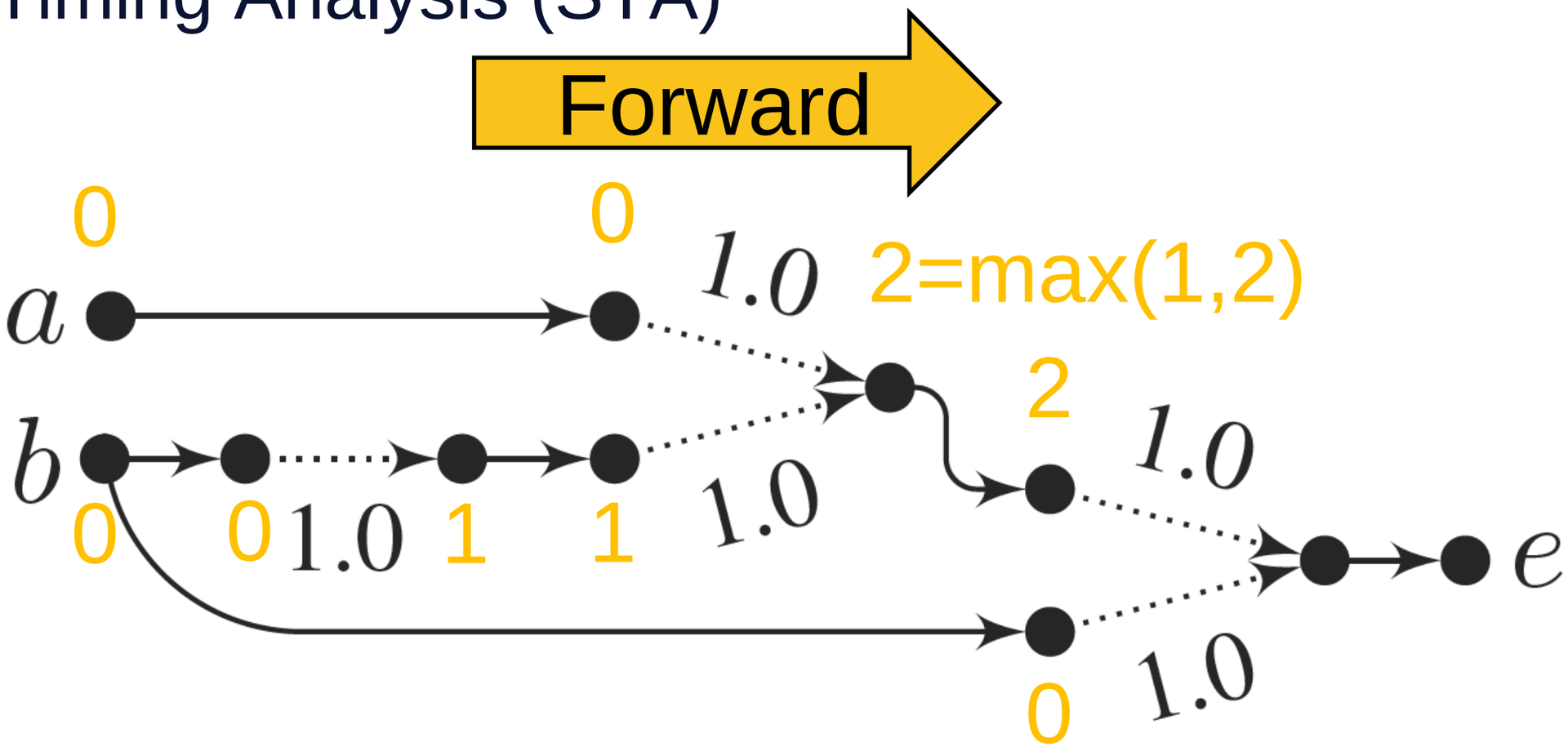

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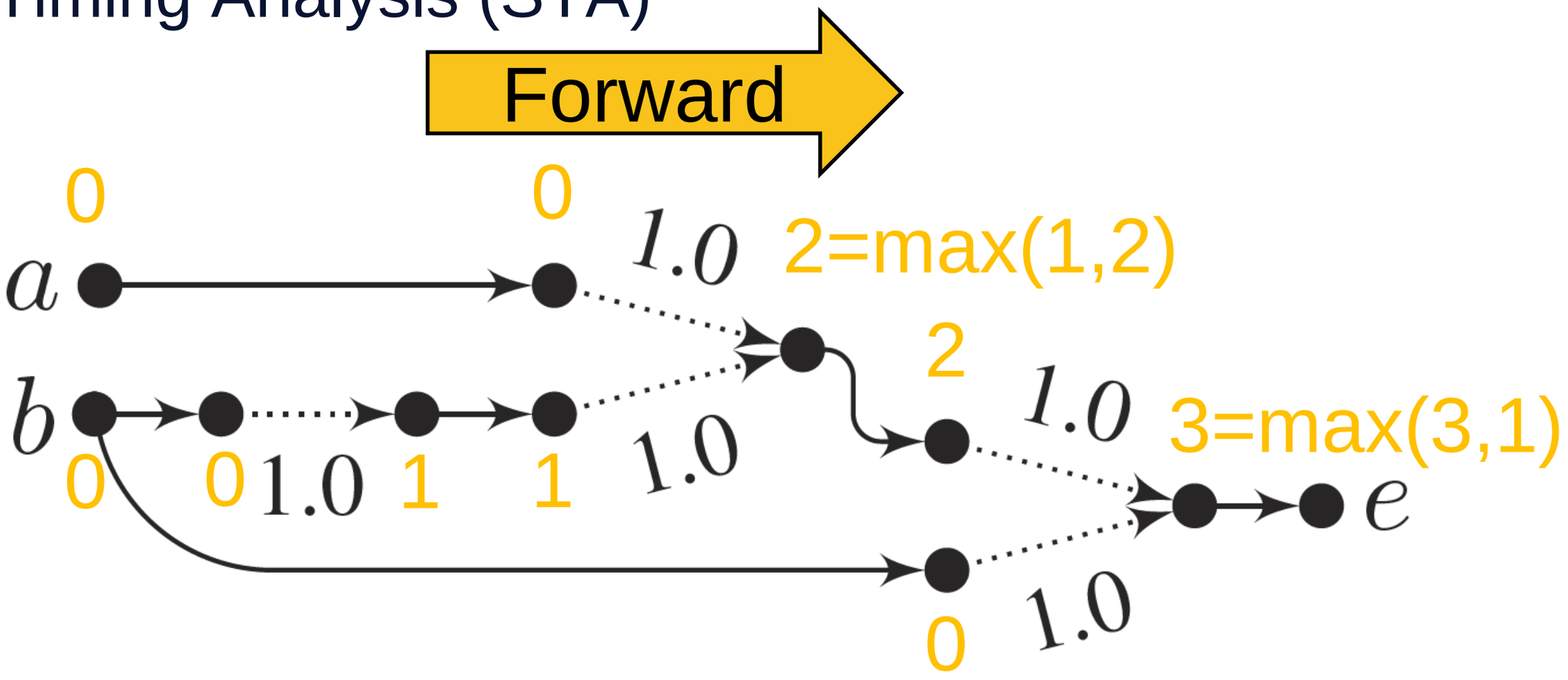

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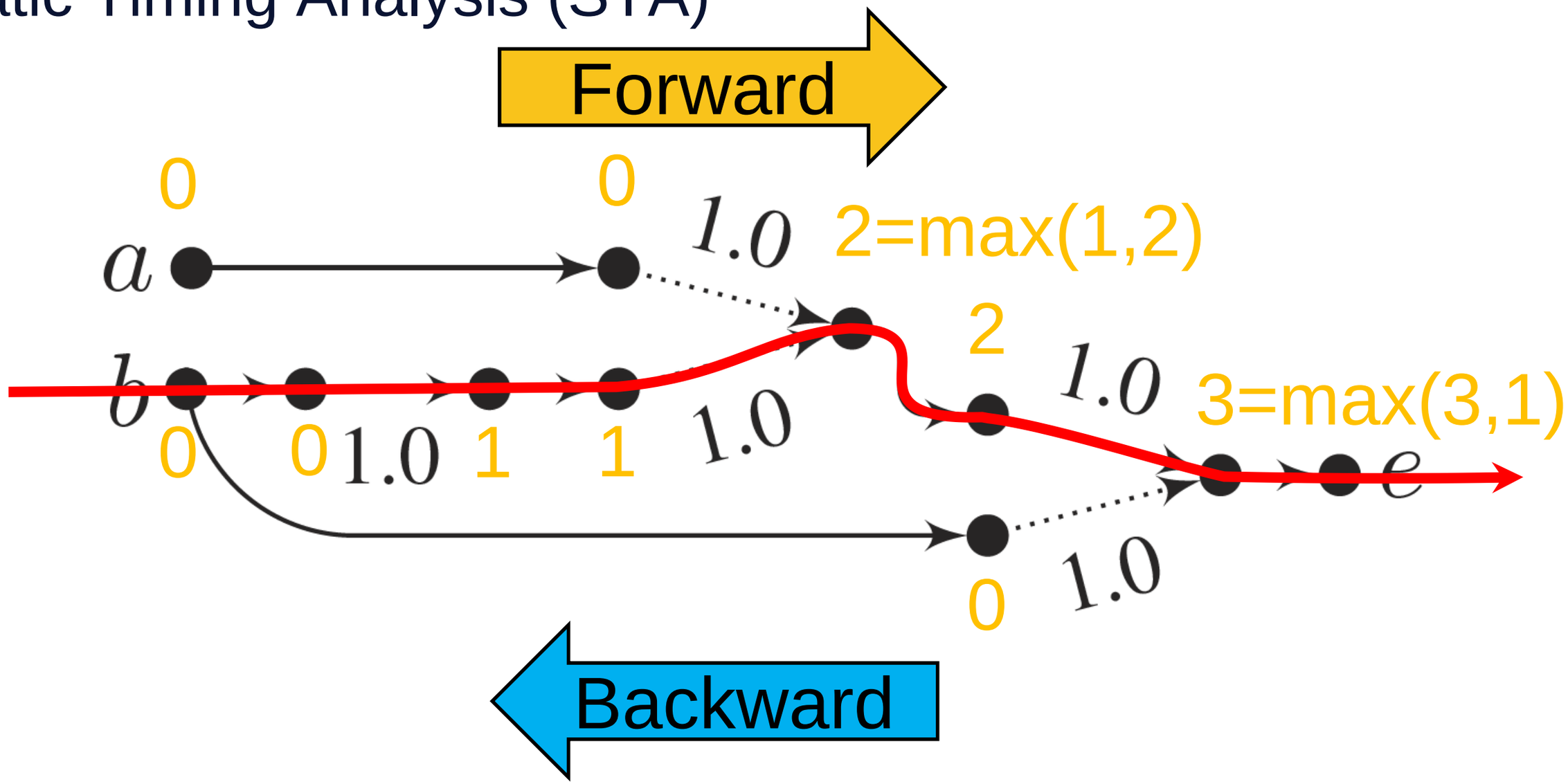

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Tatum

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- High performance & full featured STA engine
- Supports:
  - Maximum (Setup) & Minimum (Hold) Analysis
  - Multiple Clocks
  - Various Timing Constraints/Exceptions
    - *False Paths*
    - *Multicycle Paths*
  - Application defined Timing Graph
  - Application defined Delay Calculator

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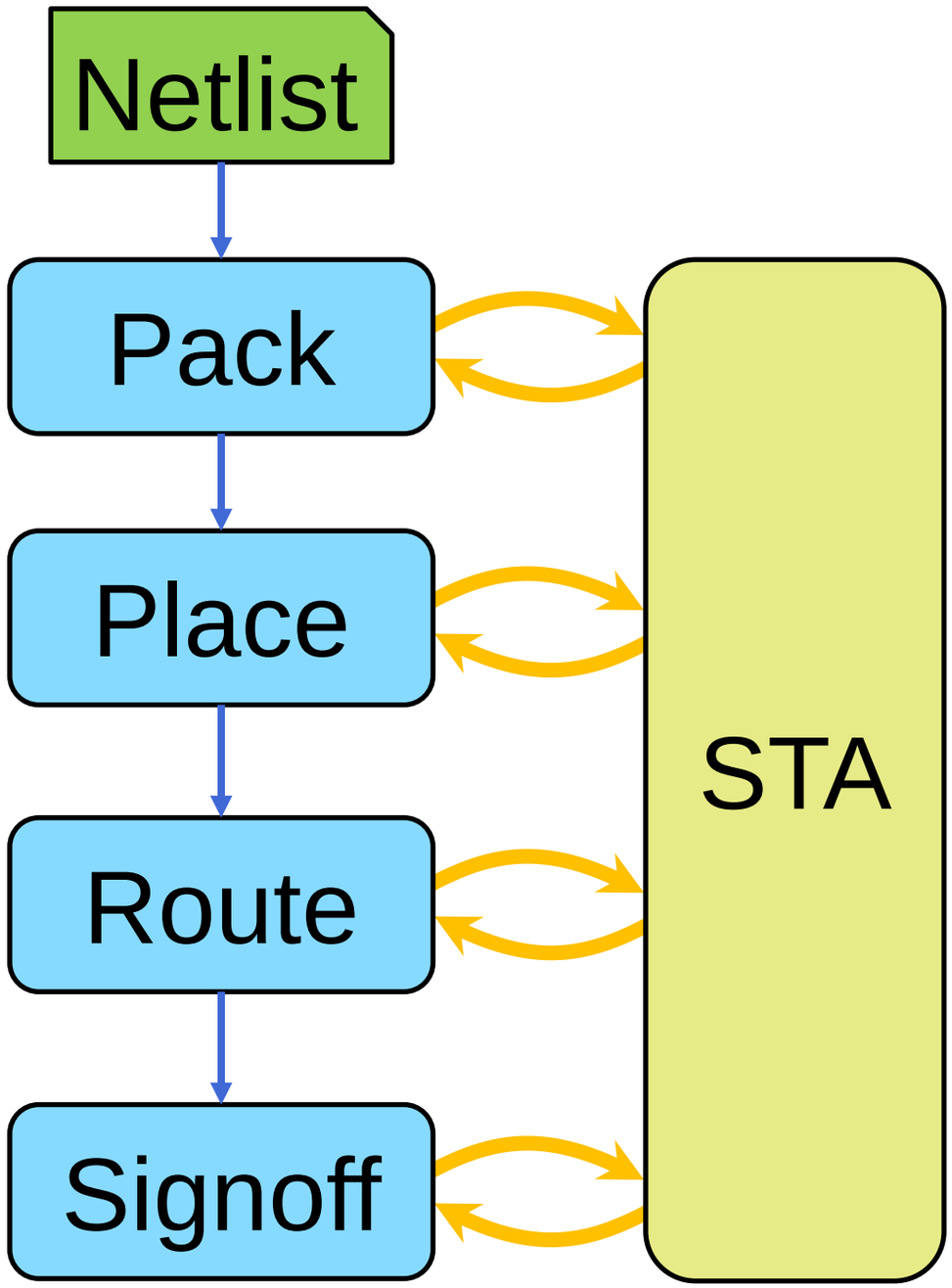
Not Enough!

FPGA Design Flow & STA

- STA used extensively to guide optimization
  - VPR calls STA hundreds of times
  - Quartus can spend 25+% run-time on STA [1]
- Typically use stale timing information



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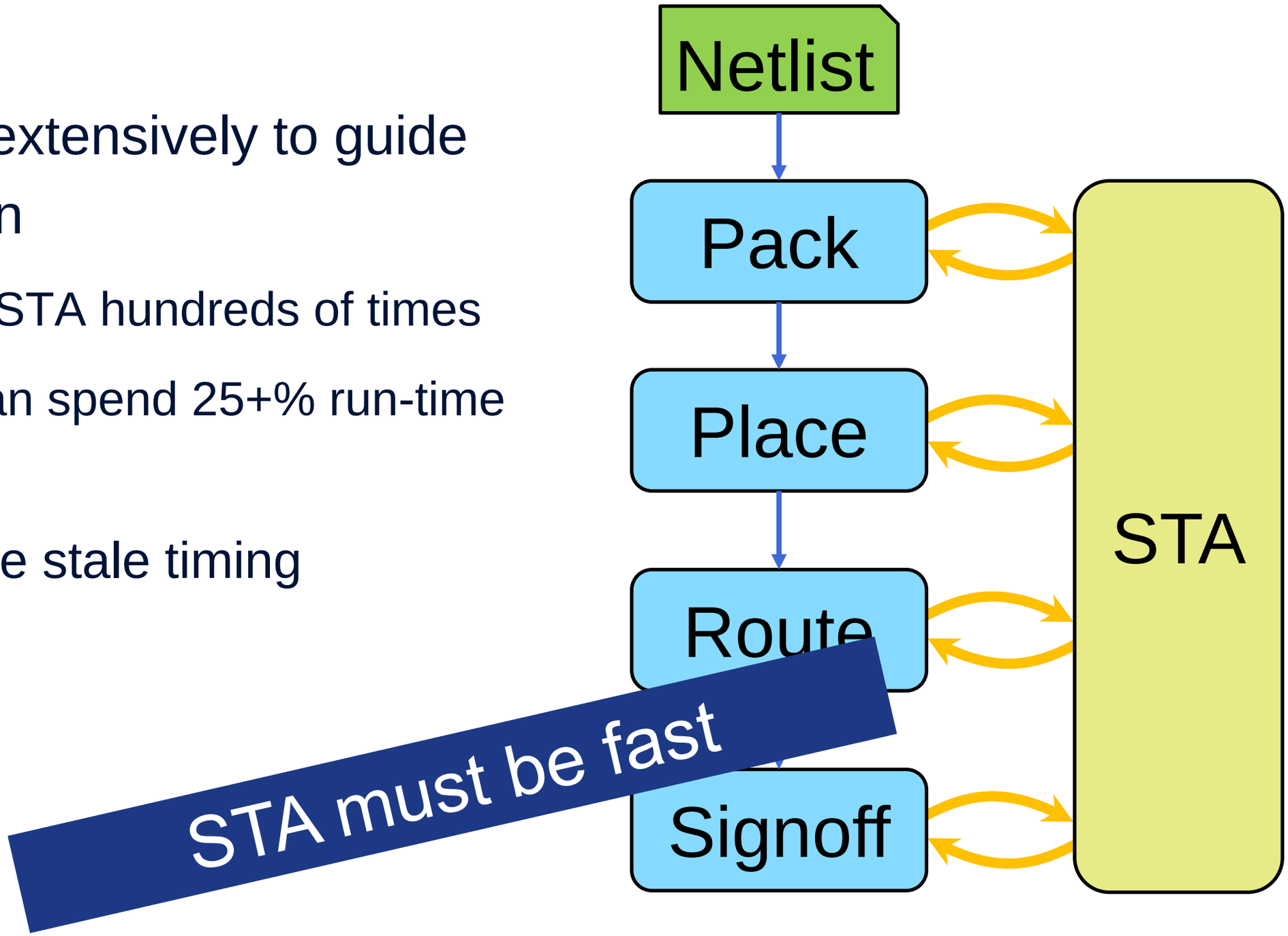

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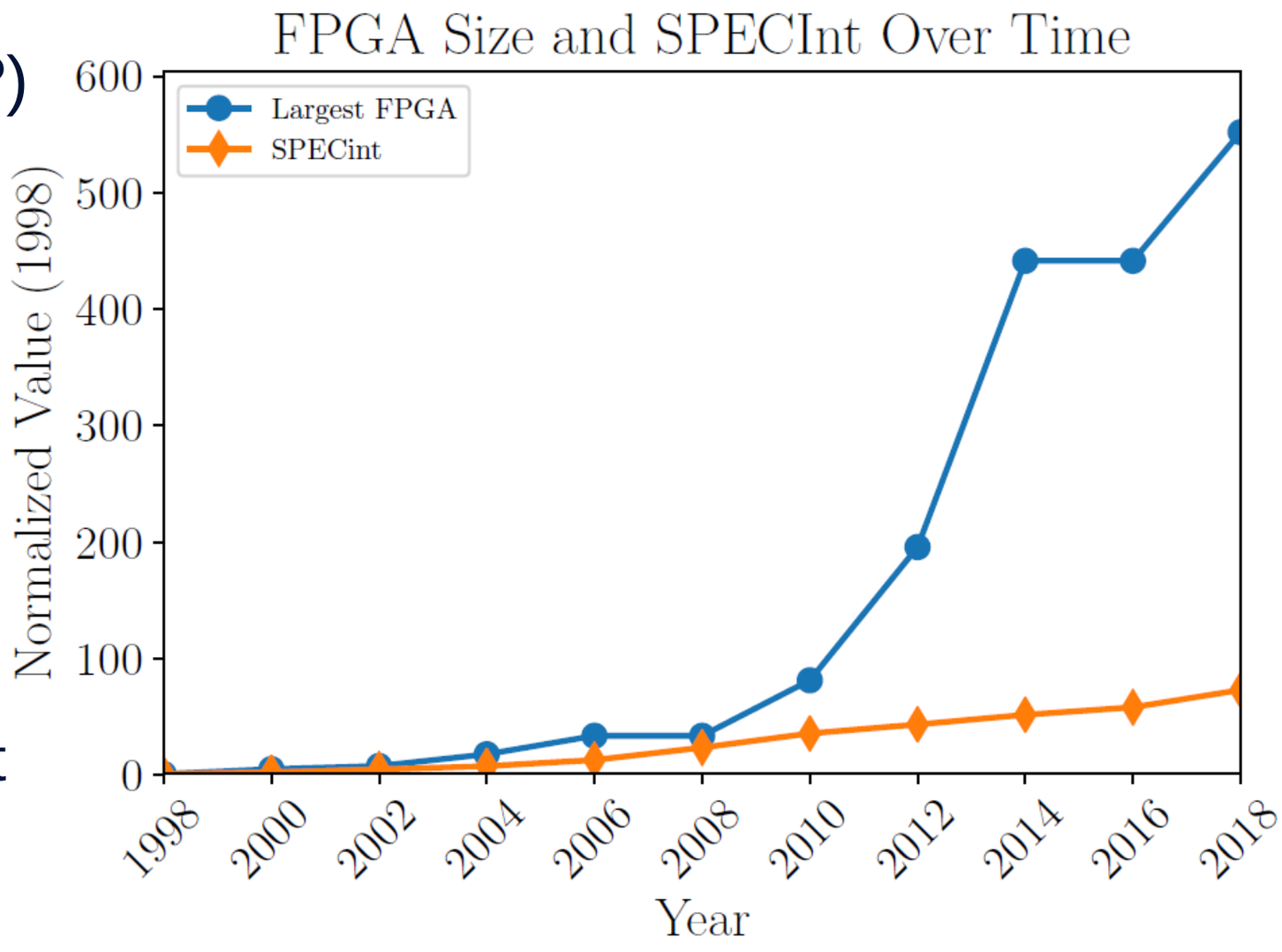
Design Flow Pressures on STA Run-Time

- More clock-domains (10s, 100s?)
- More timing corners (1, 2, 4, 8?)
- Increasing design size
- Limited single-threaded performance gains
- Increasing CAD flow parallelization
  - Ahmdal's law: 4x speed-up limit at 25% STA!



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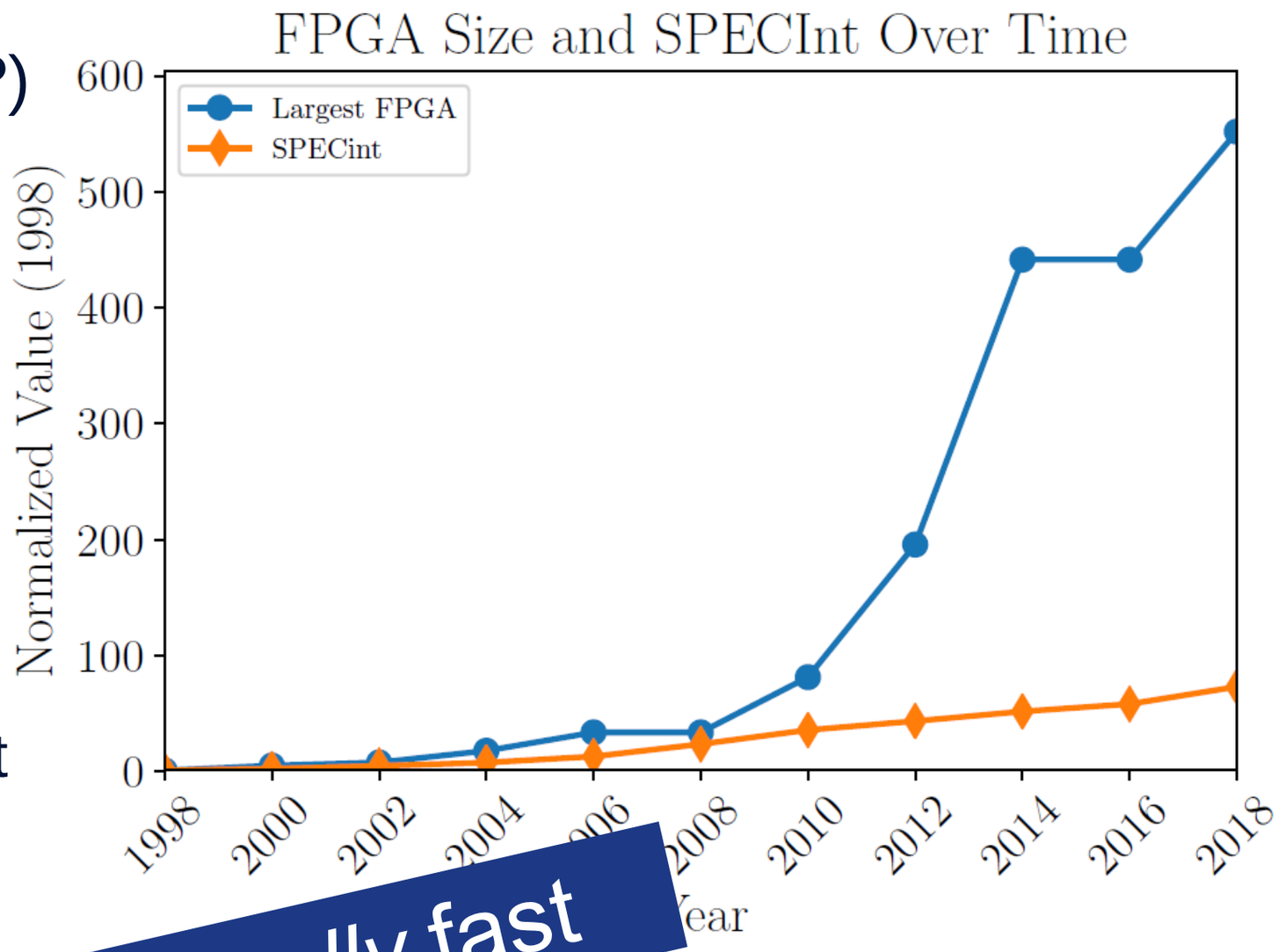

STA must be really fast

How to Speed-Up STA?

Algorithmic Improvements?

- **Bad News:** Already linear time!

STA has low Arithmetic Intensity:

- Lots of memory access (edges, nodes, times)
- Limited computation (SUM, MAX)
- Try to maximize data re-use!
  - *Efficient data structures*
  - *Single set of traversals for:*
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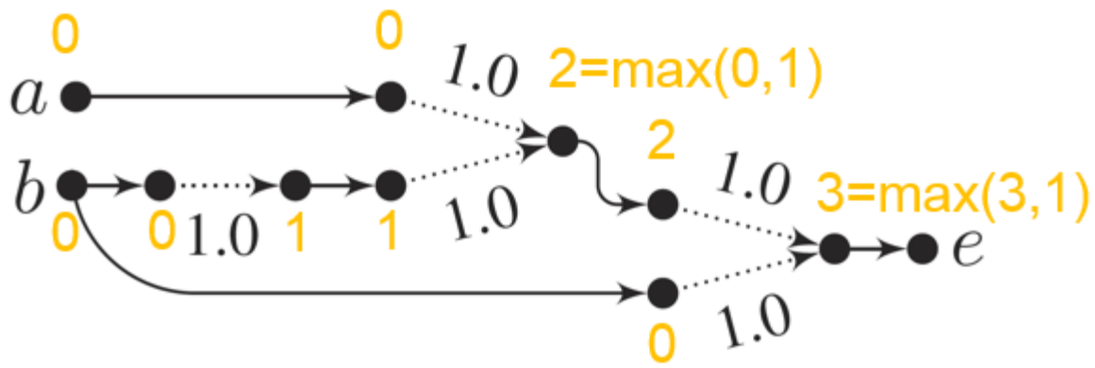
    - *Setup & Hold Analysis*



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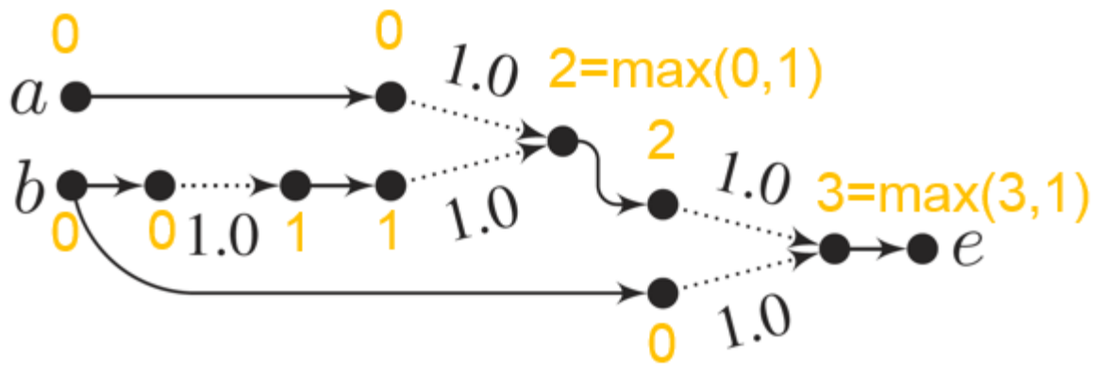
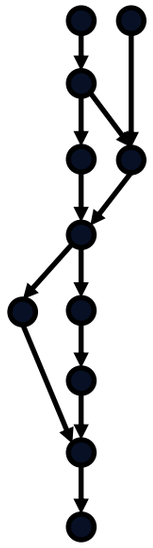


Parallel STA?

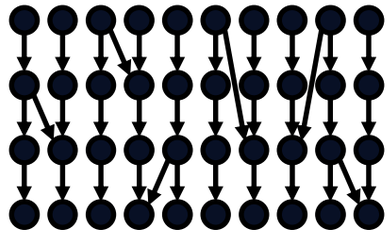
STA Parallelization

STA Parallelization Challenges

- Dependency Structure
  - Timing Graph defines dependencies
  - Must be respected in parallelization



High Logic Depth



Deeply Pipelined

- Low Arithmetic Intensity

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Low Overhead Parallelization

Parallel Platforms

GPU?

CPU?

GPU Parallelization

	Speed-Up
Kernel	6.2x
Overall	0.9x

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Data Transfer Limits GPU Speed-up!

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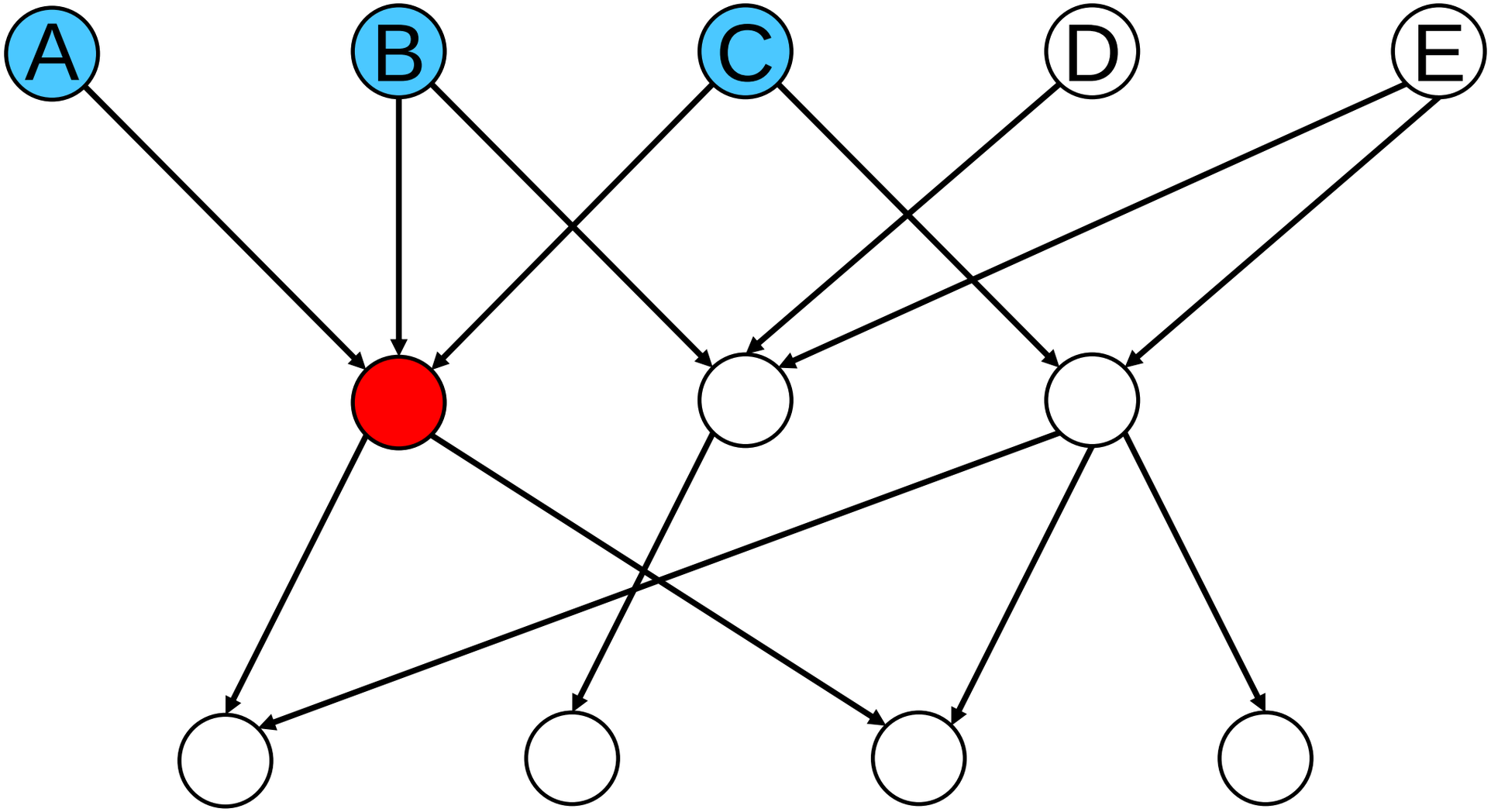
Data Transfer Limits GPU Speed-up!

- Compute: O(V+E)
- Data: O(V+E)

CPU Parallelization I

- **Push** Arrival Time from Source to Sink



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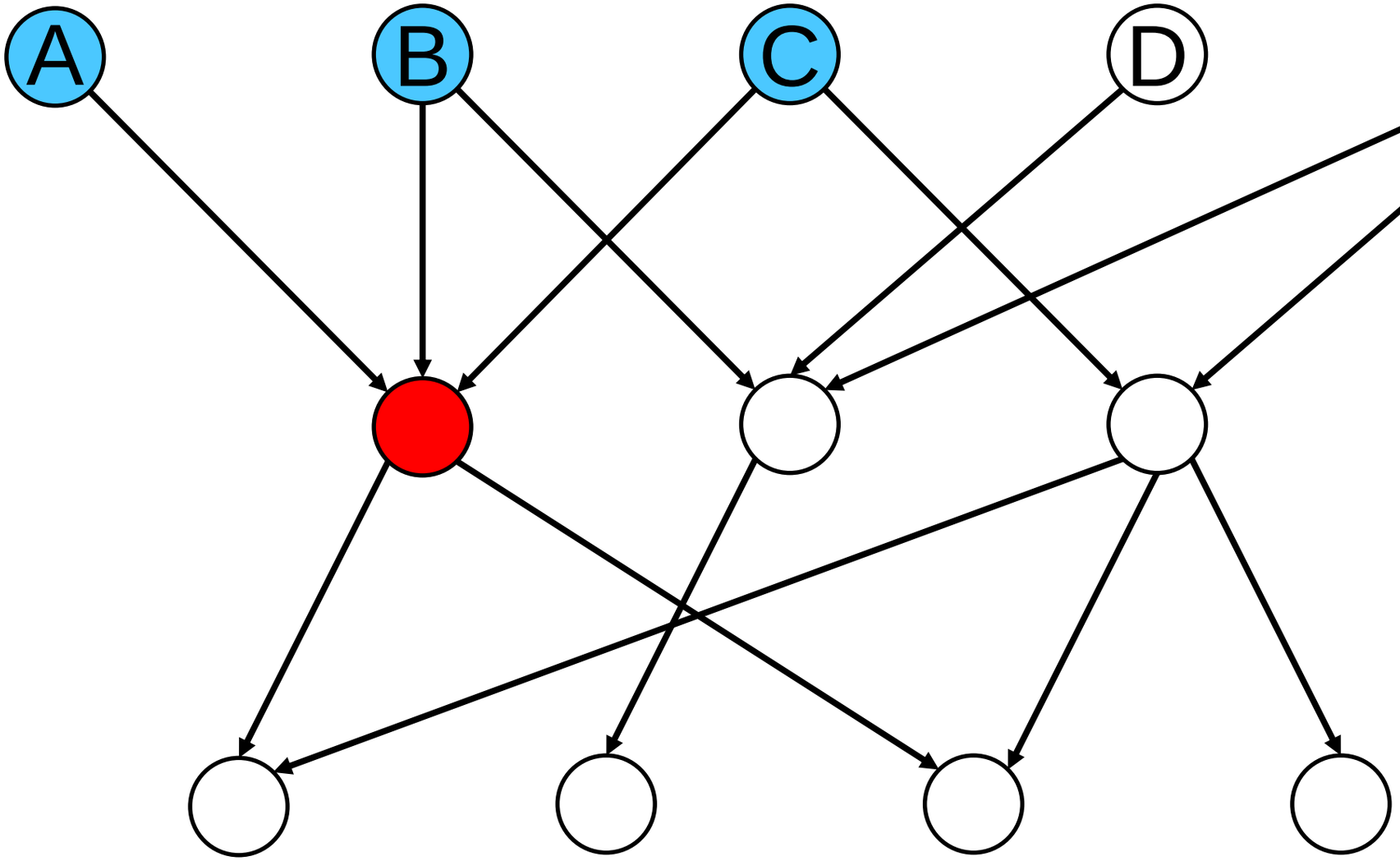

Multiple Writers!

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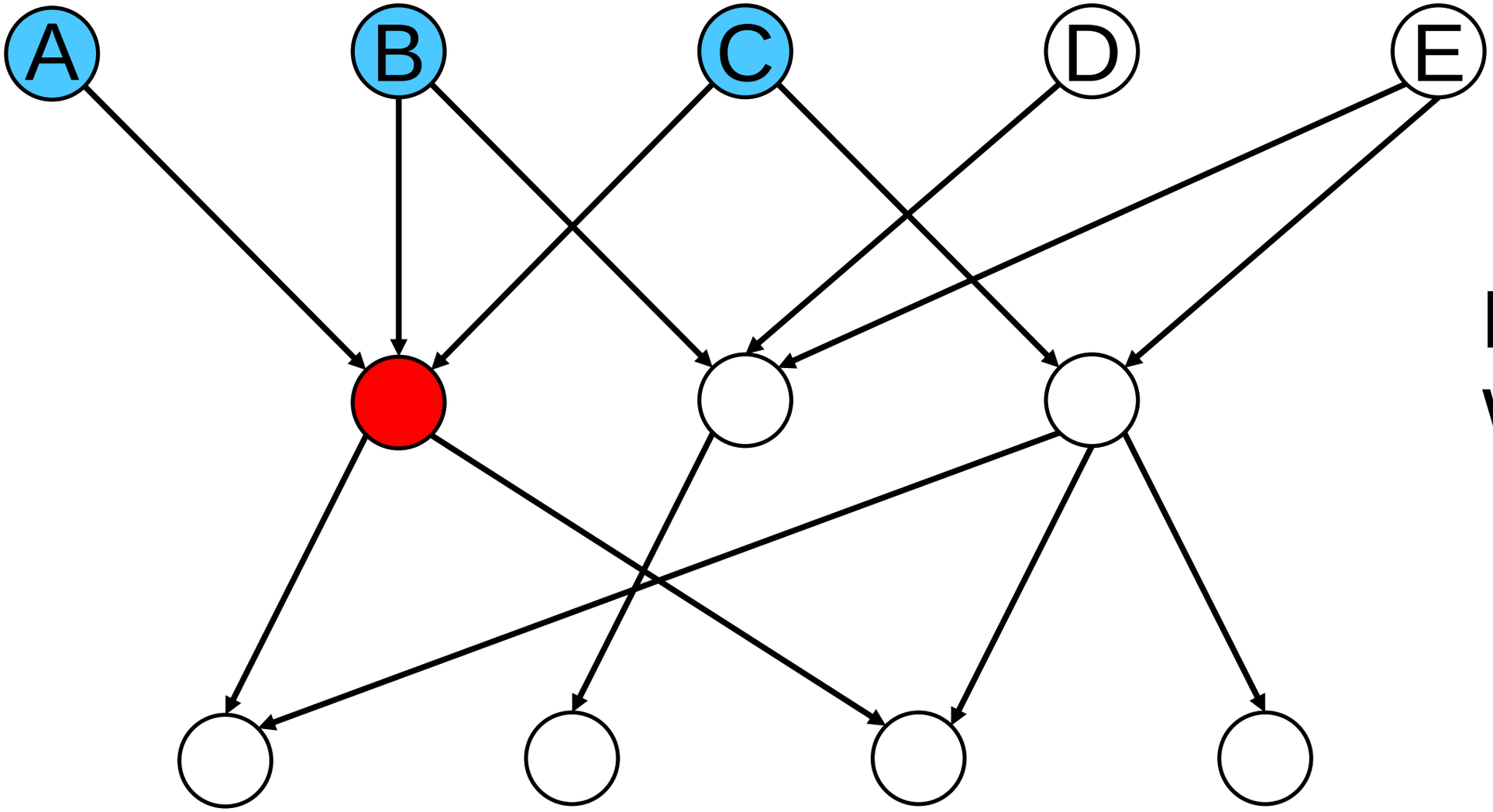

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Must use locks to synchronize

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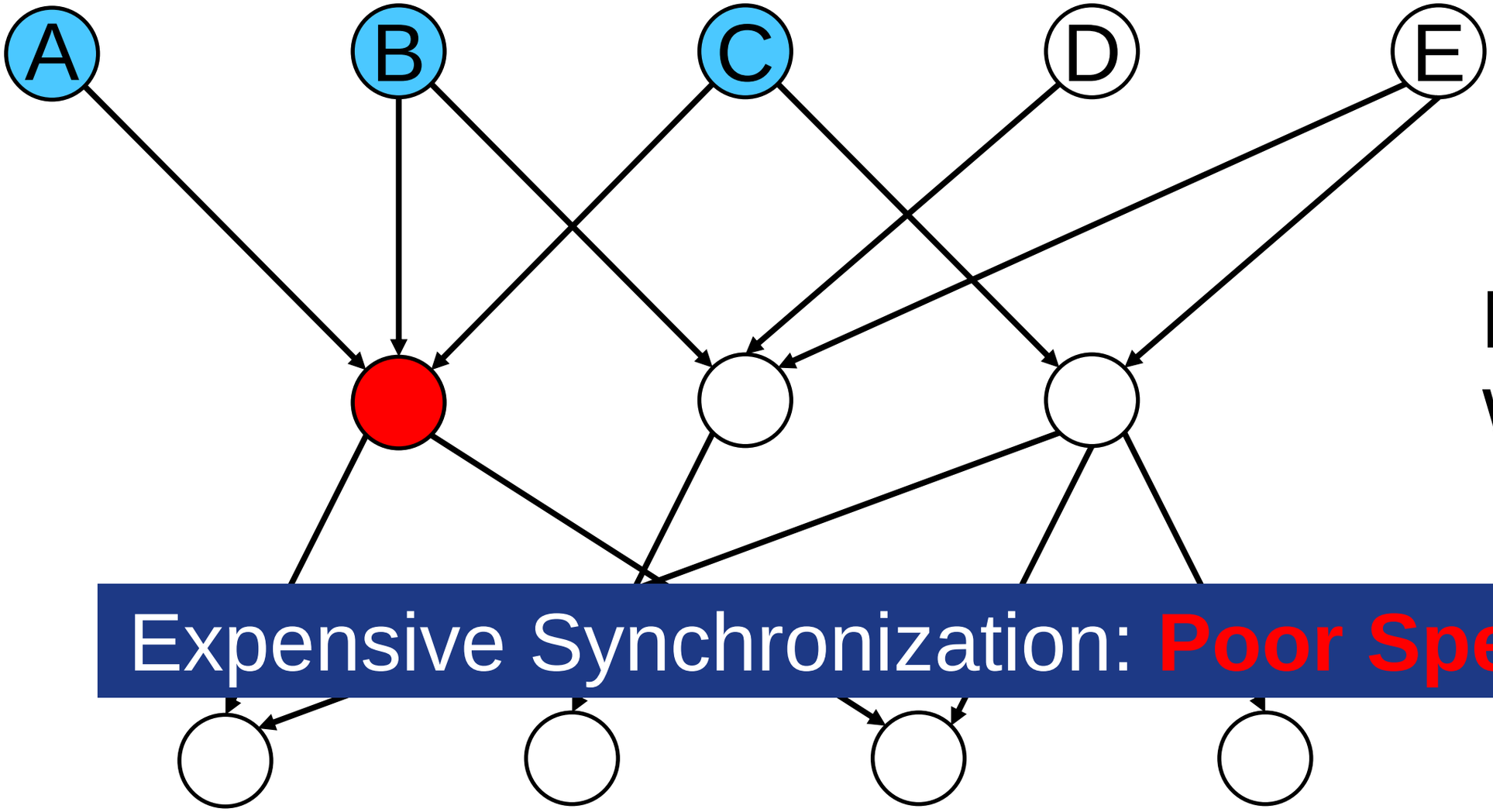


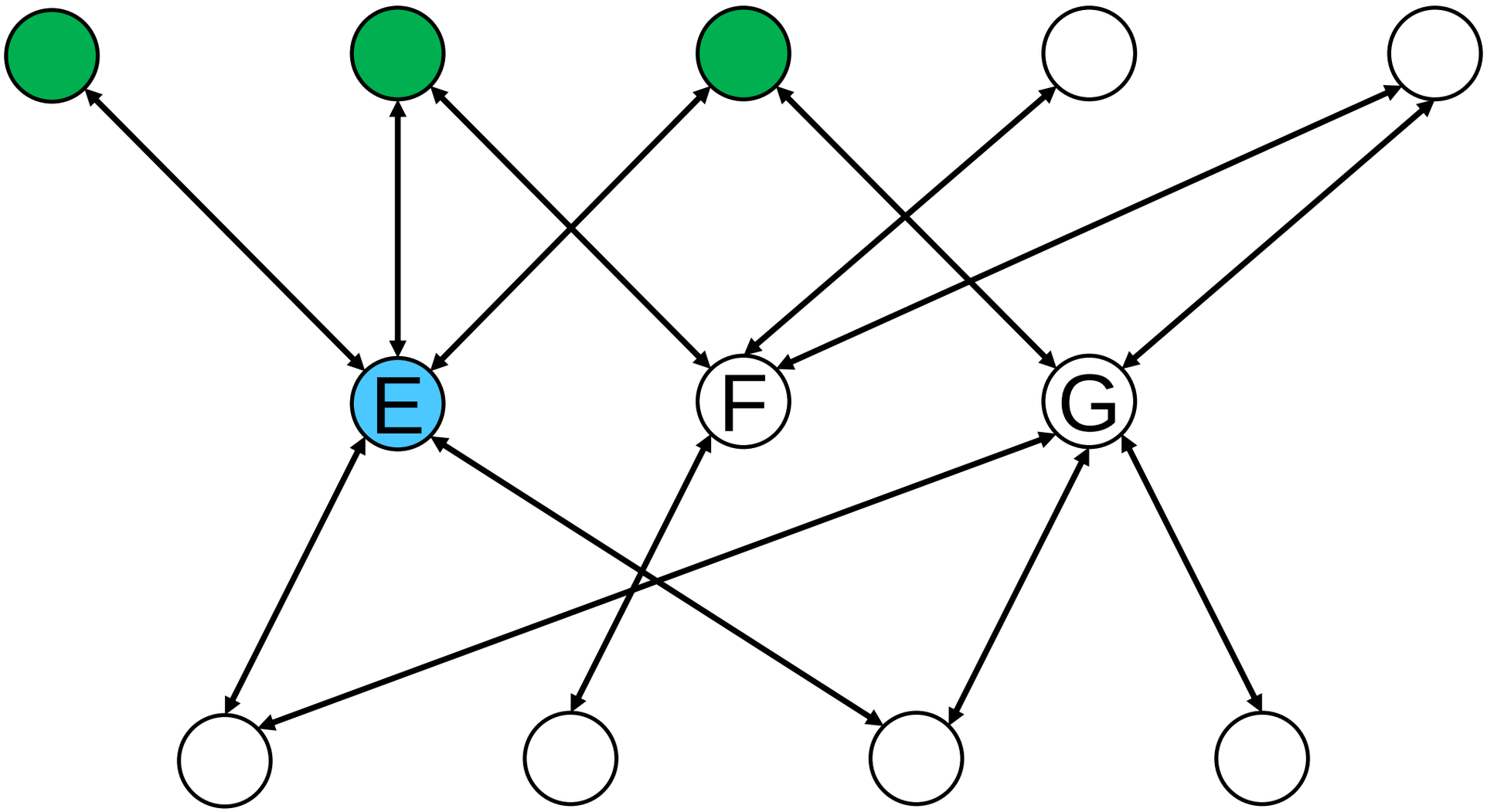
Multiple Writers!

Expensive Synchronization: **Poor Speed-Up**

Must use locks to synchronize

CPU Parallelization II

- **Pull** arrival times from Sources
- Requires bi-directional edges



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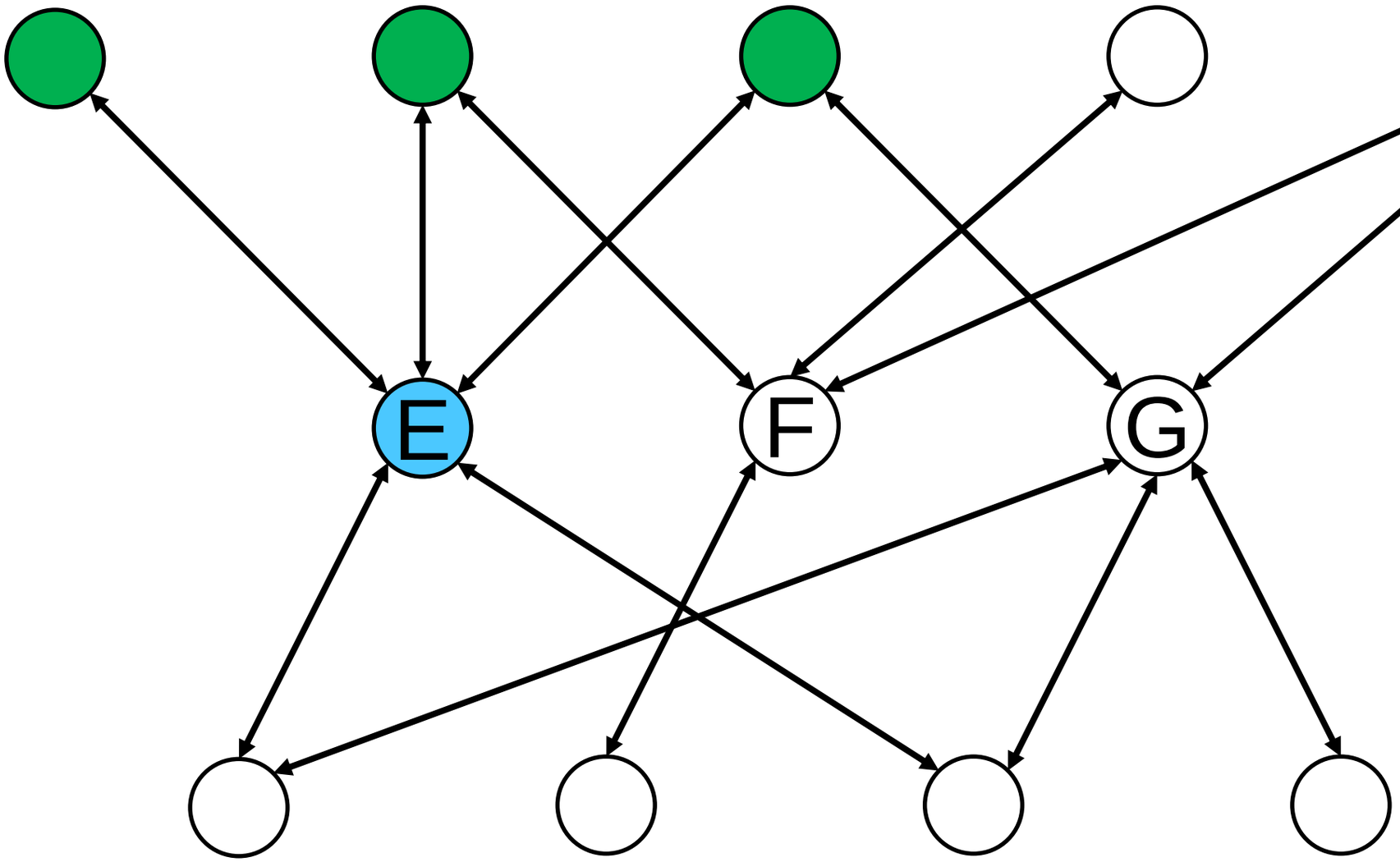

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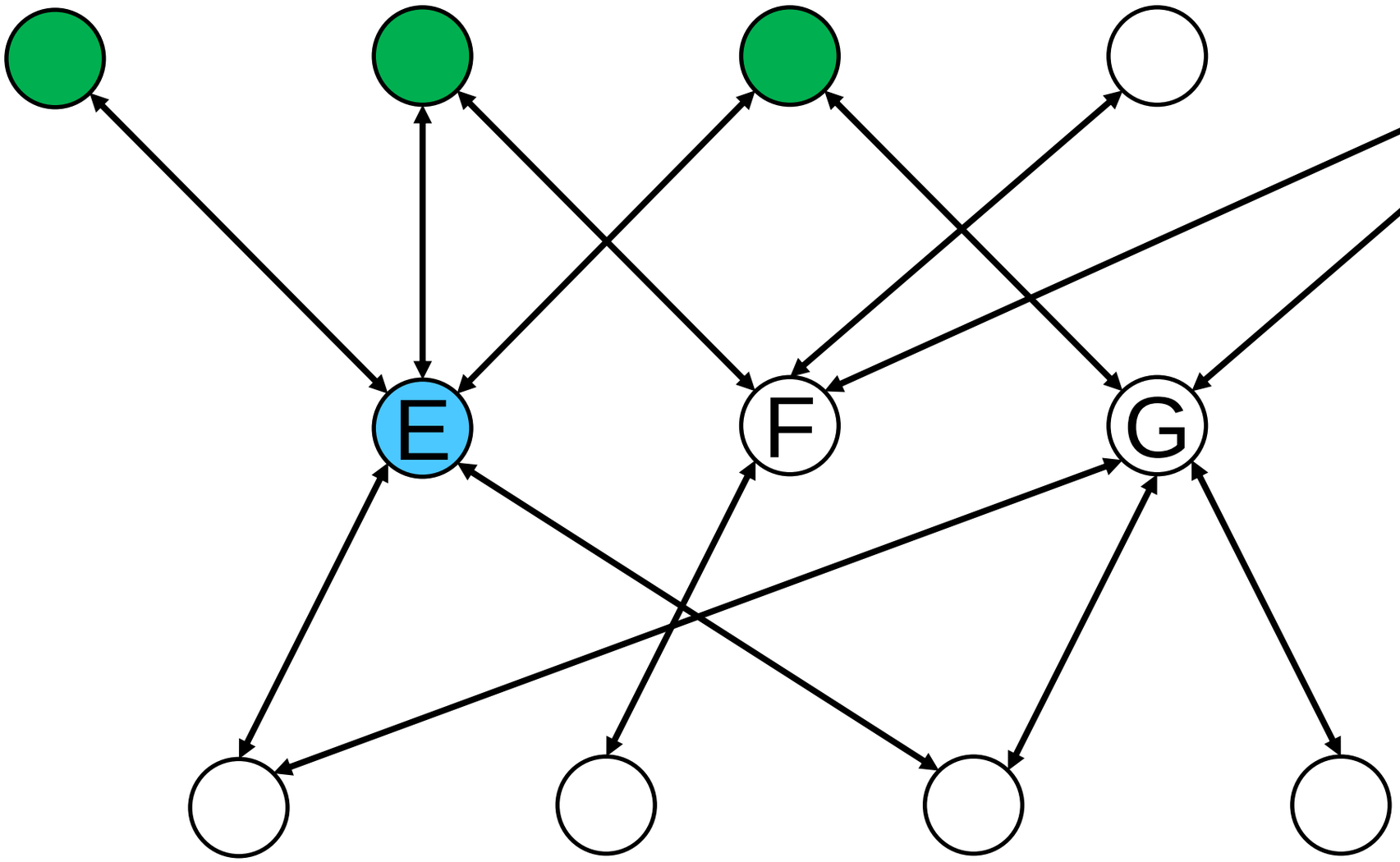

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No Locks!

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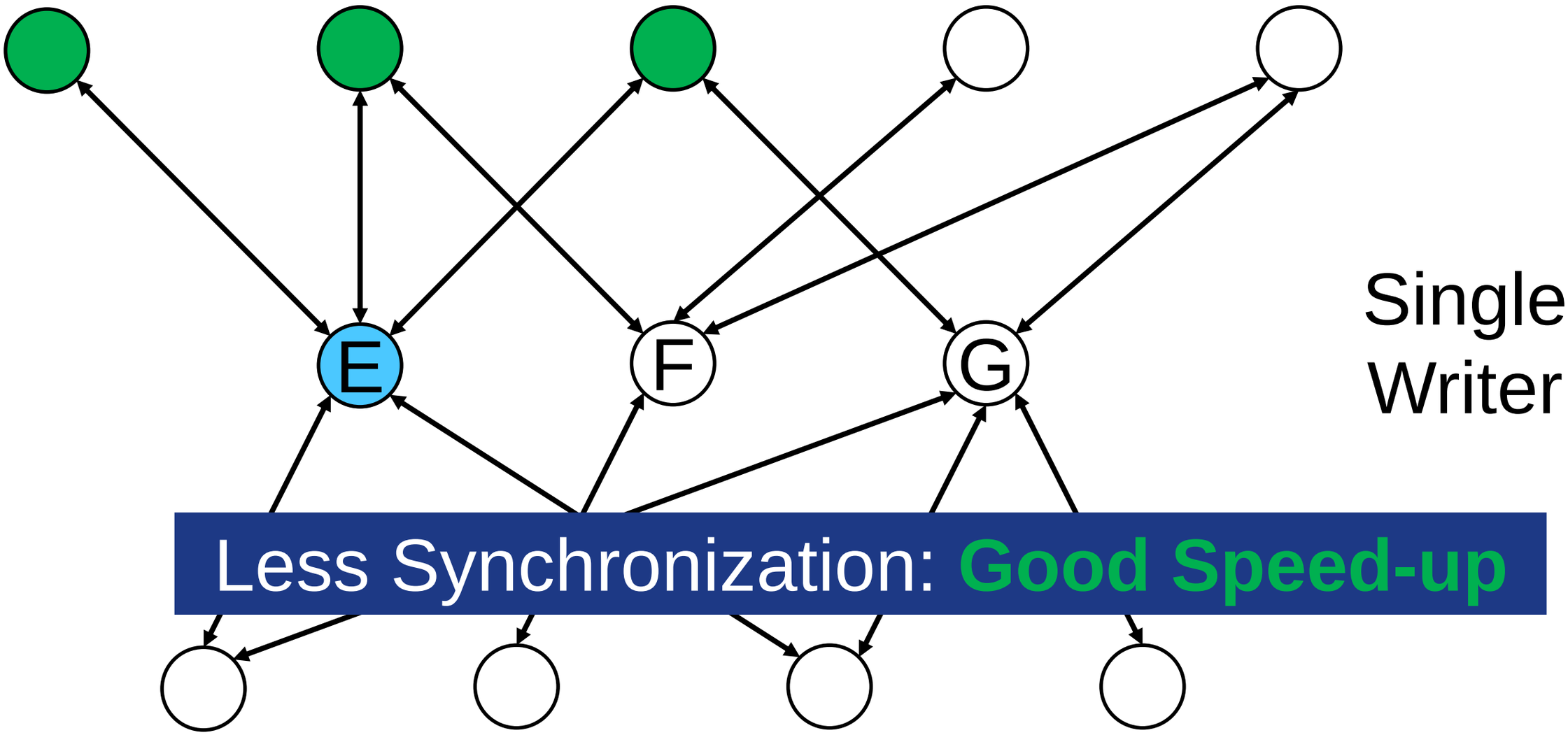

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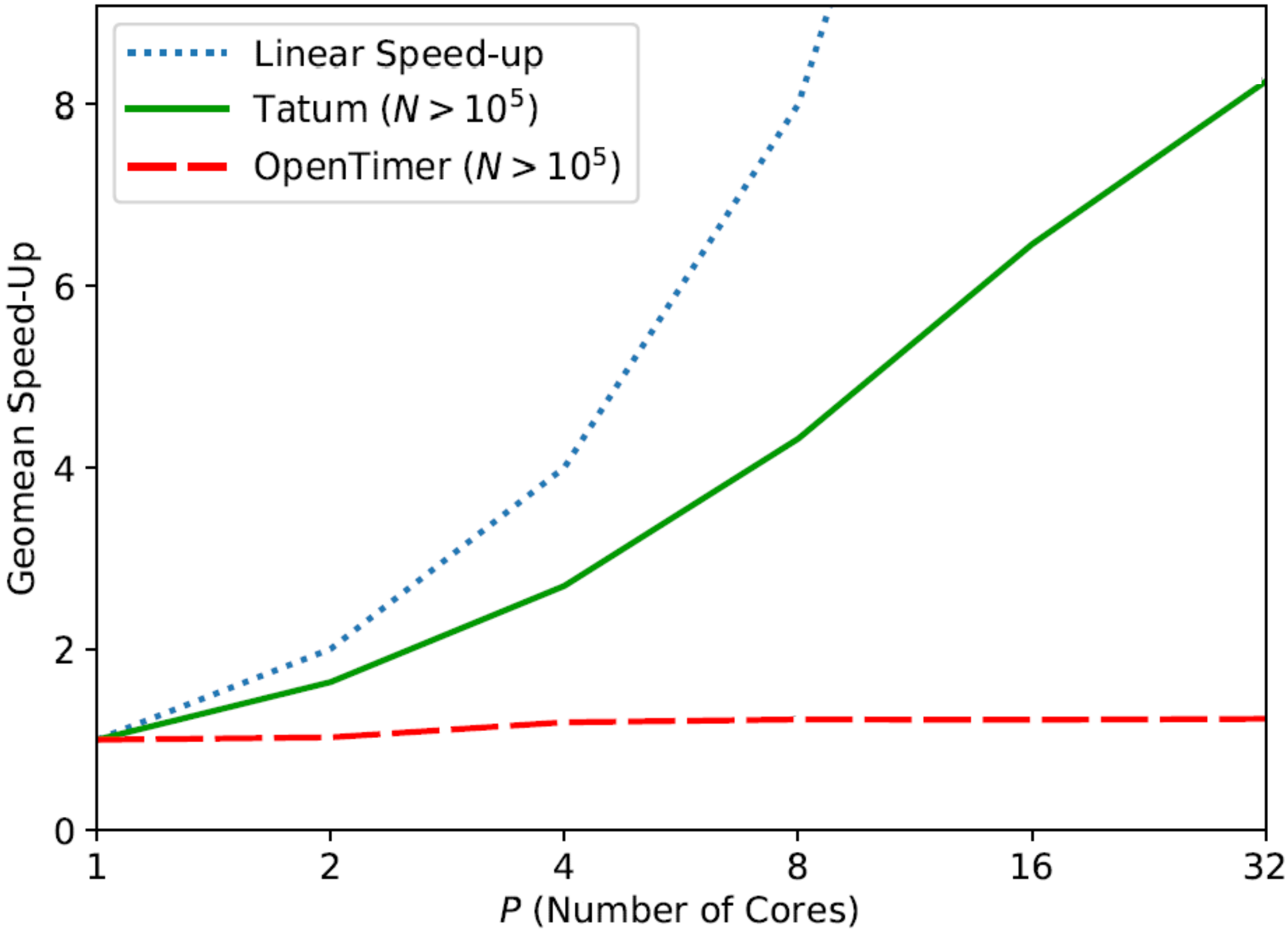
Performance Results

Tatum STA Performance: Tau'15 ASIC Benchmarks

- Self-relative speed-up



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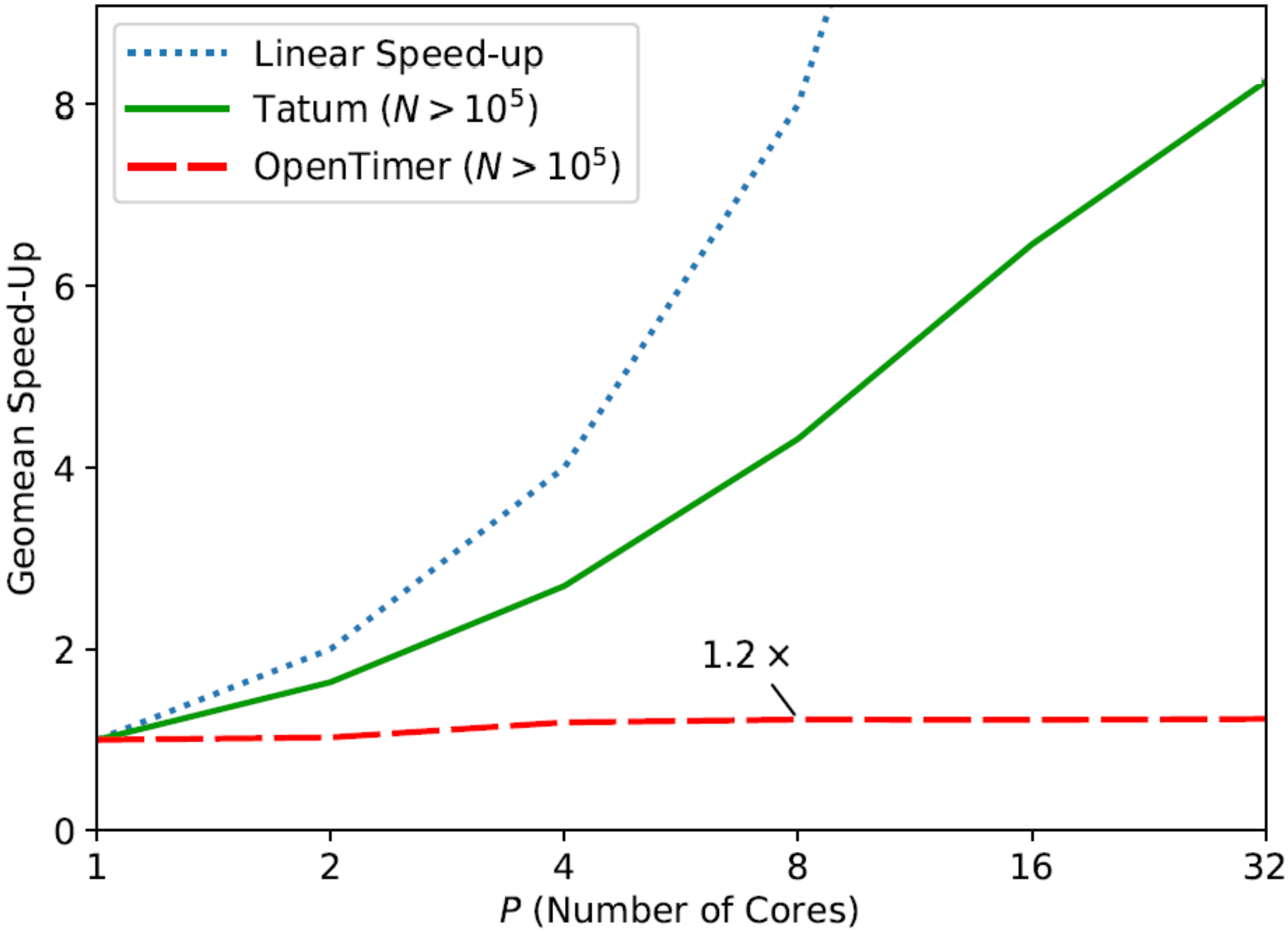

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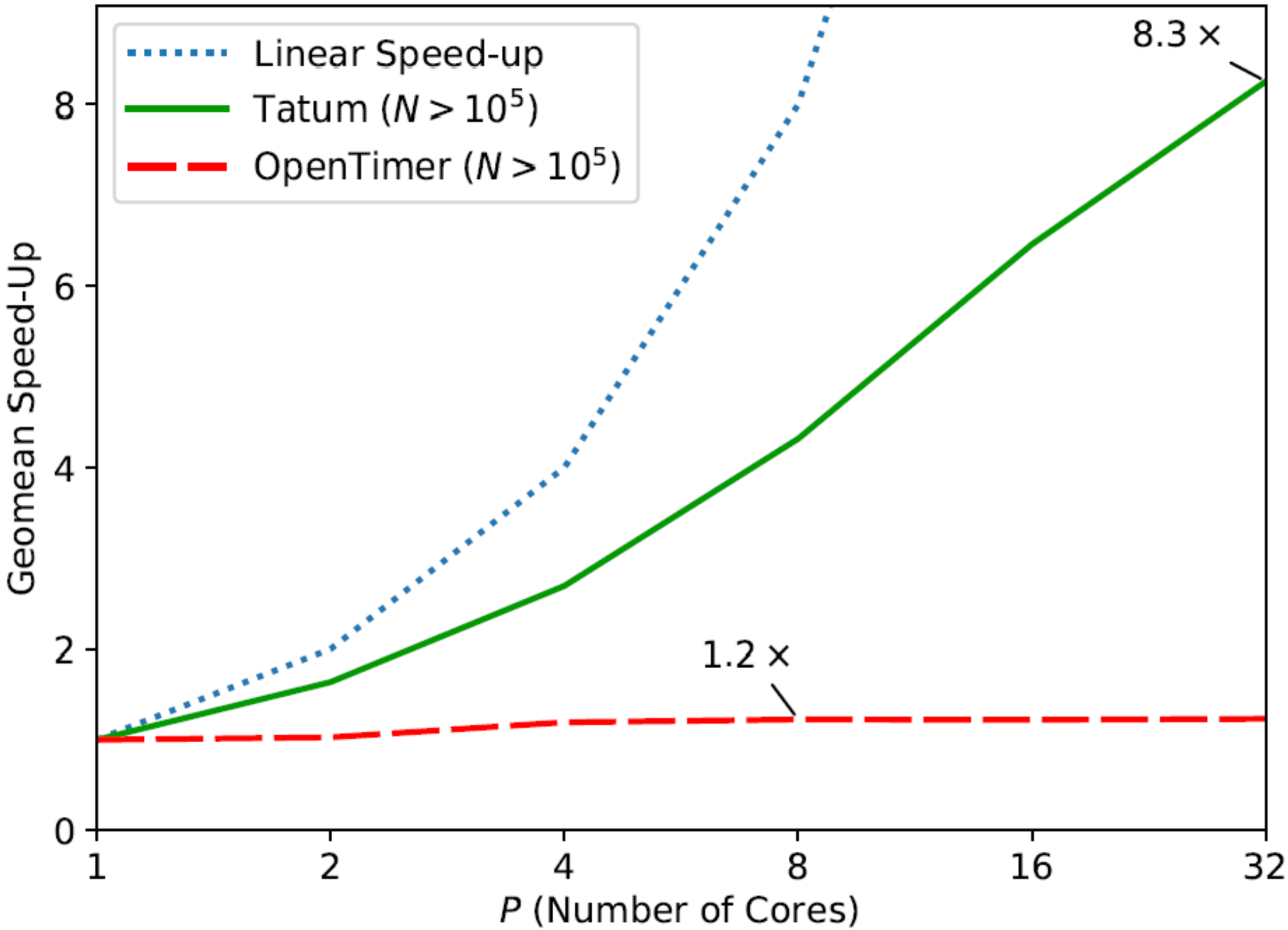
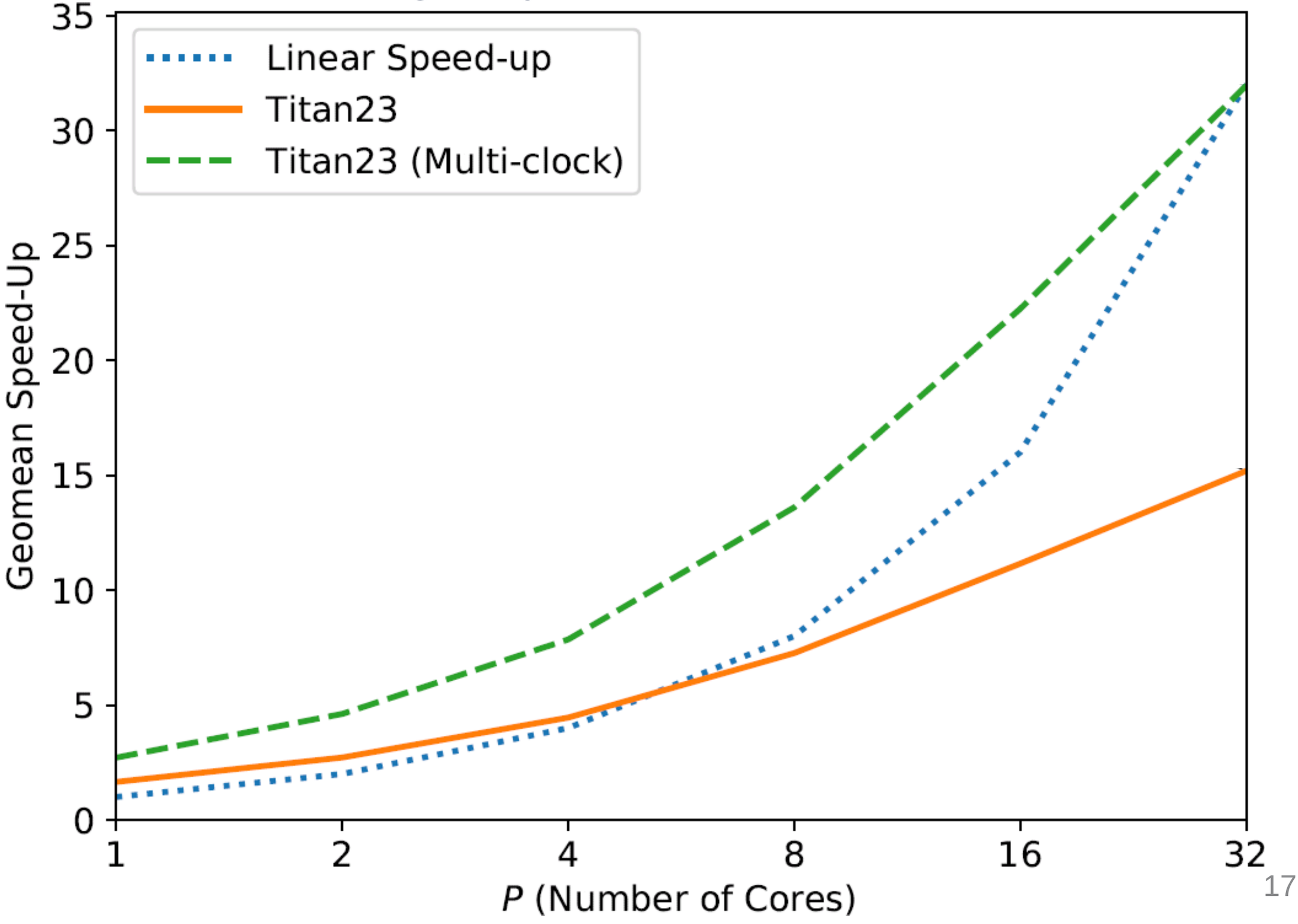


Tatum STA Performance: Titan Benchmarks

- Relative to VPR 7 timing analyzer



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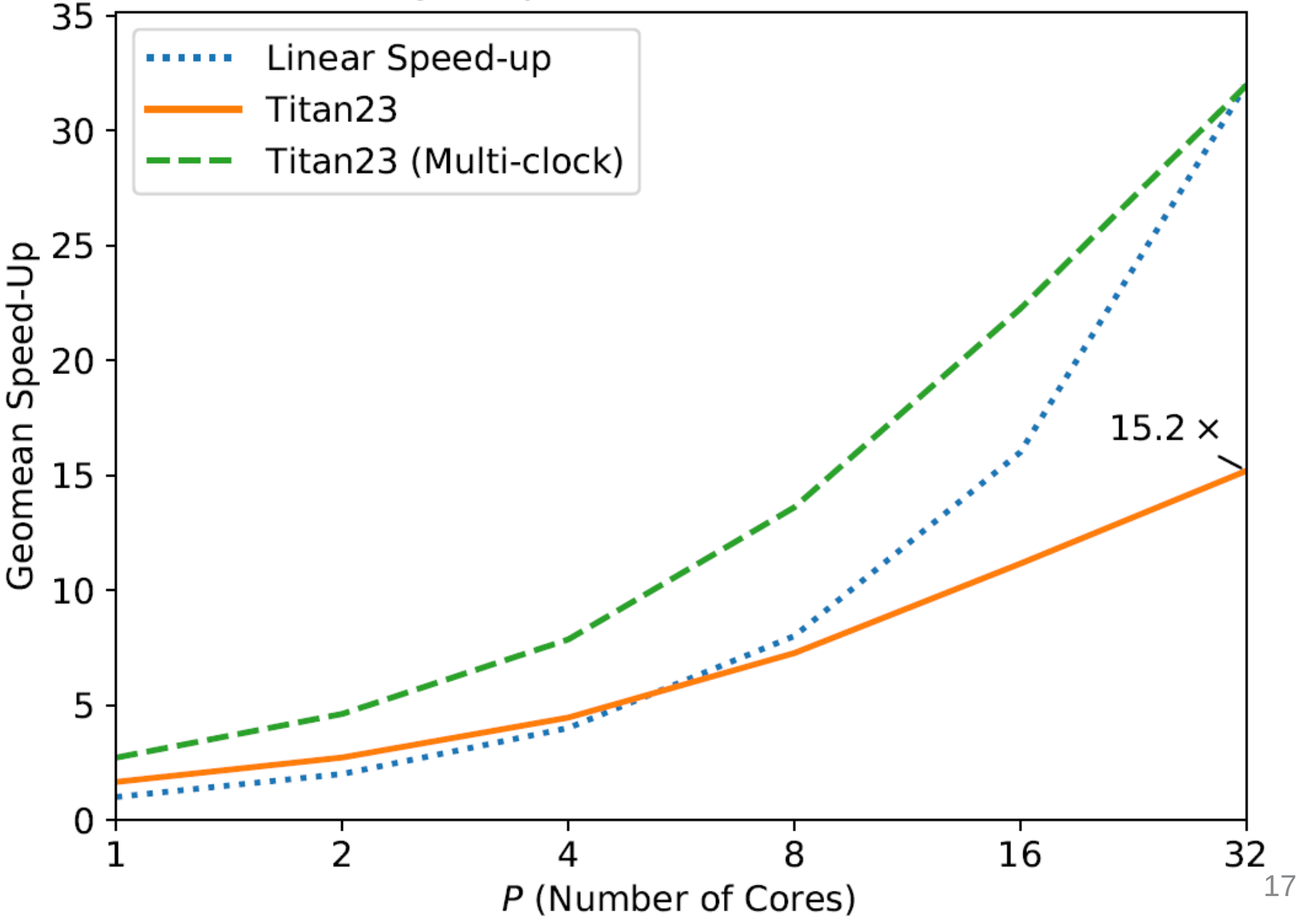

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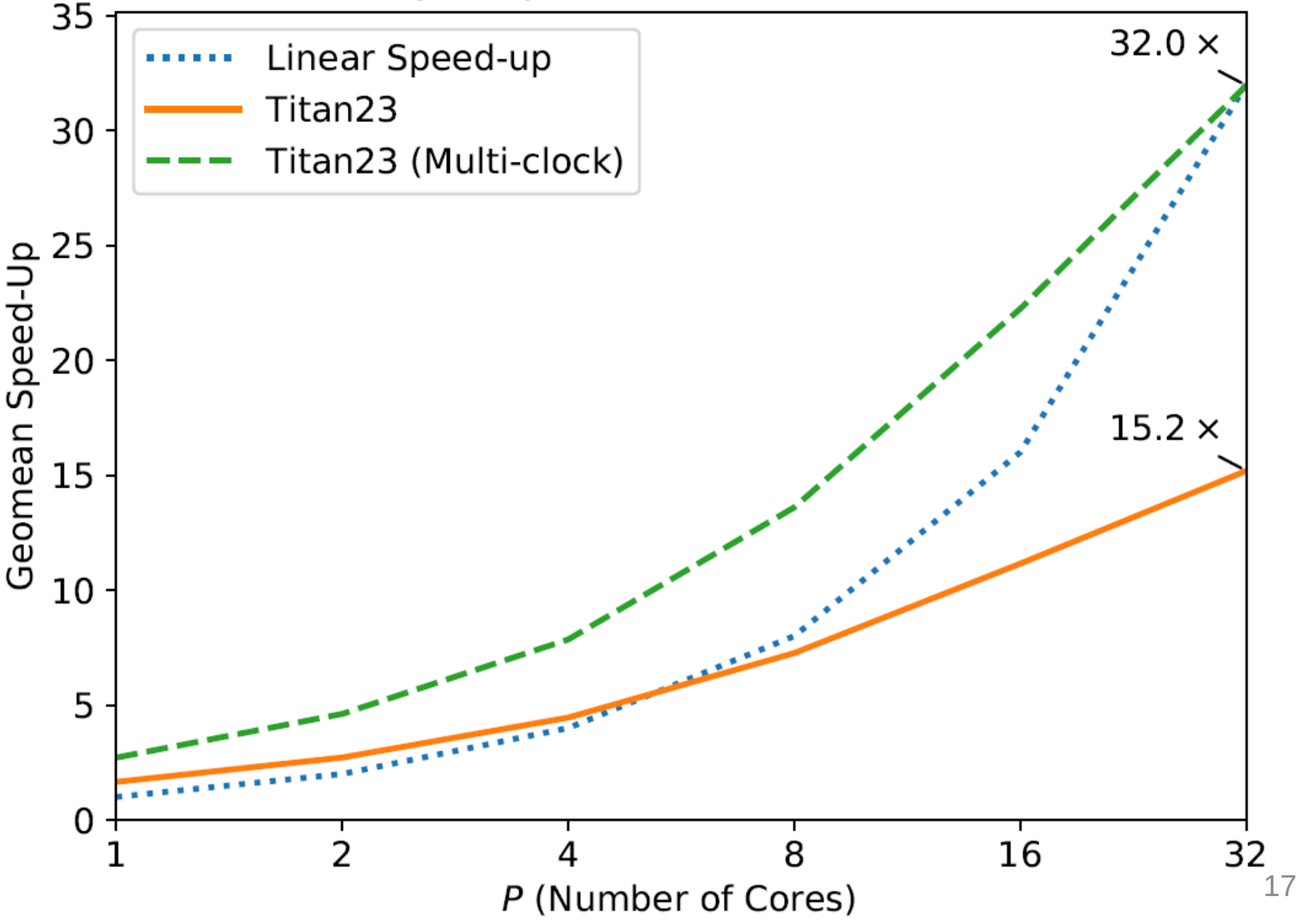
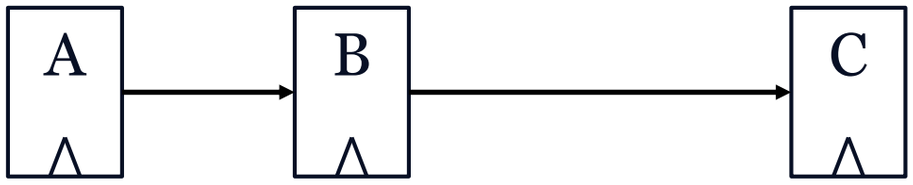


Improving Optimization

Placement Critical Path Optimization



Up-to-date
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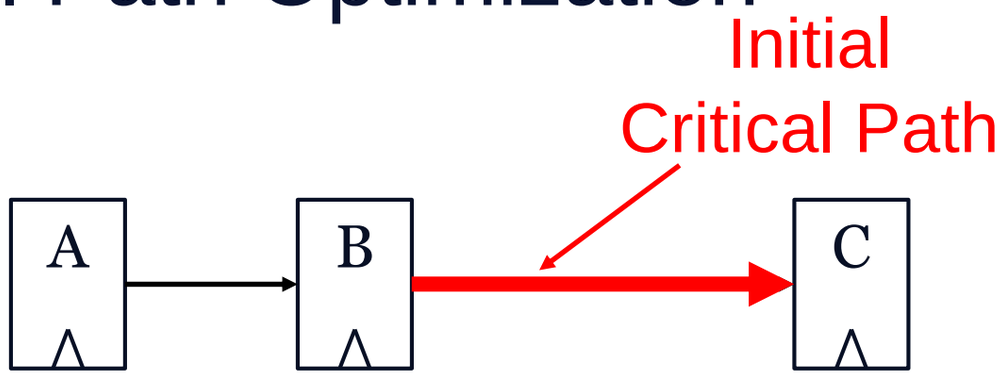

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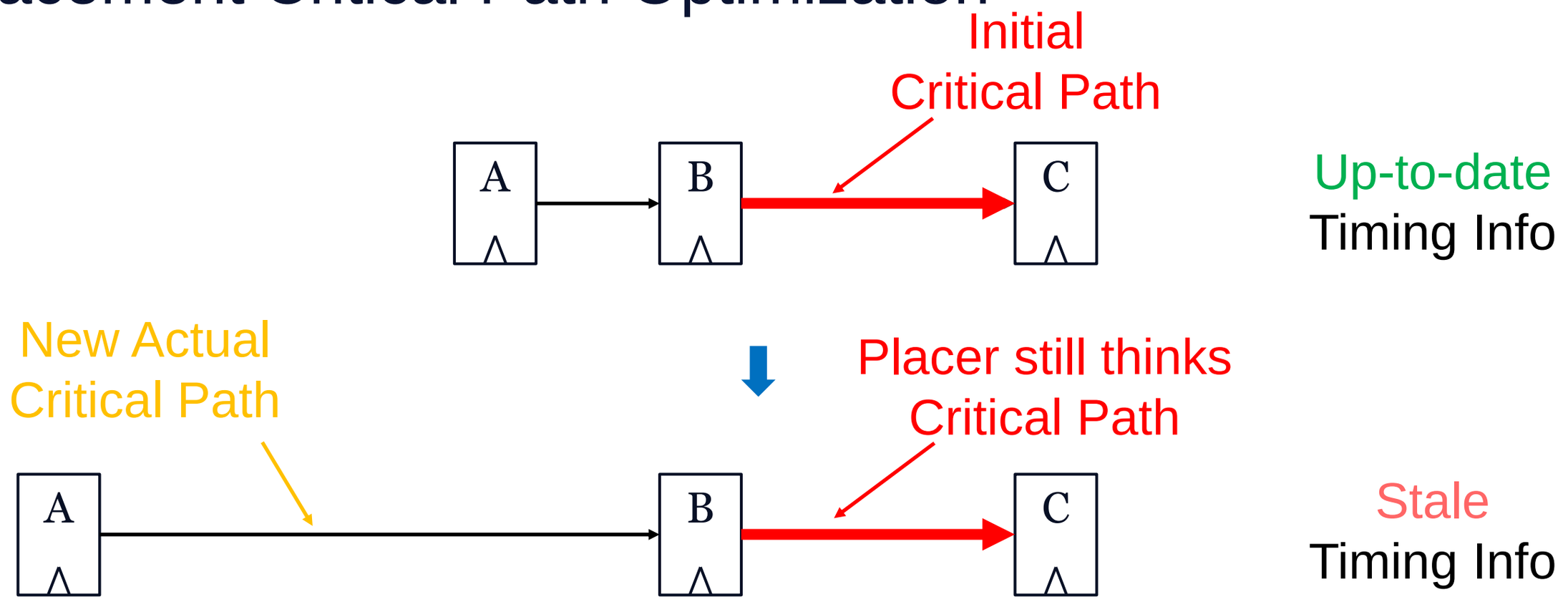

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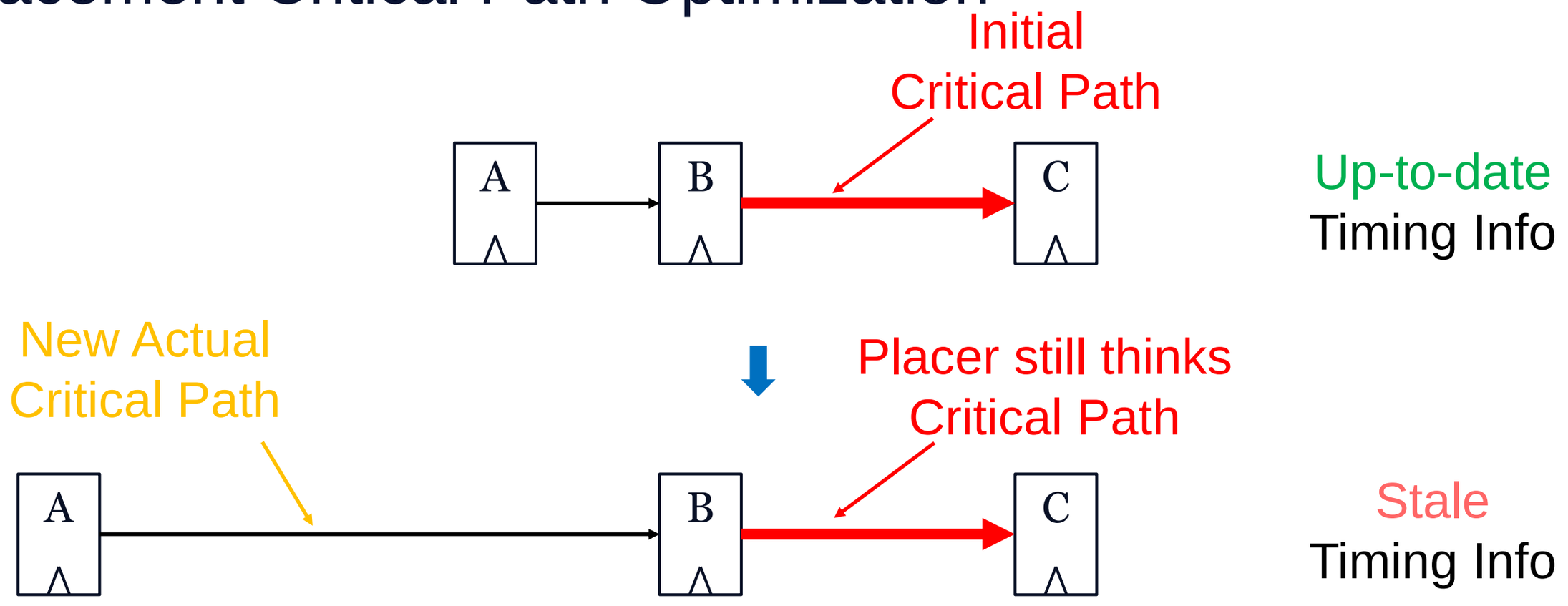

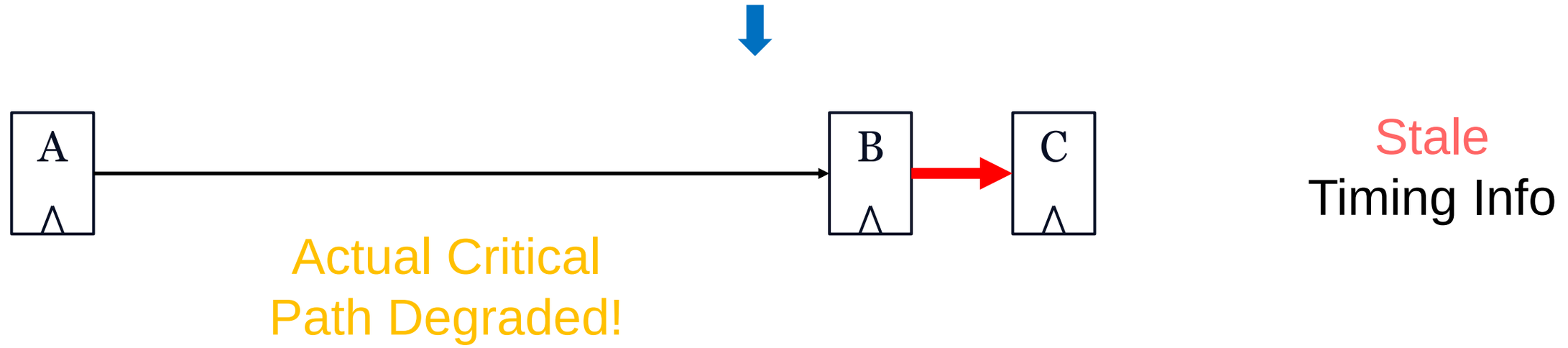

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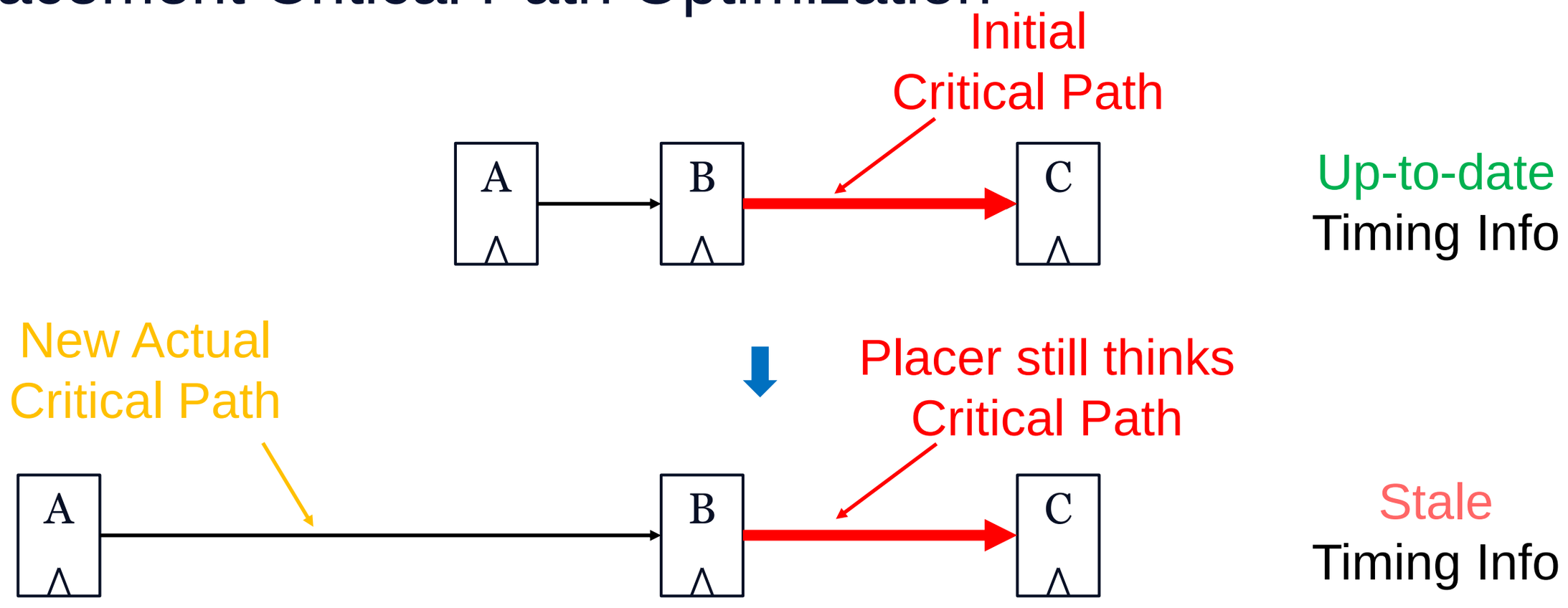

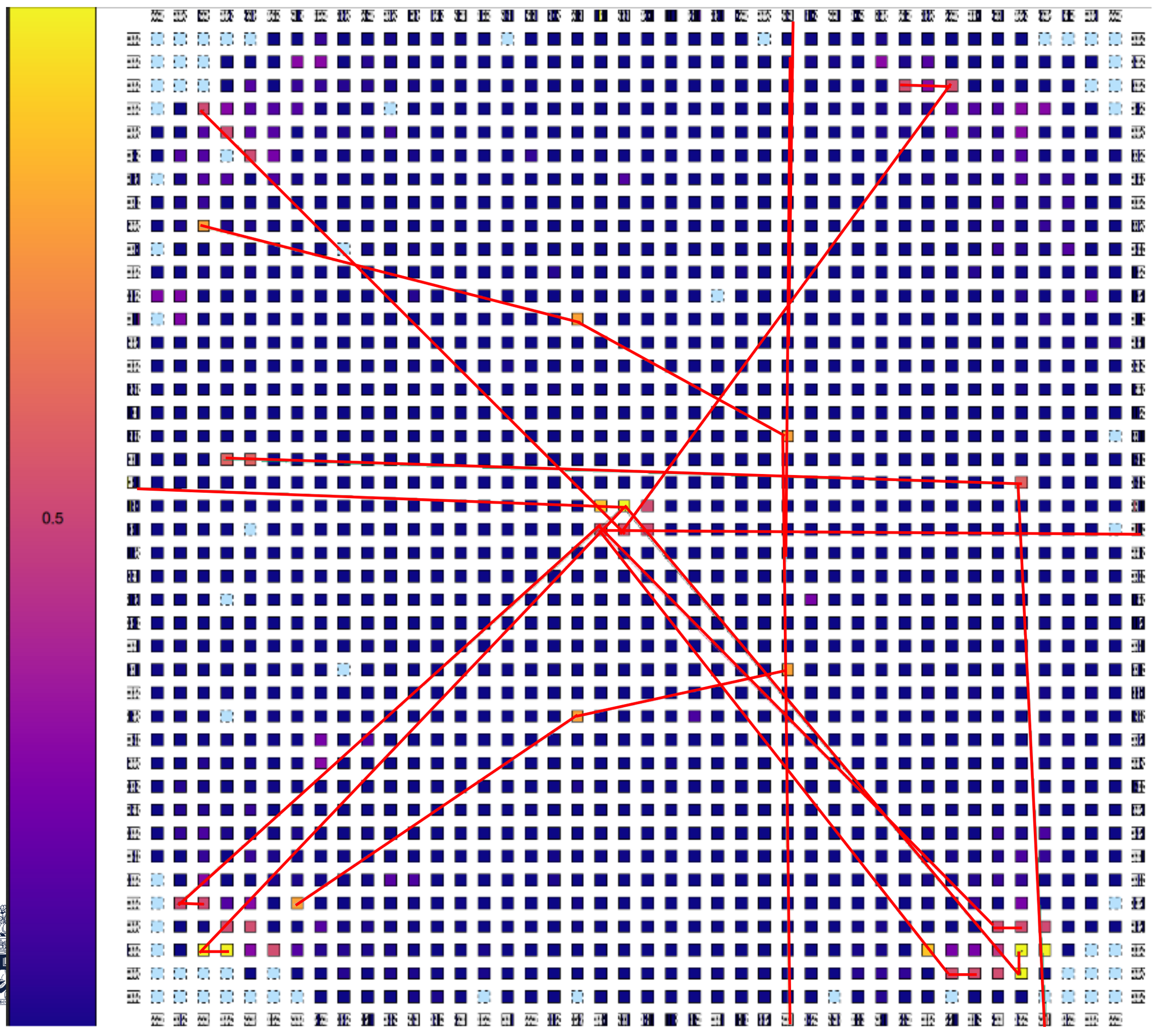
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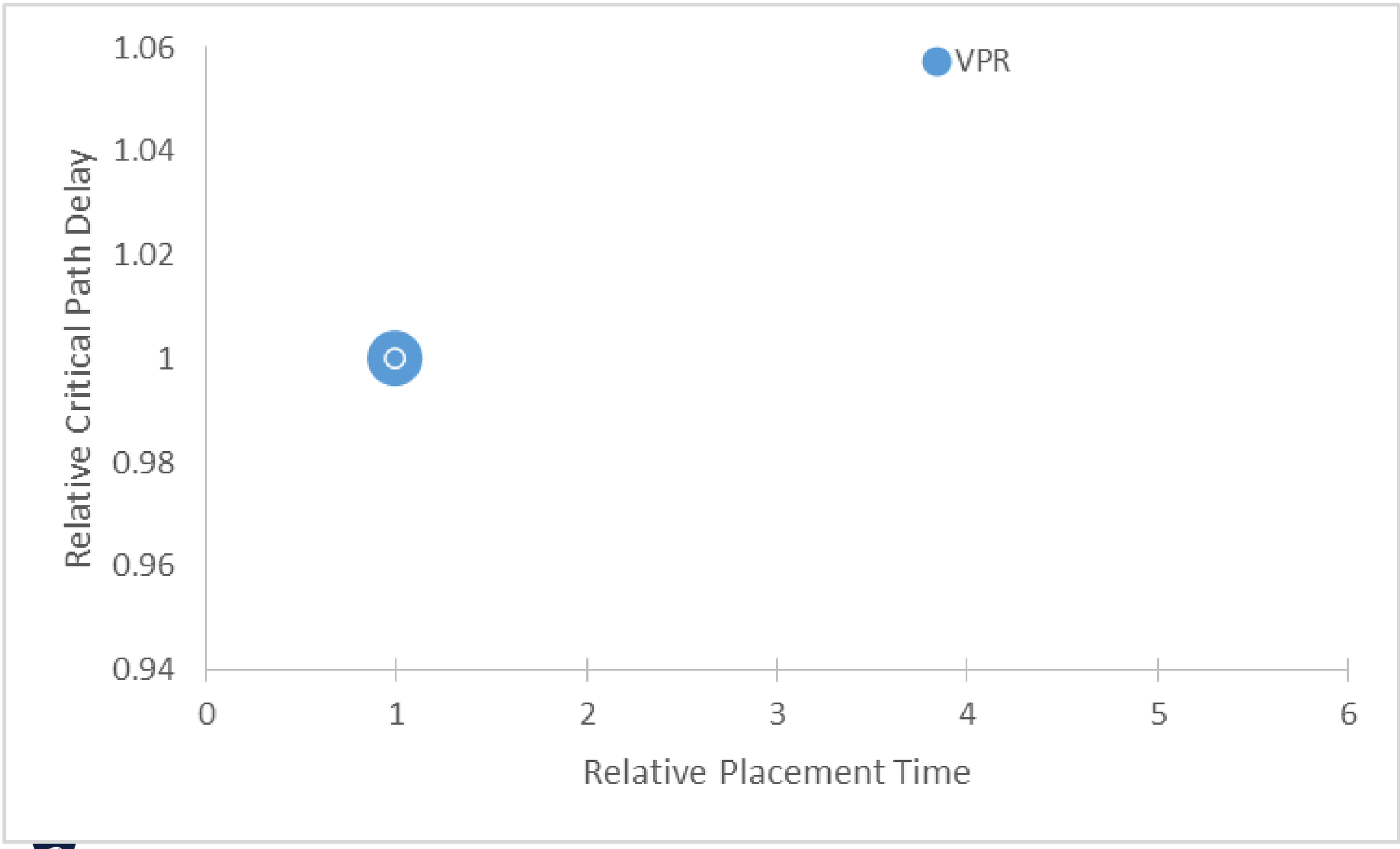
VPR Placement & STA Frequency



VPR Placement & STA Frequency

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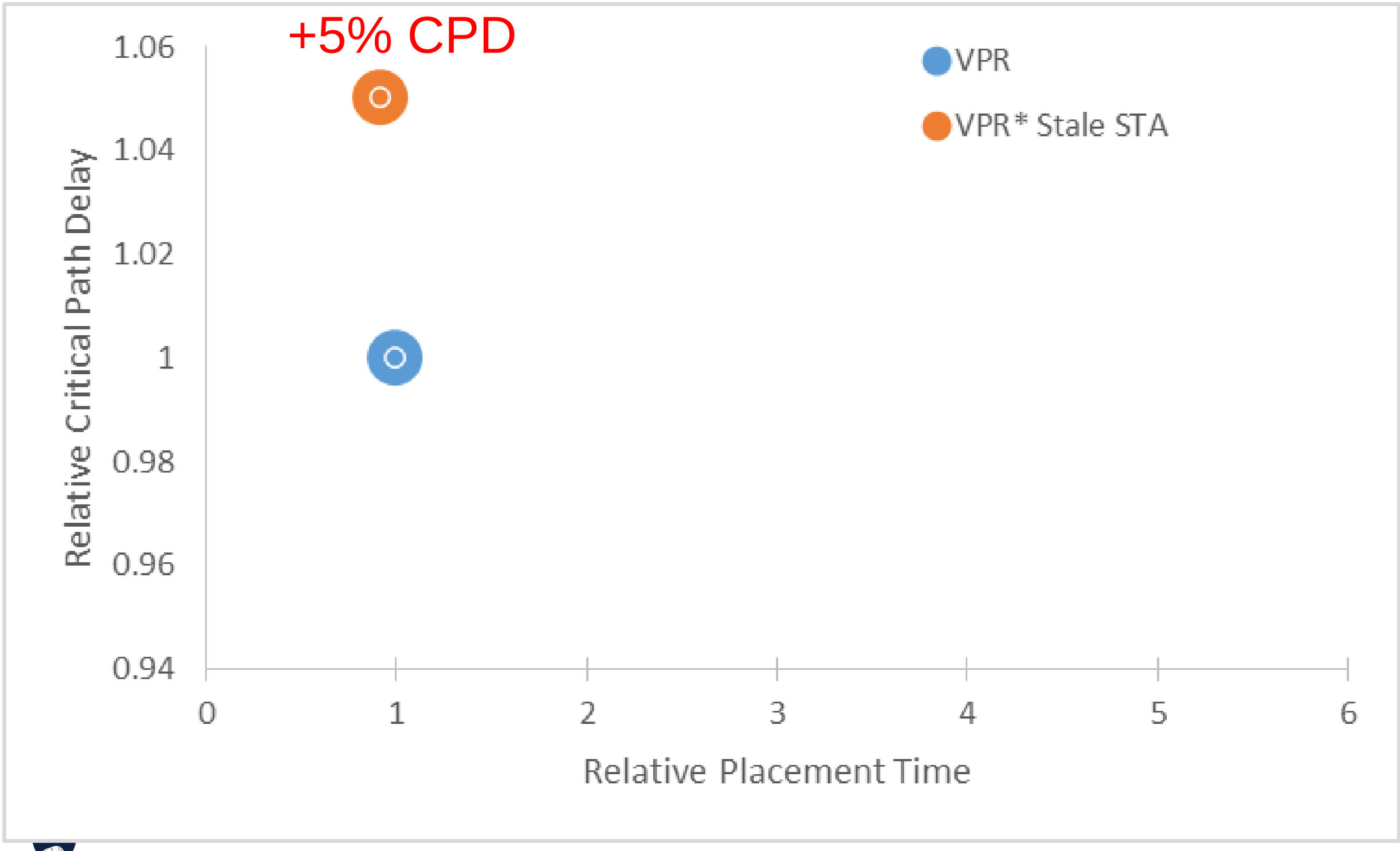

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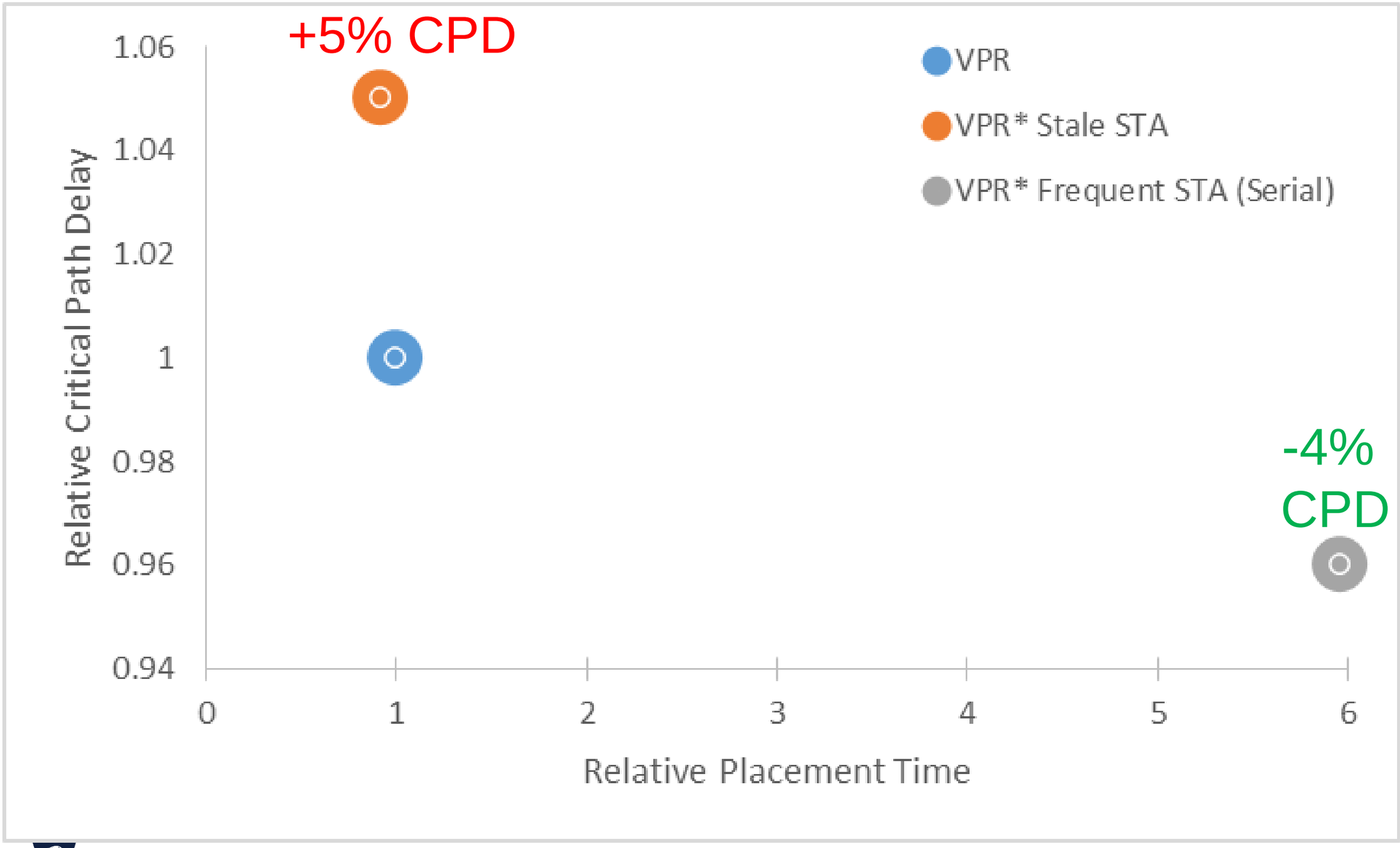

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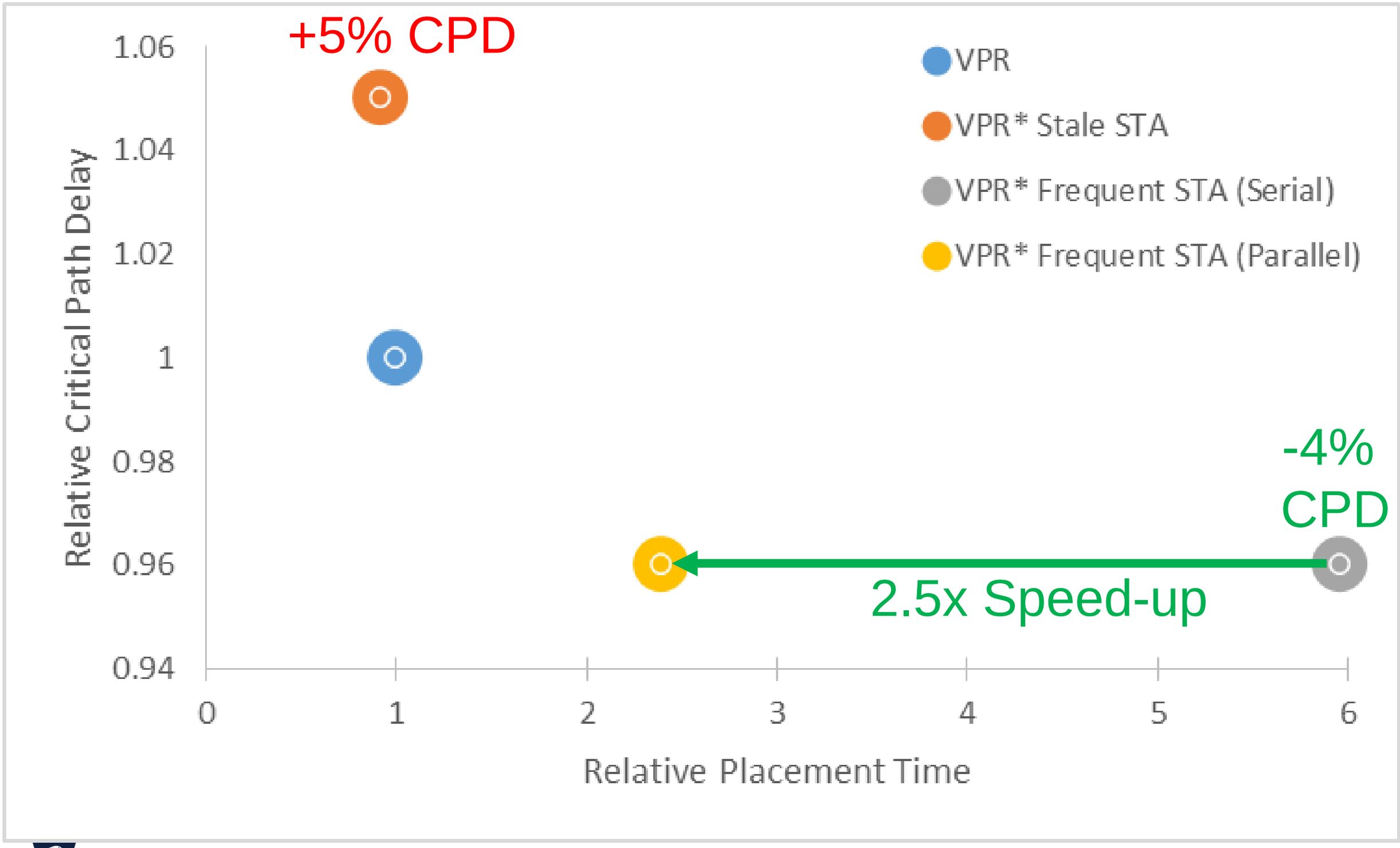

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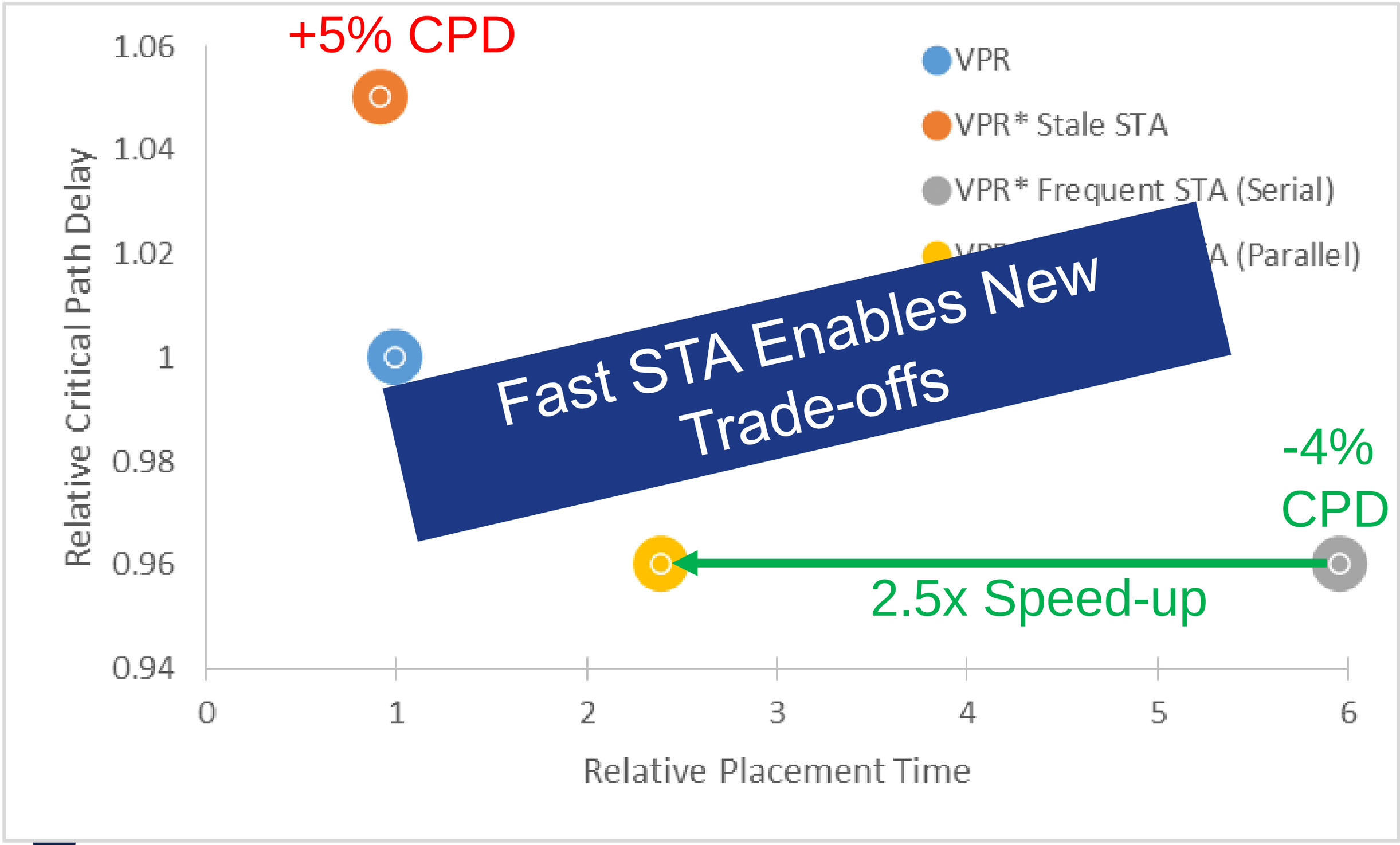

Conclusion

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- Tatum STA Engine
  - Full featured & high performance
  - **15-32x** faster than VPR 7 STA with 32 cores
  - Already used by:
    - *VTR 8*
    - *CGRA-ME*
- Fast STA enables new possibilities for timing-driven CAD
  - 4% F_{max} in late placement
  - Routing, Placement, Clustering, Synthesis, ….

Thanks!

Questions?

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Tatum Open Source Release:

uoft.me/tatum

UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE & ENGINEERING

Backup

Multi-corner STA