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From Quartus to VPR: Converting HDL to BLIF with the Titan Flow

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Motivation

- Few real benchmarks designs in academic FPGA CAD
- Missing HDL coverage and IP library

Hybrid Flow

- Quartus II performs HDL elaboration and technology mapping
- Full support for SystemVerilog, VHDL and Altera's IP Library

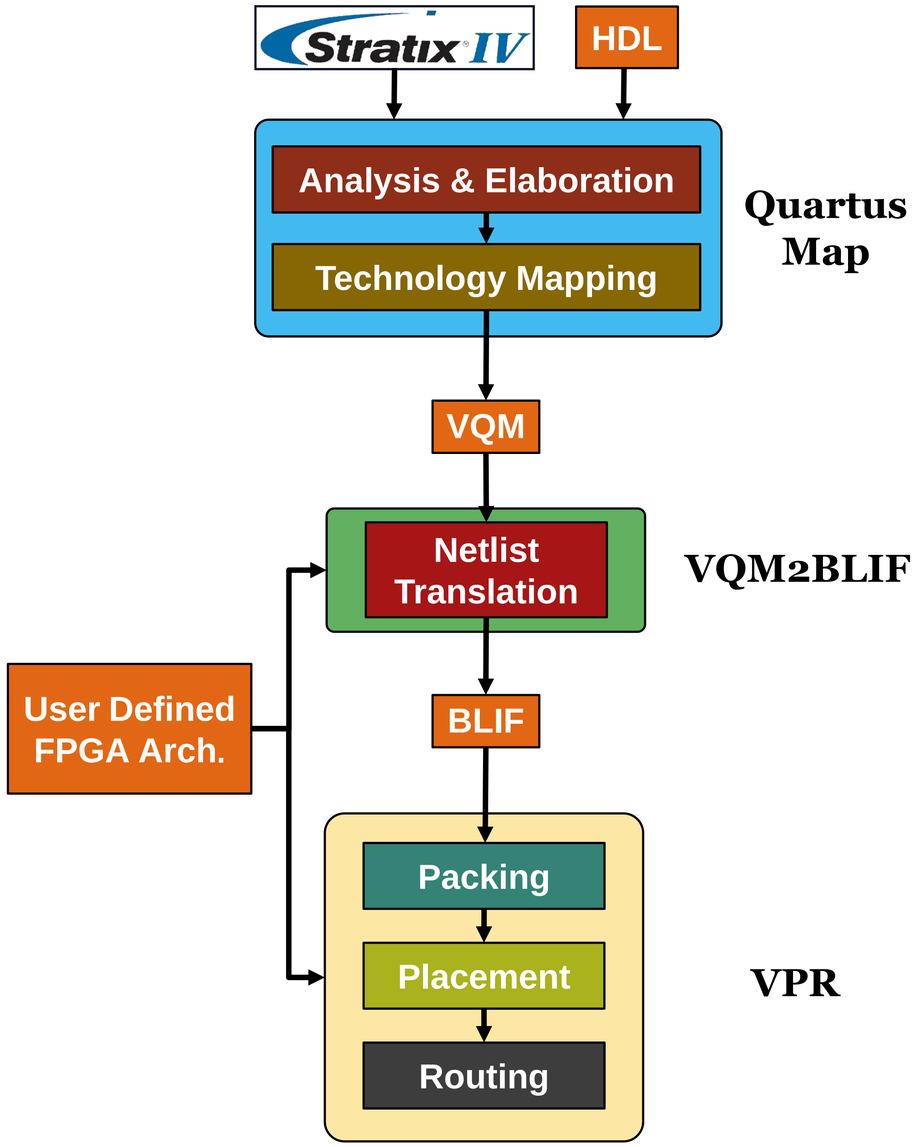
VQM Generation

- Set hidden variables in Quartus II
- Must remove encrypted IP

VQM2BLIF

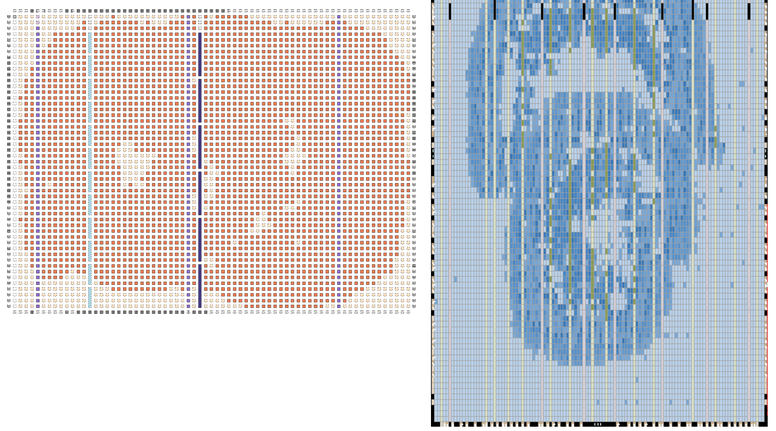
- Converts VQM into academic netlist (BLIF) based on VPR arch. file

Titan CAD Flow



Results

- Created flow enabling conversion from HDL to BLIF with minimal benchmark modifications
- Used flow to compare Quartus II and VPR



VPR (left) and Quartus II (right) placement of the *bc_small* benchmark

Download

Titan Flow & Benchmarks:
http://uoft.me/titan