Titan:
Large and Complex Benchmarks in Academic CAD

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FACULTY OF APPLIED SCIENCE & ENGINEERING

Outline

- Motivation

- Hybrid CAD Flow & Benchmarks

- VPR and Quartus II Comparison

- Conclusion and Future Work

Motivation

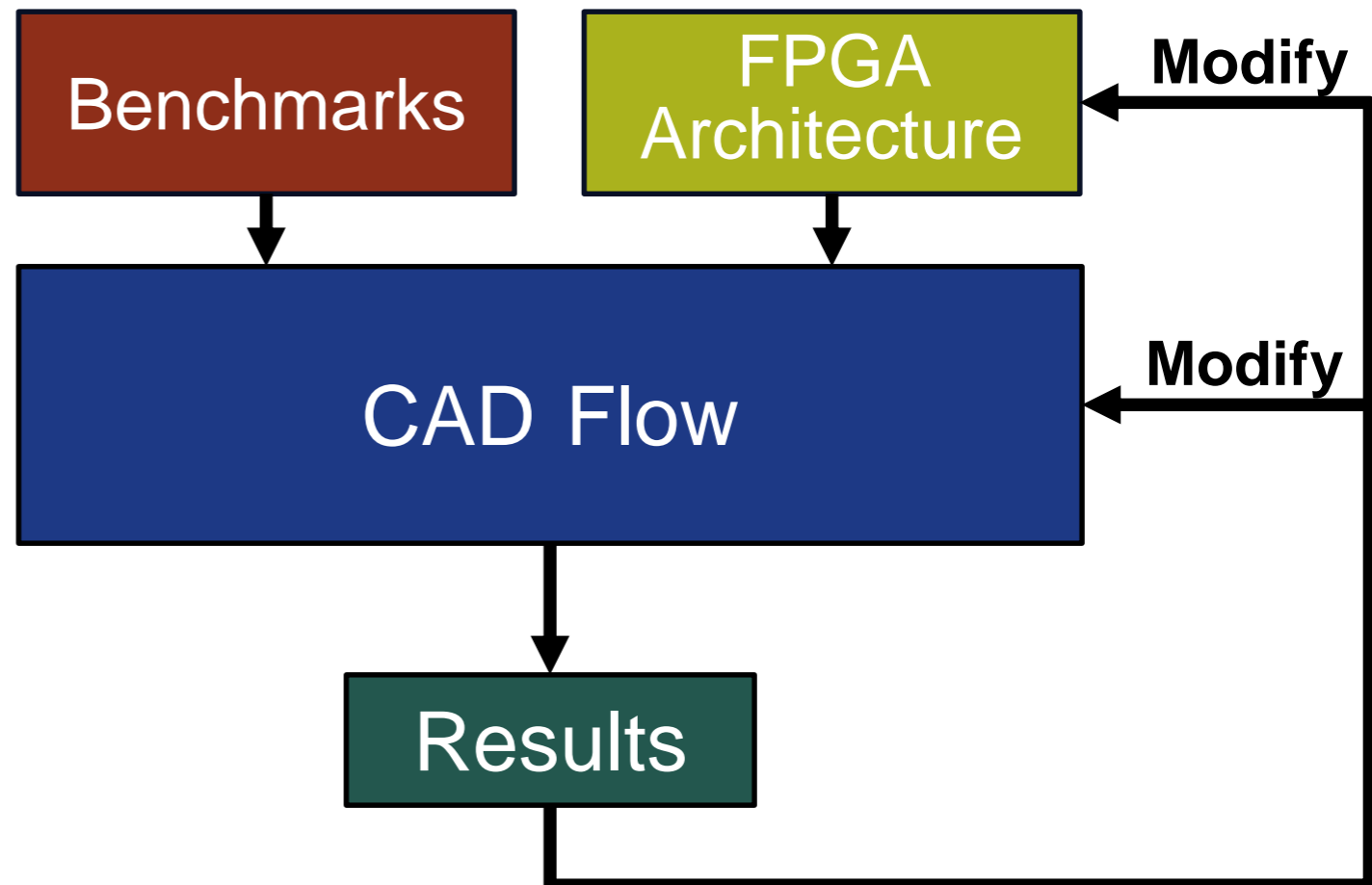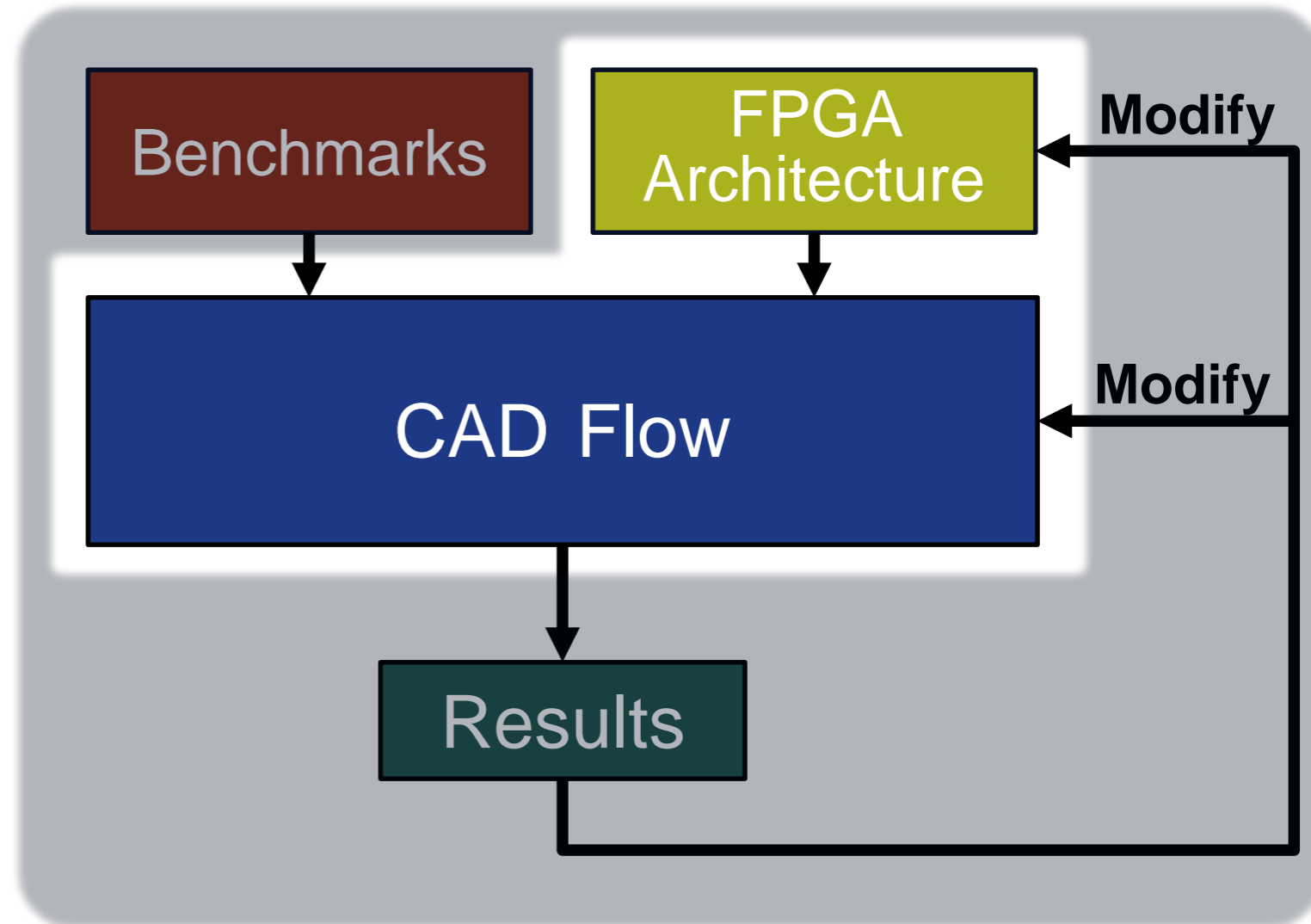# Evaluating FPGA Architectures and CAD

Must quantitatively compare:

- FPGA Architectures

- FPGA CAD Algorithms

Benchmarks often neglected

Good benchmarks:

- Exploit device characteristics (i.e. hard blocks)

- Comparable to modern device sizes

Benchmarks

FPGA Architecture

Modify

CAD Flow

Modify

Results

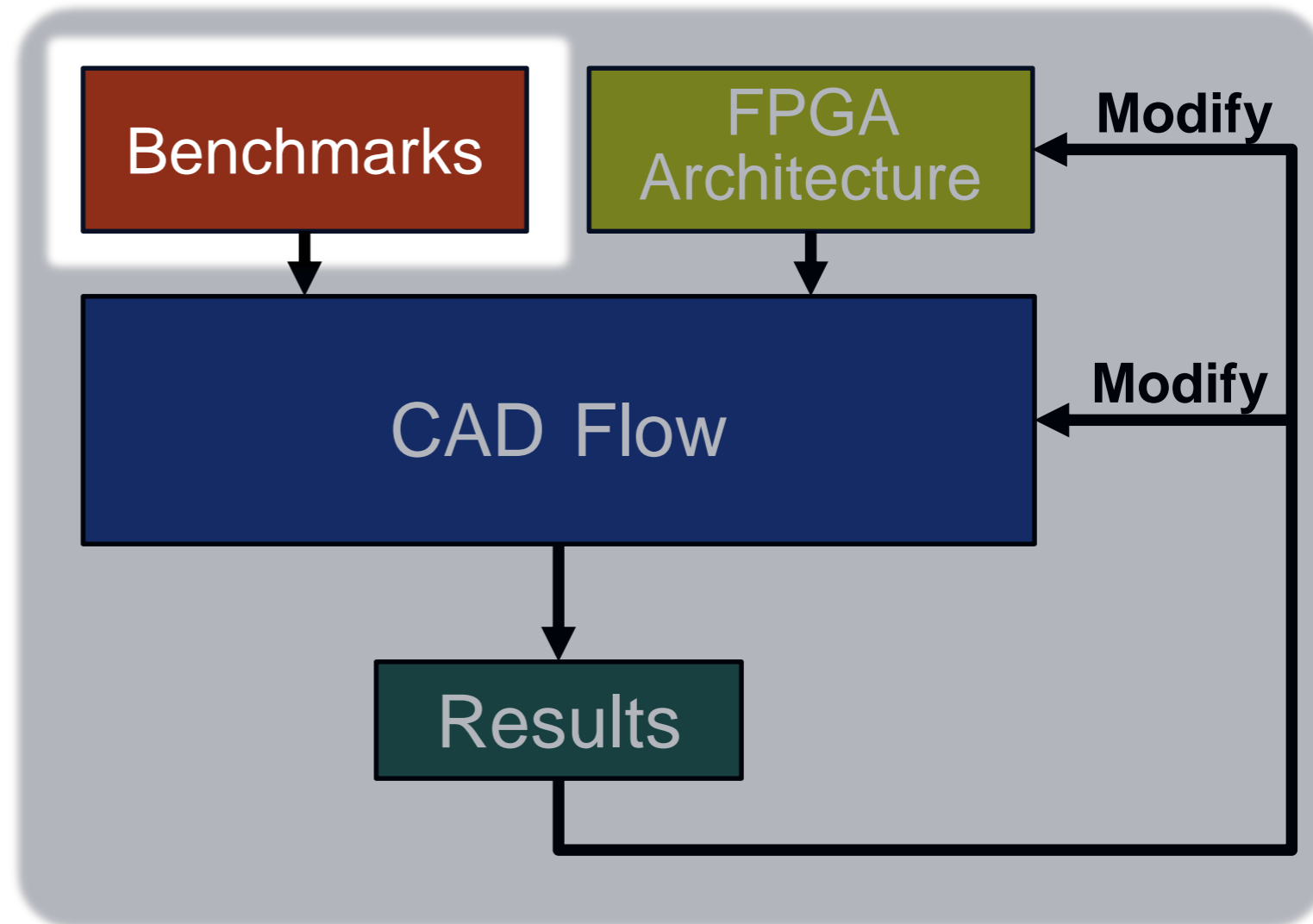# Evaluating FPGA Architectures and CAD

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Evaluating FPGA Architectures and CAD

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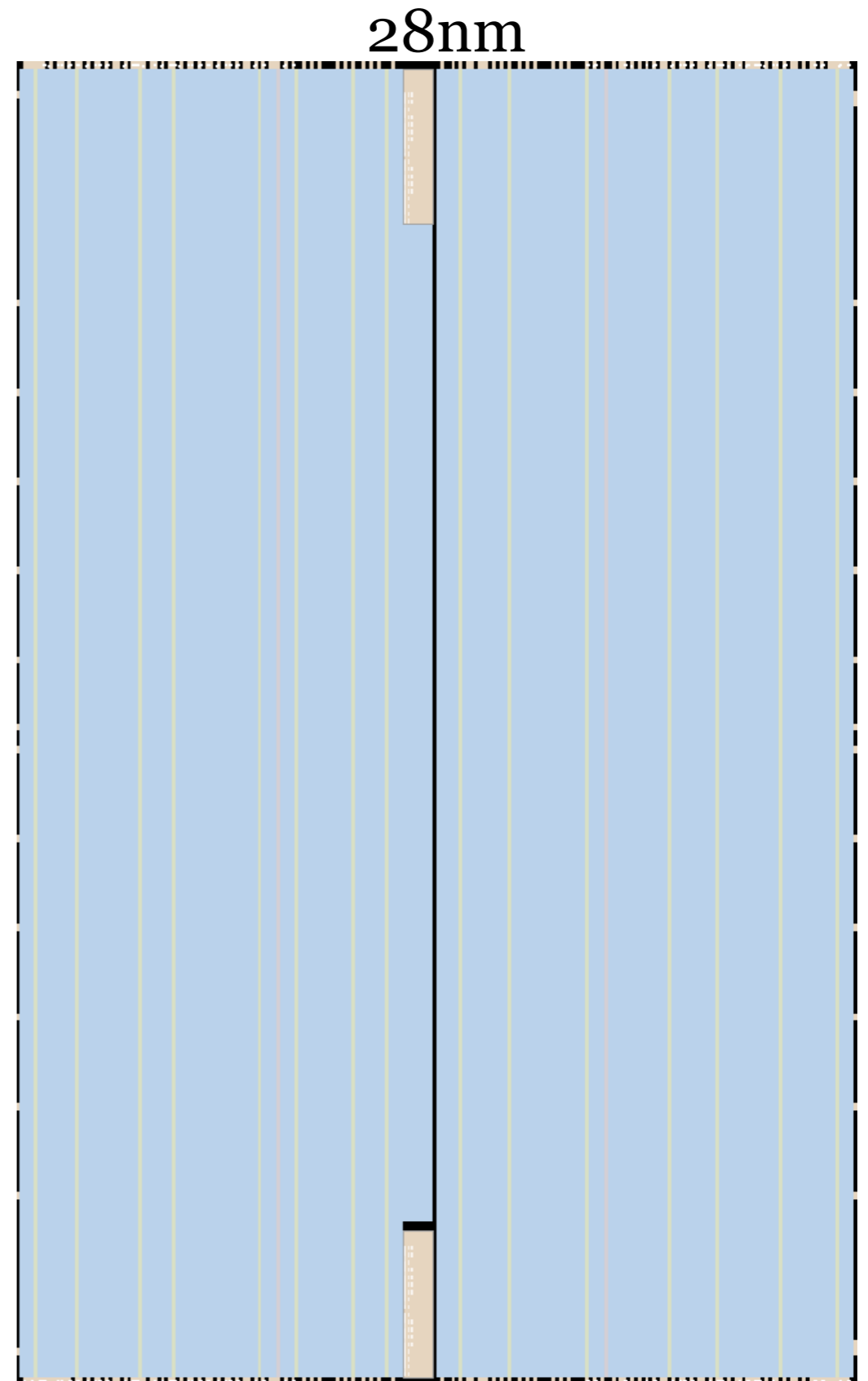
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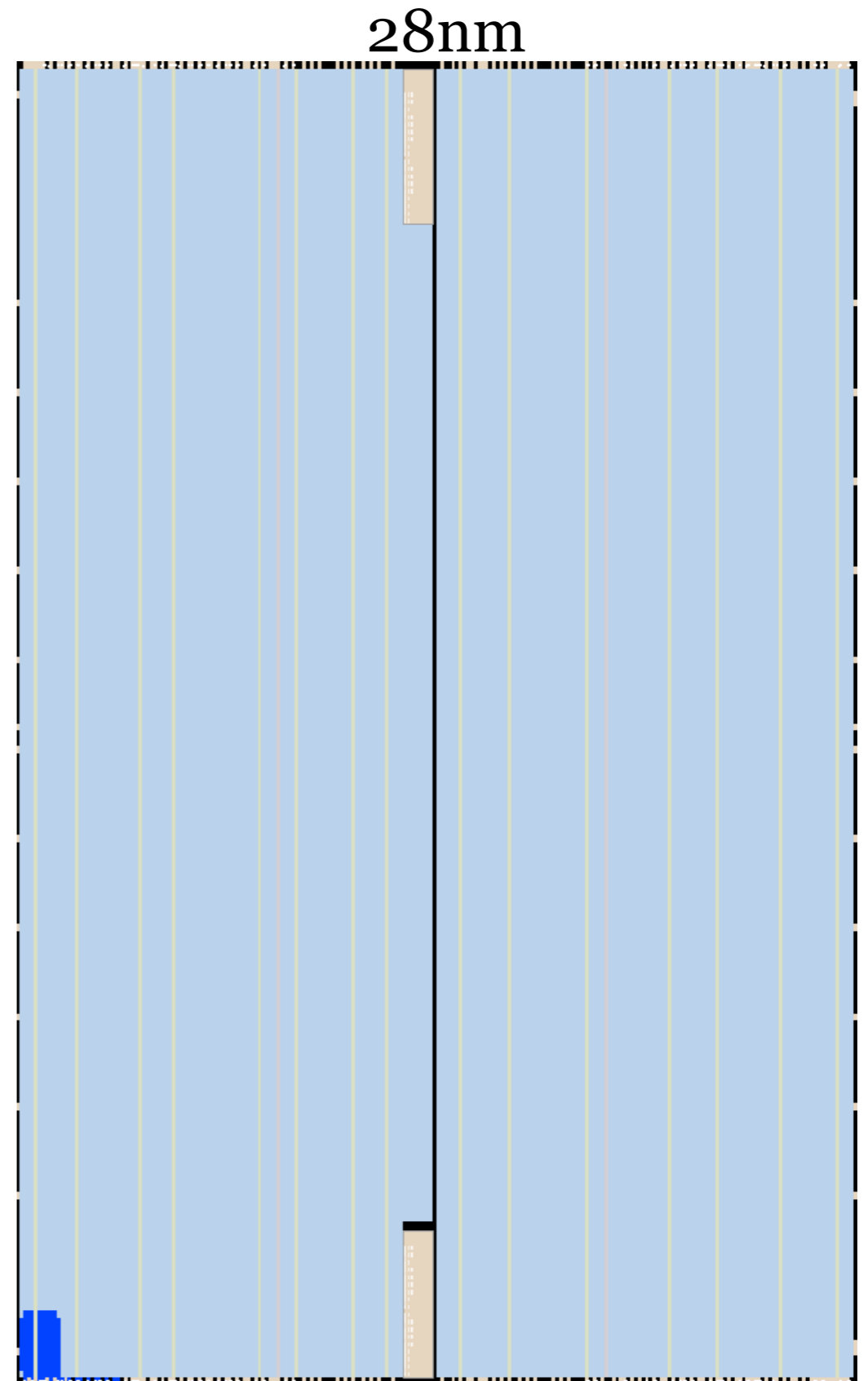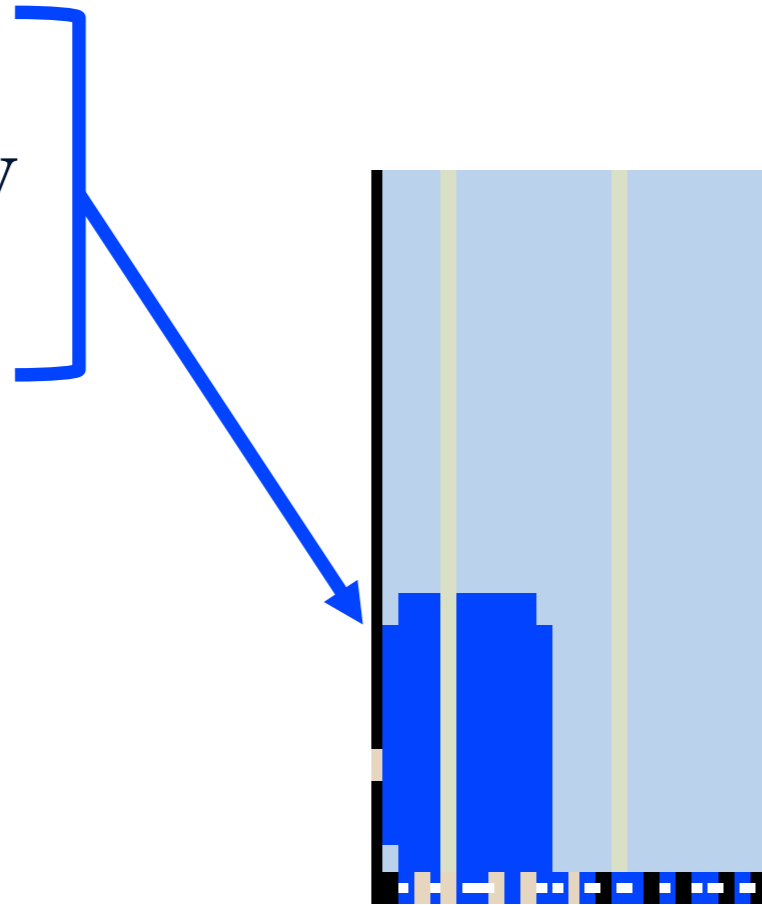
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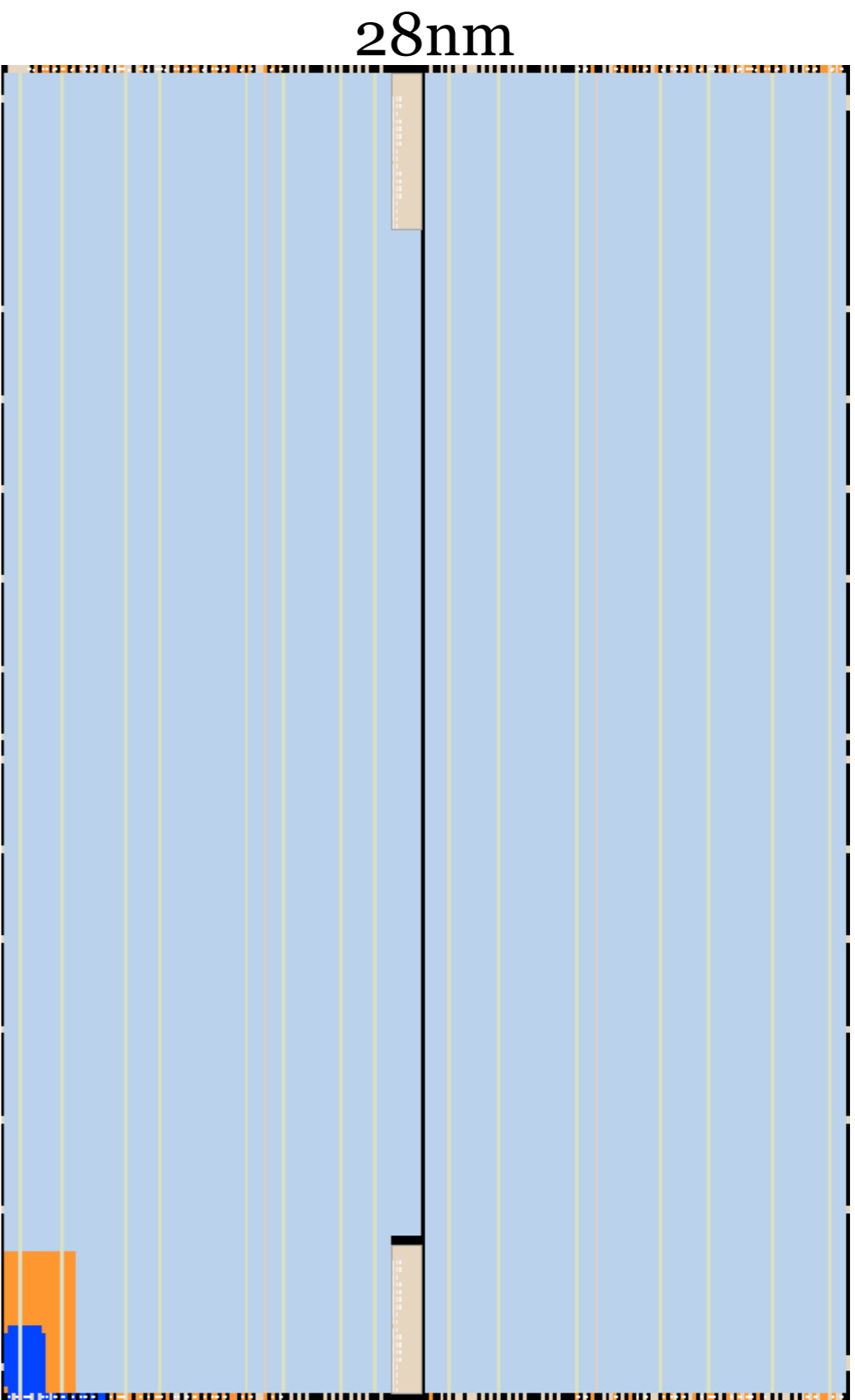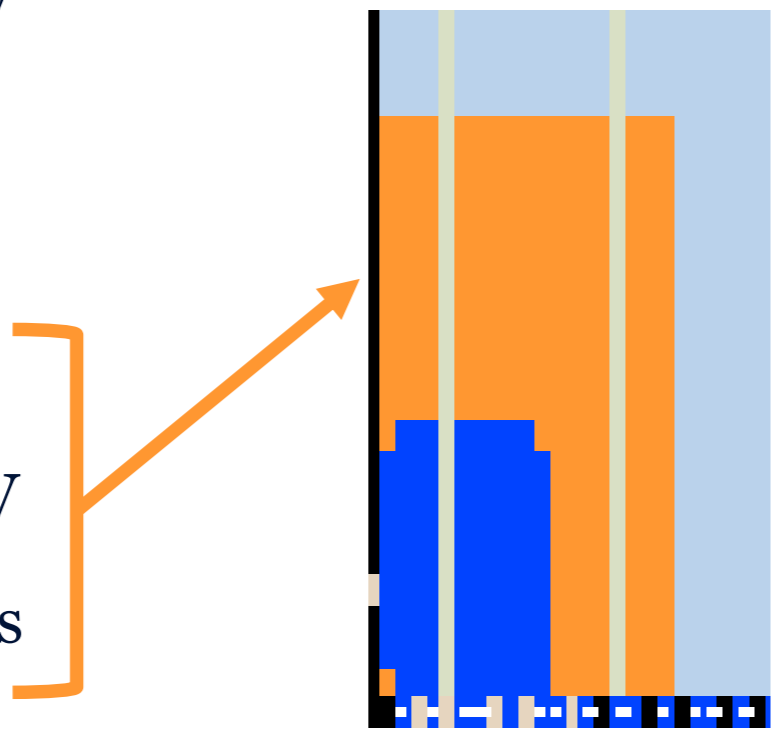
State of FPGA Benchmarks

28nm

State of FPGA Benchmarks

MCNC20 (1991)

- < 1% of Stratix V

- No Hard Blocks

28nm

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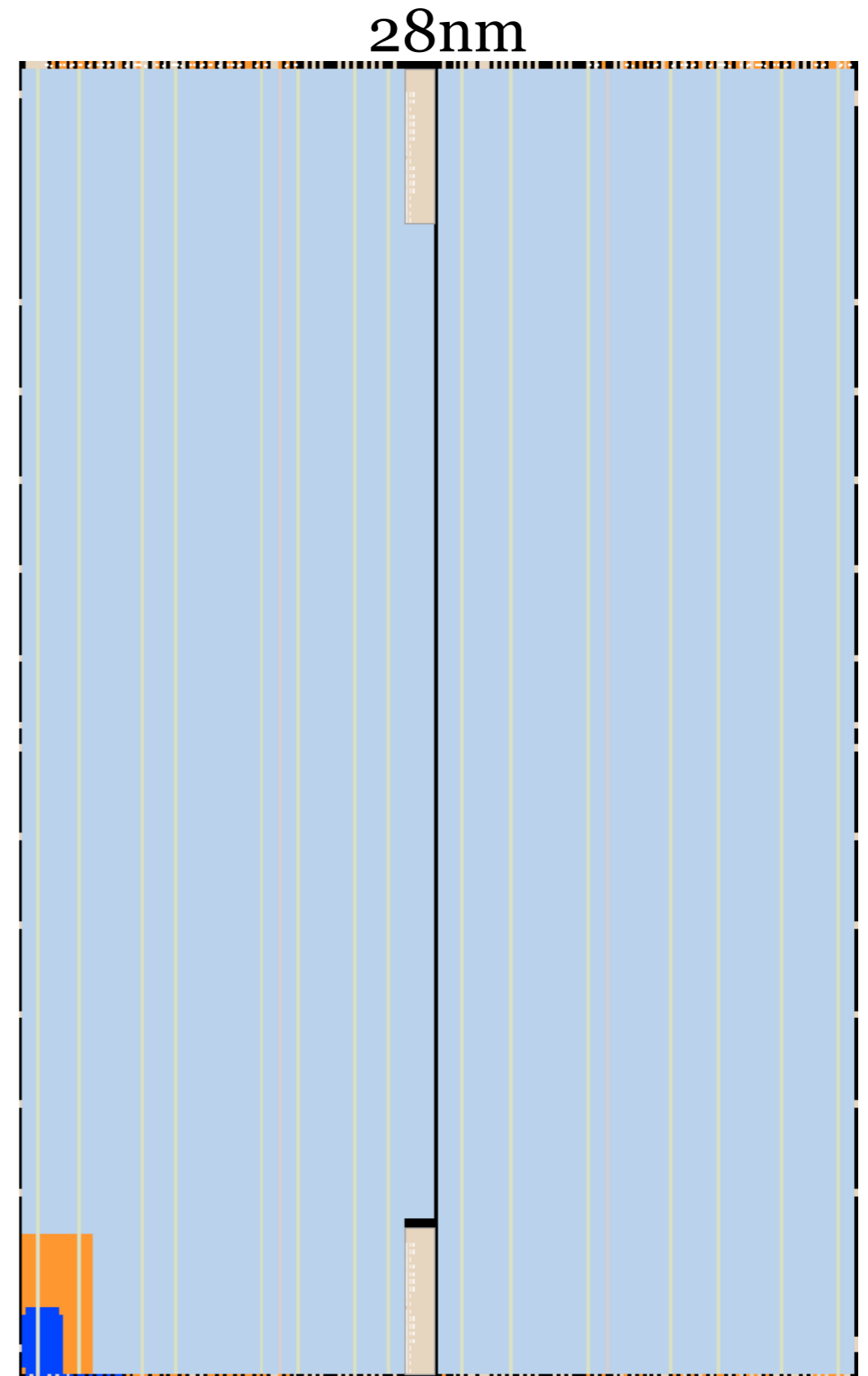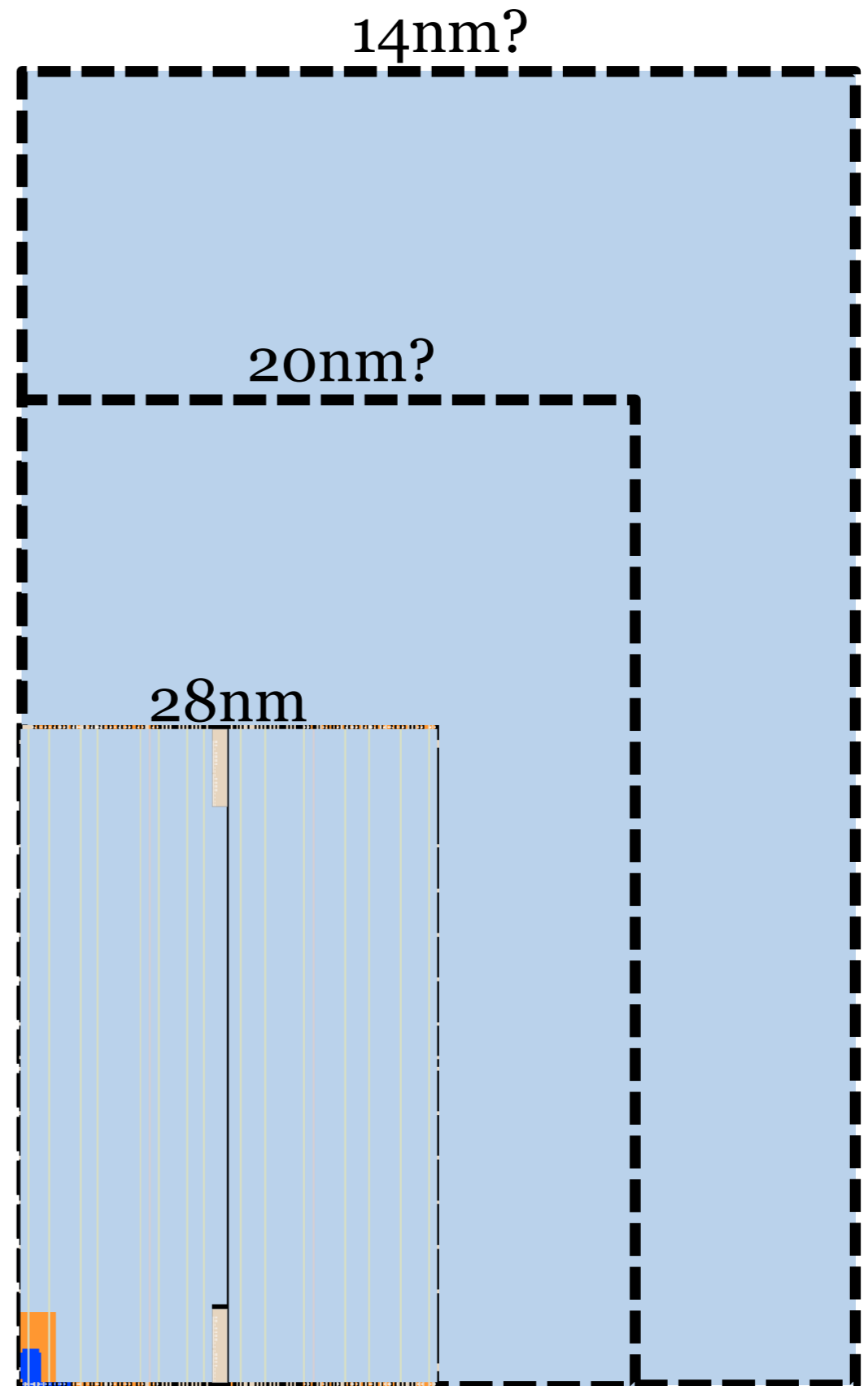## Even smaller on future devices

14nm?

20nm?

28nm
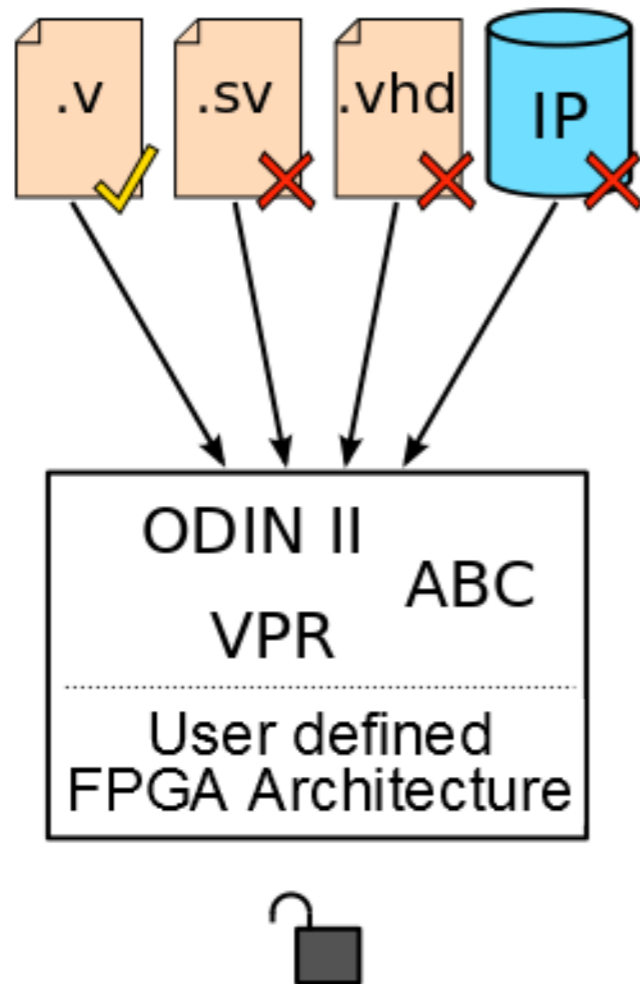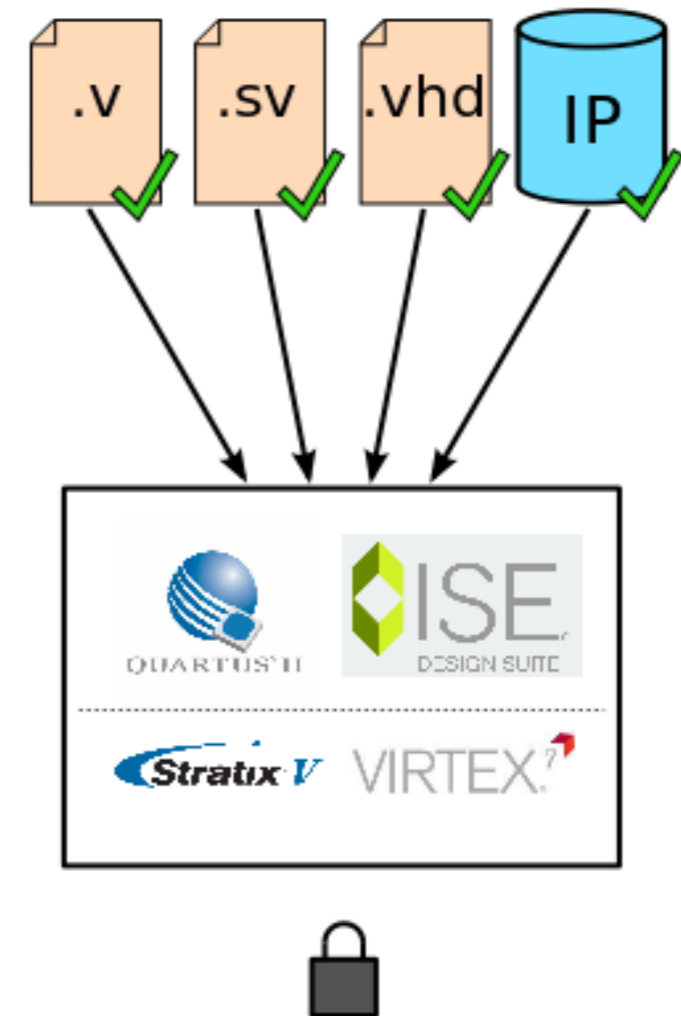
Why Don't We Have Better Benchmarks?

Academic tools cannot handle real designs

- Limited HDL support

- No IP Cores (Vendor, 3rd party)

Vendor tools are too restrictive

- *Limited to Vendor's Architectures*
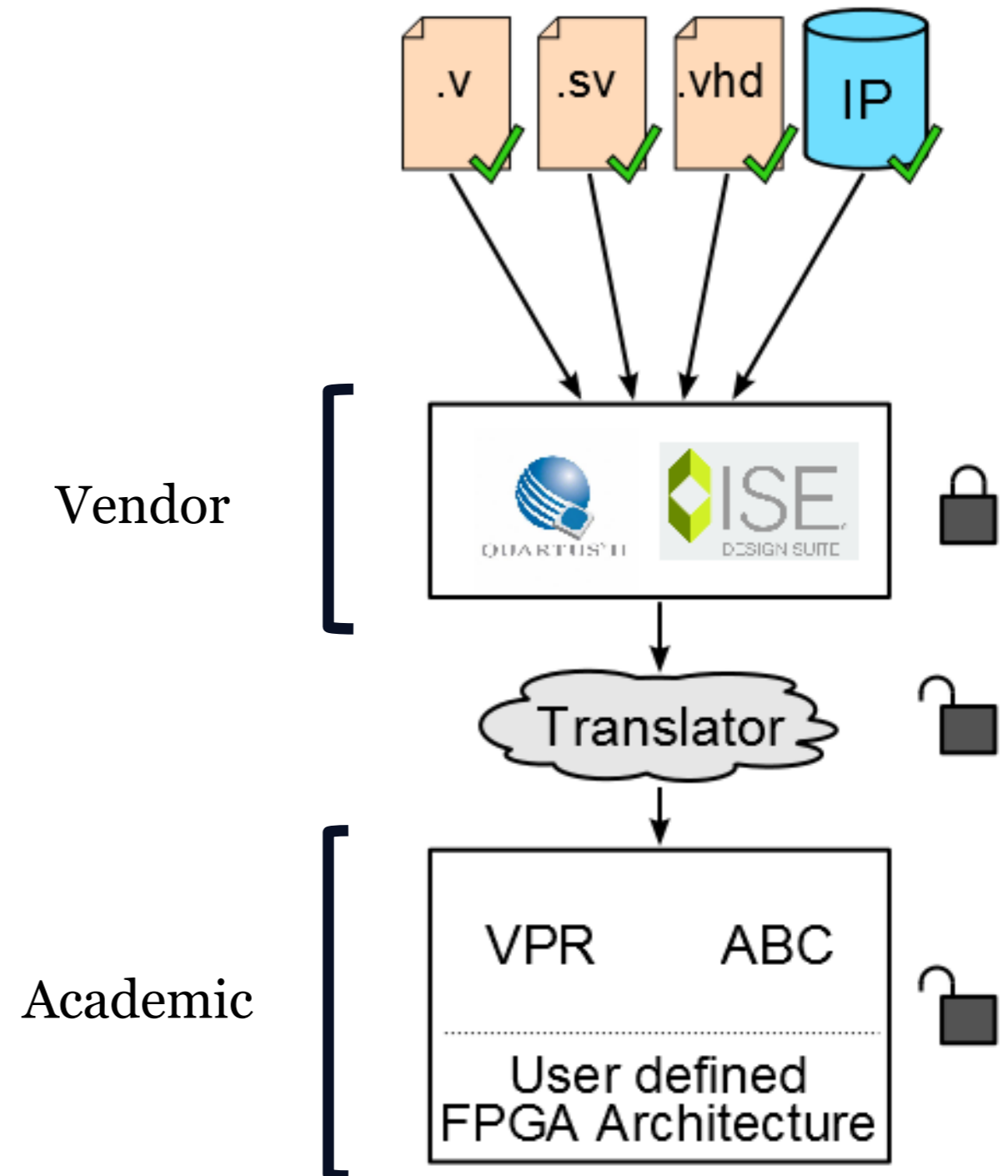
- *Cannot modify CAD algorithms*

Options?

Upgrade academic tools

- Add support for wide range of HDLs

- Create an IP library

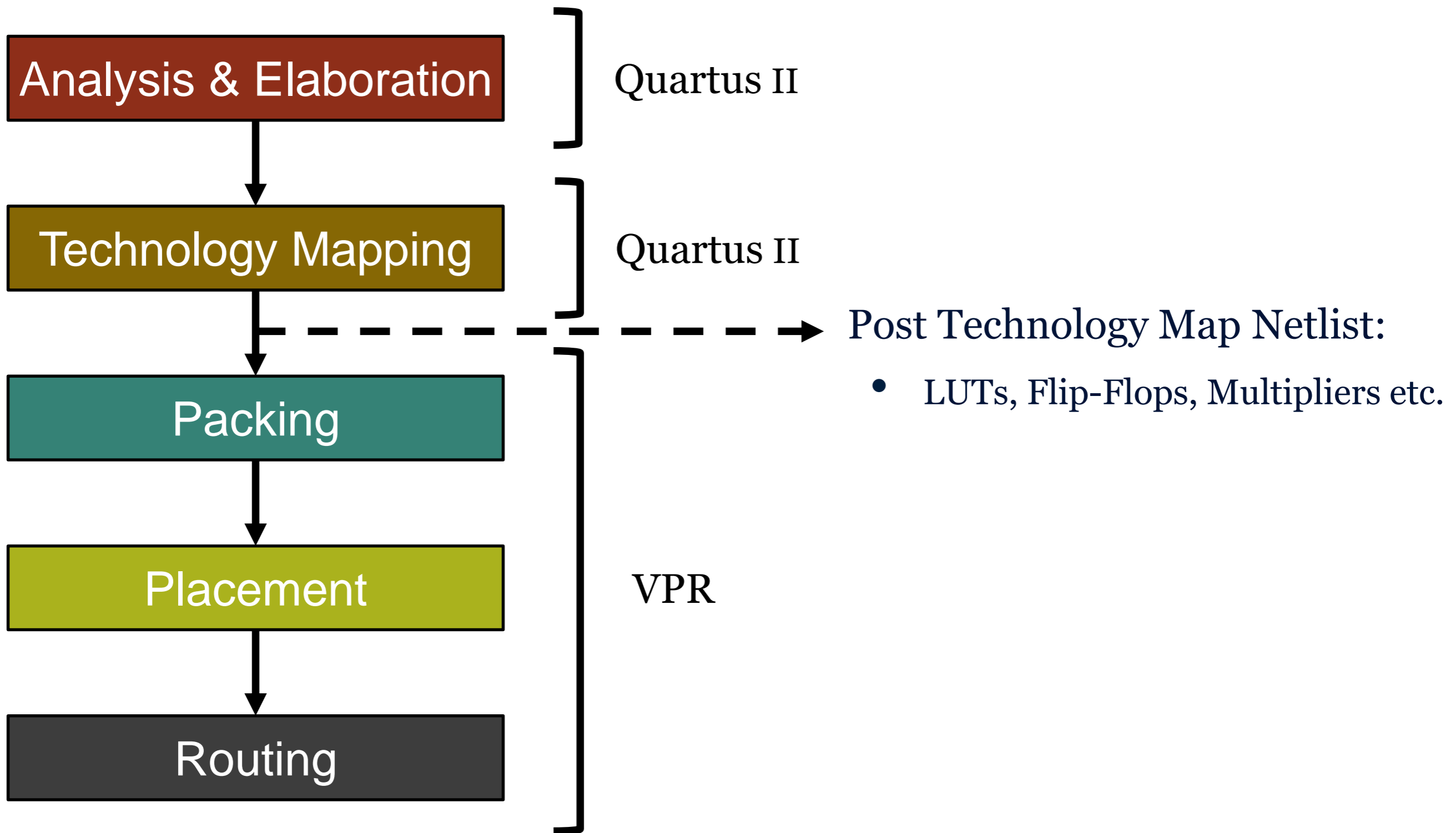- A huge investment!

Exploit vendor tool strengths?

- Hybrid CAD flow

Hybrid CAD Flow & Benchmarks

Building a Hybrid CAD Flow

Building a Hybrid CAD Flow

Analysis & Elaboration — Quartus II

Technology Mapping — Quartus II

Packing, Placement, Routing — VPR

Post Technology Map Netlist:
- LUTs, Flip-Flops, Multipliers etc.

Building a Hybrid CAD Flow

Analysis & Elaboration — Quartus II

Technology Mapping — Quartus II

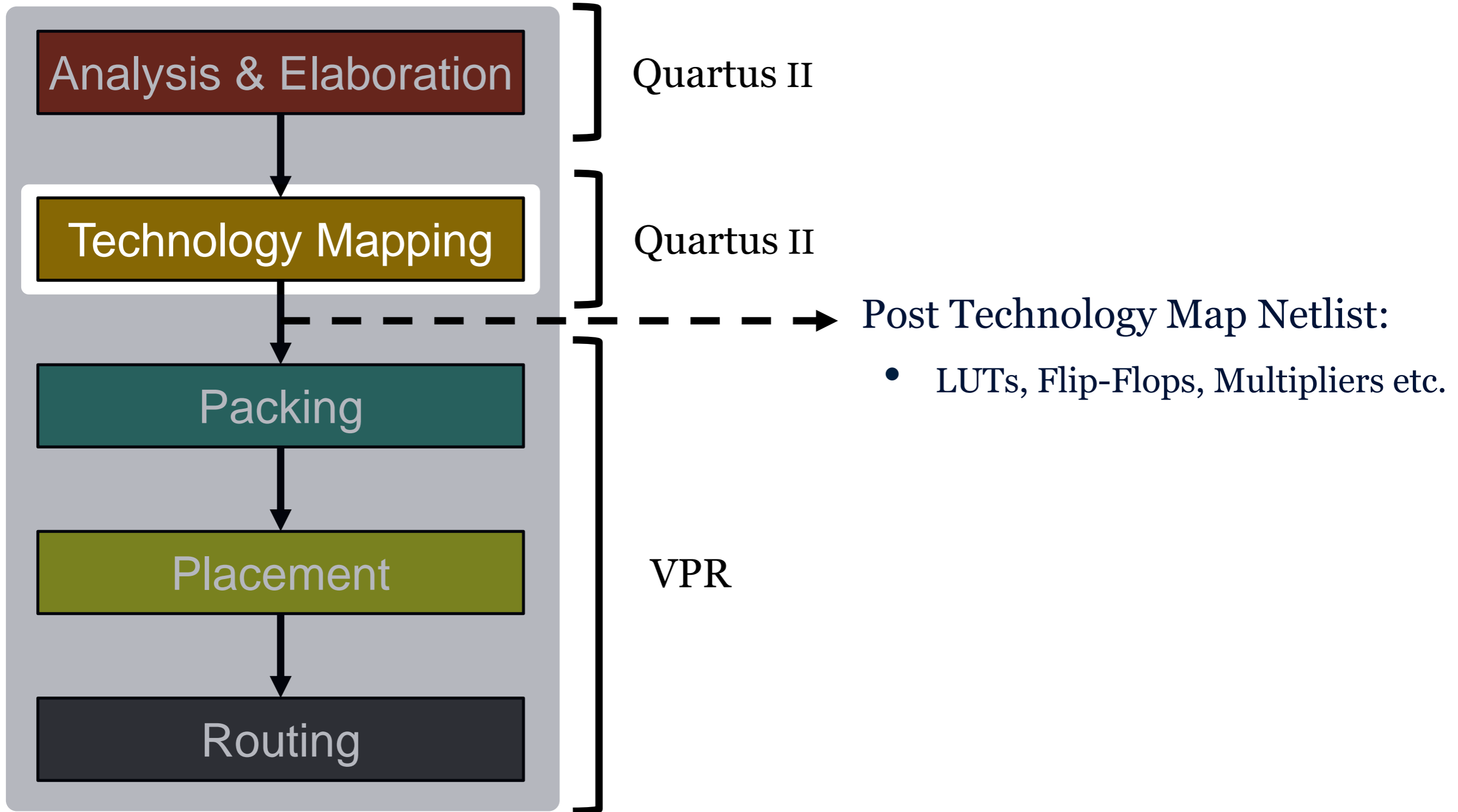Post Technology Map Netlist:
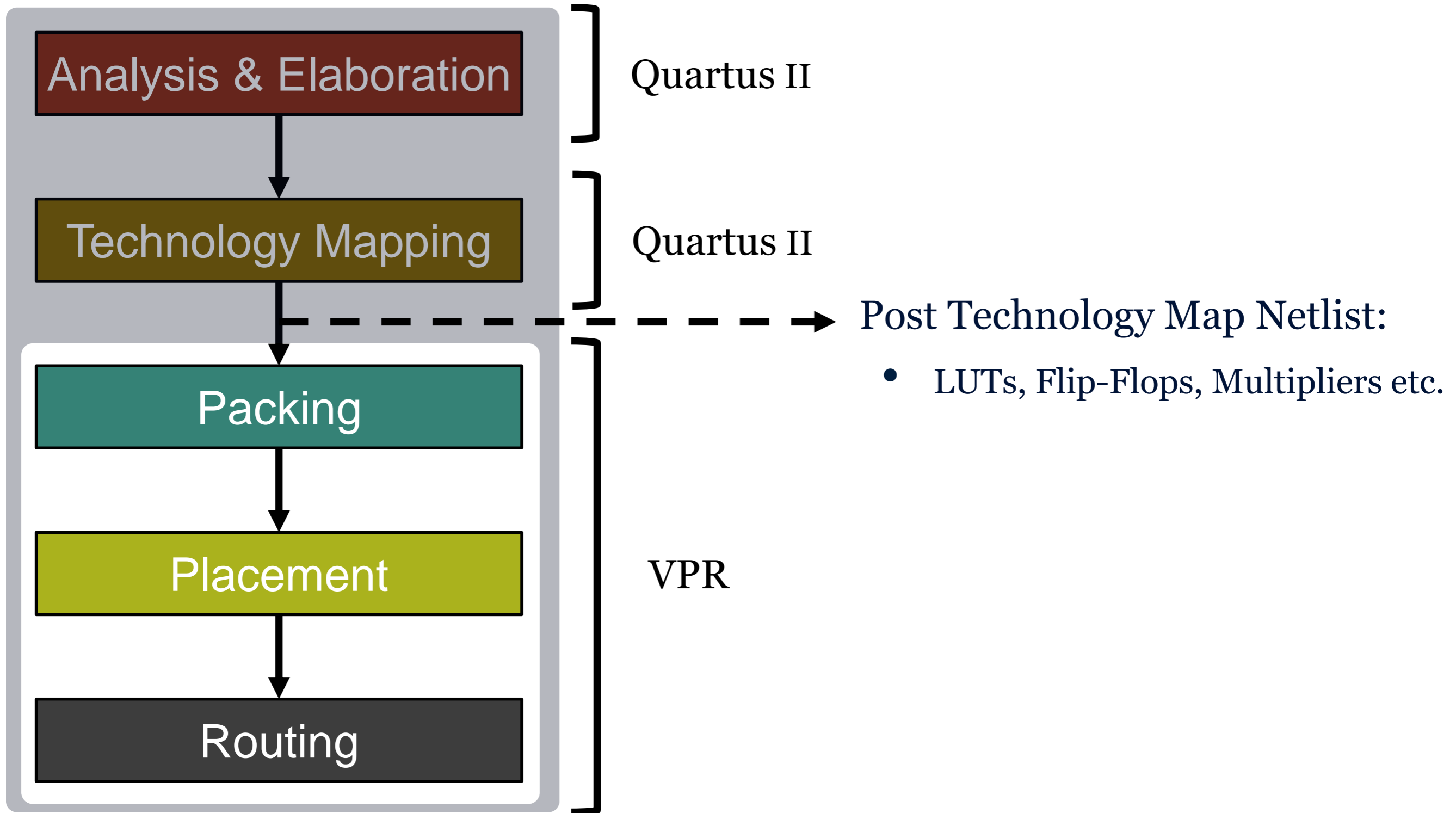- LUTs, Flip-Flops, Multipliers etc.

Packing

Placement — VPR

Routing

Building a Hybrid CAD Flow

Titan Flow Capabilities & Limitations

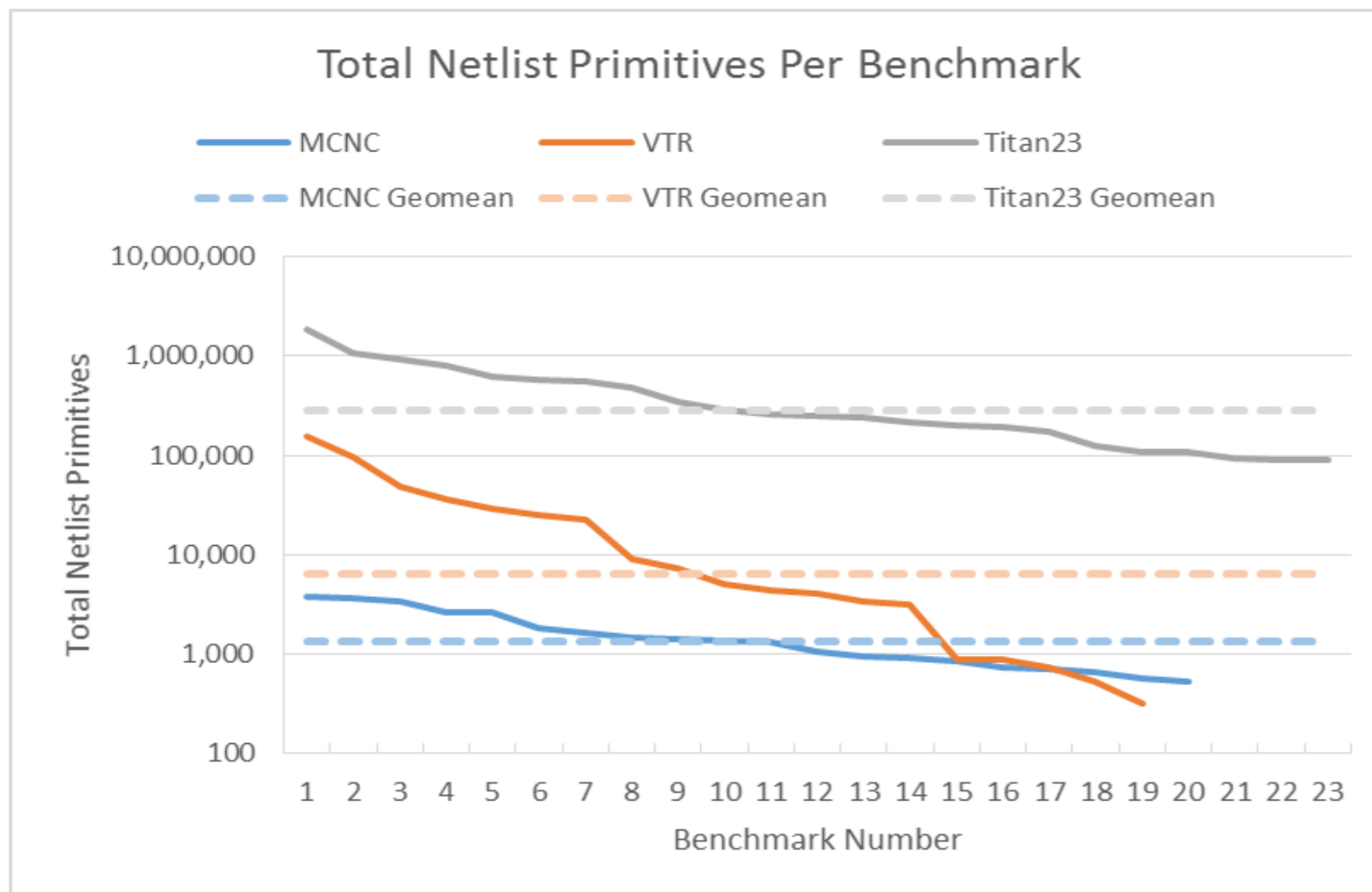| Experiment Modification	VTR	Titan	Titan Flow Method
Device Floorplan	Yes	Yes	Architecture file
Inter-cluster Routing	Yes	Yes	Architecture file
Clustered Block Size / Configuration	Yes	Yes	Architecture file
Intra-cluster Routing	Yes	Yes	Architecture file
LUT size / Combinational Logic Element	Yes	Yes	ABC re-synthesis
New RAM Block	Yes	Yes	Architecture file (up to 16K depth*)
New DSP Block	Yes	Yes	Architecture file (up to 36 bit width*)
New Primitive Type	Yes	No	No method to pass black box through Quartus II

* Maximum for Stratix IV

Titan 23 Benchmarks

- 23 Benchmarks

- Wide range of application domains

- All make use of hard blocks (DSPs, RAMs)
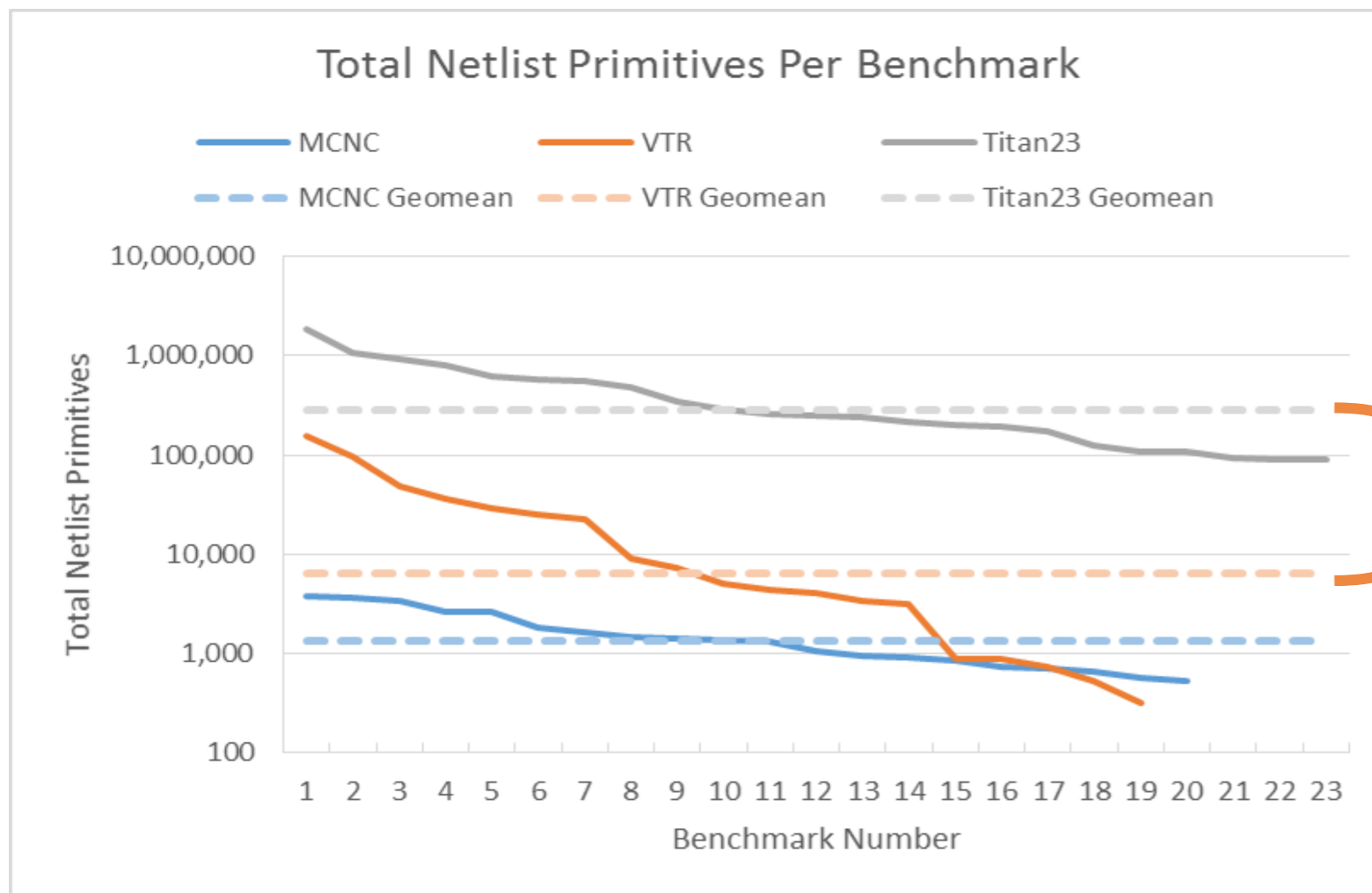
- 90K to 1.9M netlist primitives

Neural Network Control Systems
Signal Processing
Communications SHA Hashing
Computer Vision
Sorting
Microprocessor DSP
Radar Processing
Communication Switch
On Chip Network
Matrix Decomposition Multi-core
Image Processing

Total Netlist Primitives Per Benchmark

Legend: MCNC, VTR, Titan23, MCNC Geomean, VTR Geomean, Titan23 Geomean

Y-axis: Total Netlist Primitives (100 to 10,000,000)

X-axis: Benchmark Number (1 to 23)

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44 ×
VTR

# Titan 23 Benchmarks

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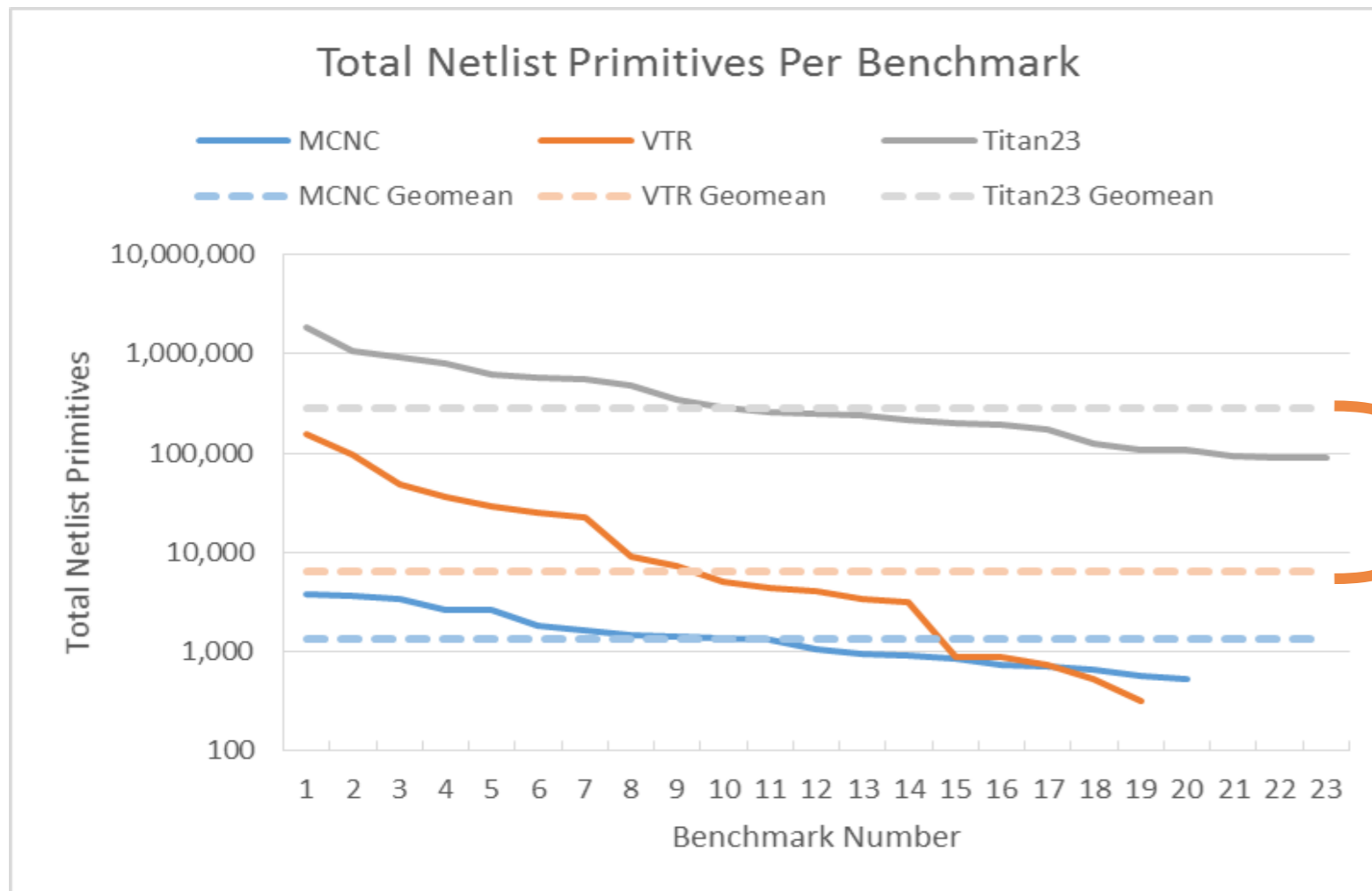
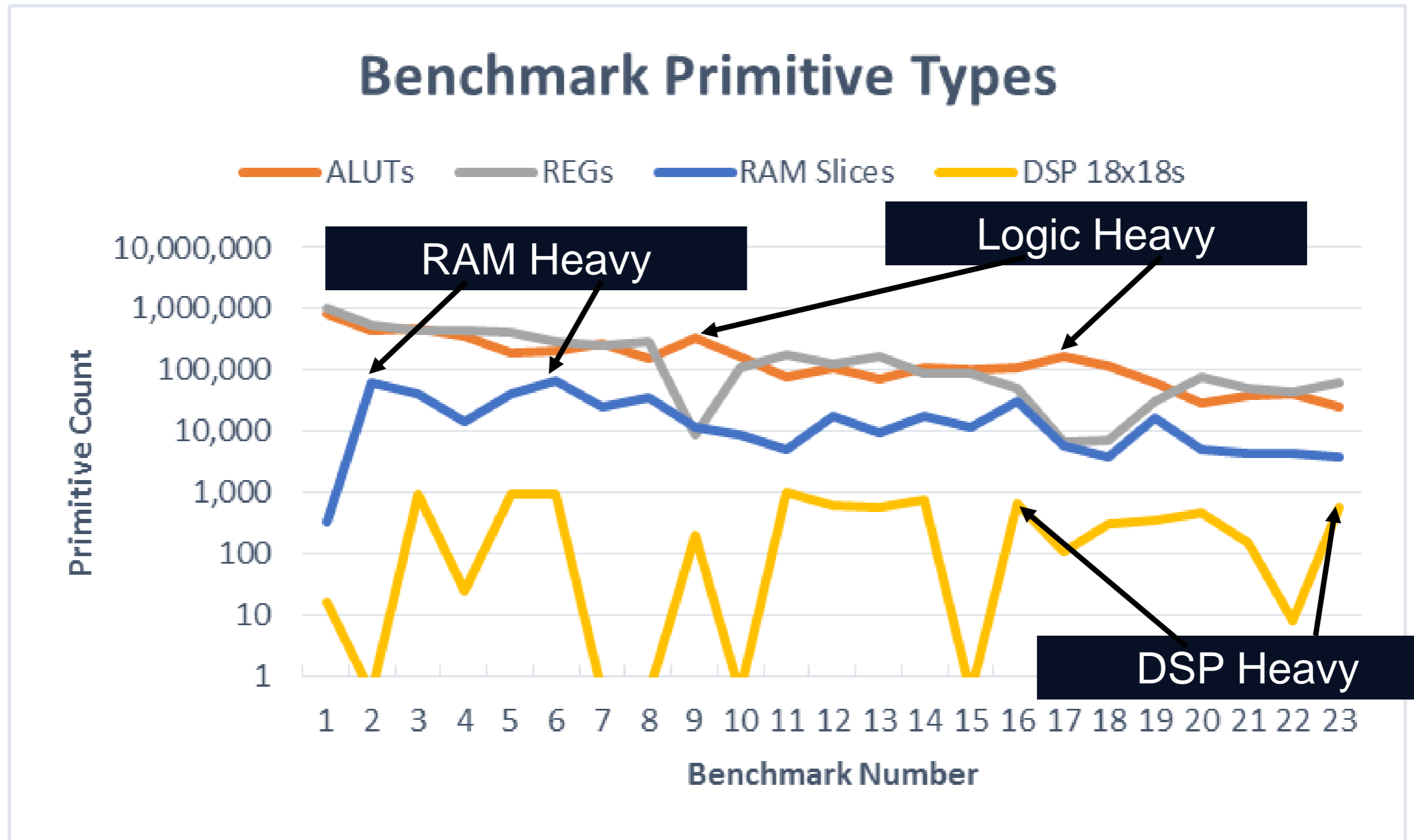**44 × VTR**

215 × MCNC

Benchmark Details

Benchmark Primitive Types

Benchmark Details
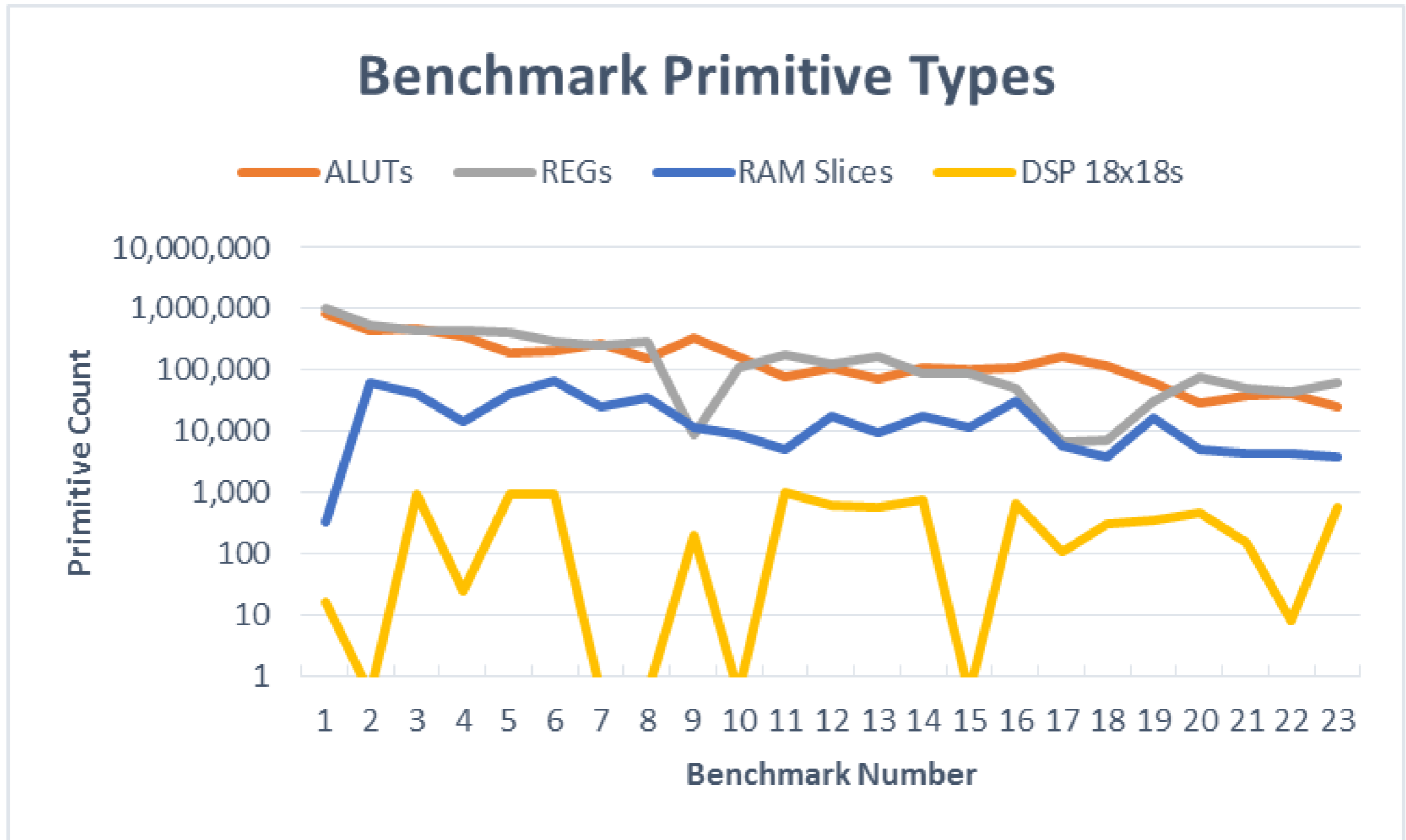
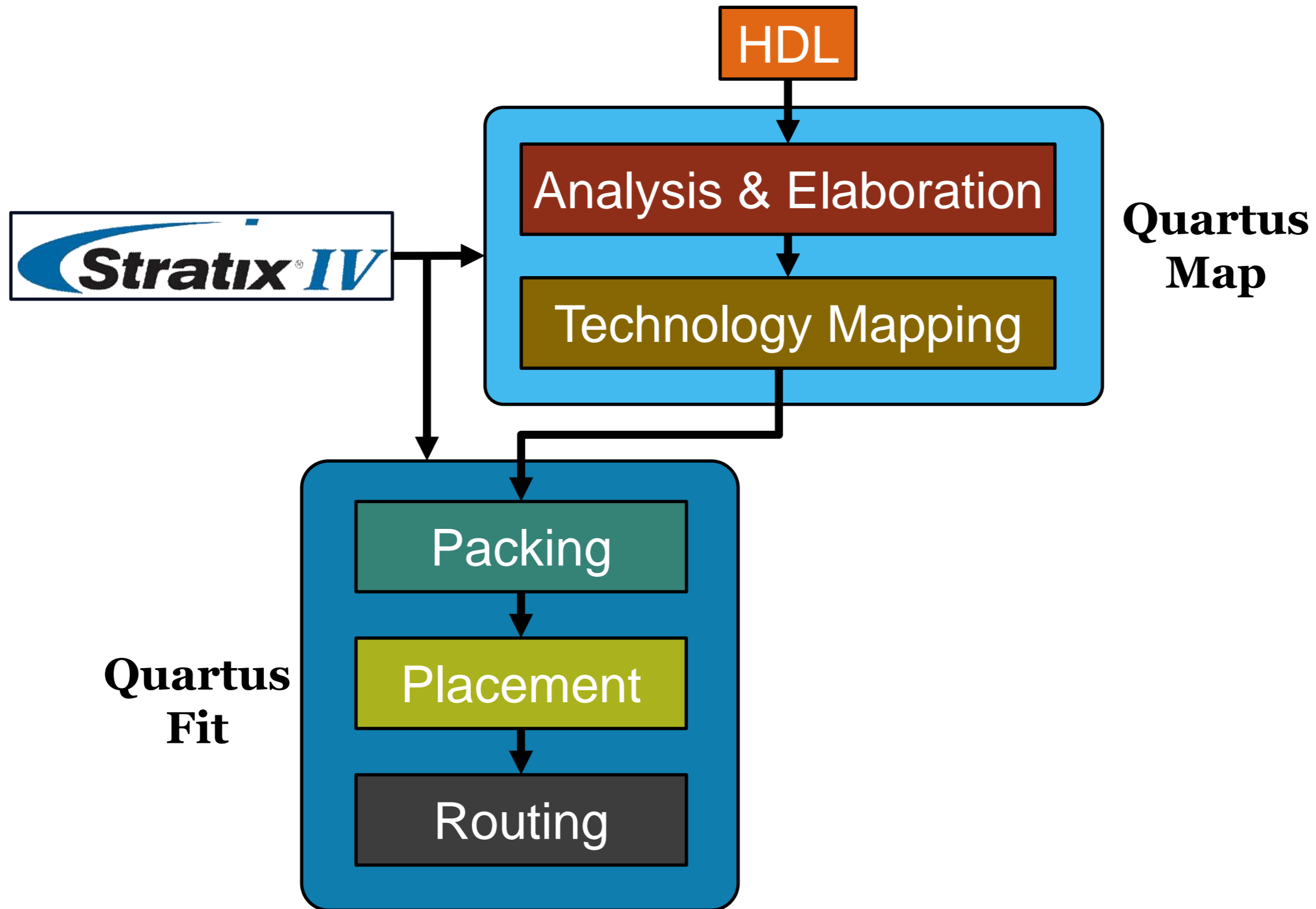# Benchmark Details
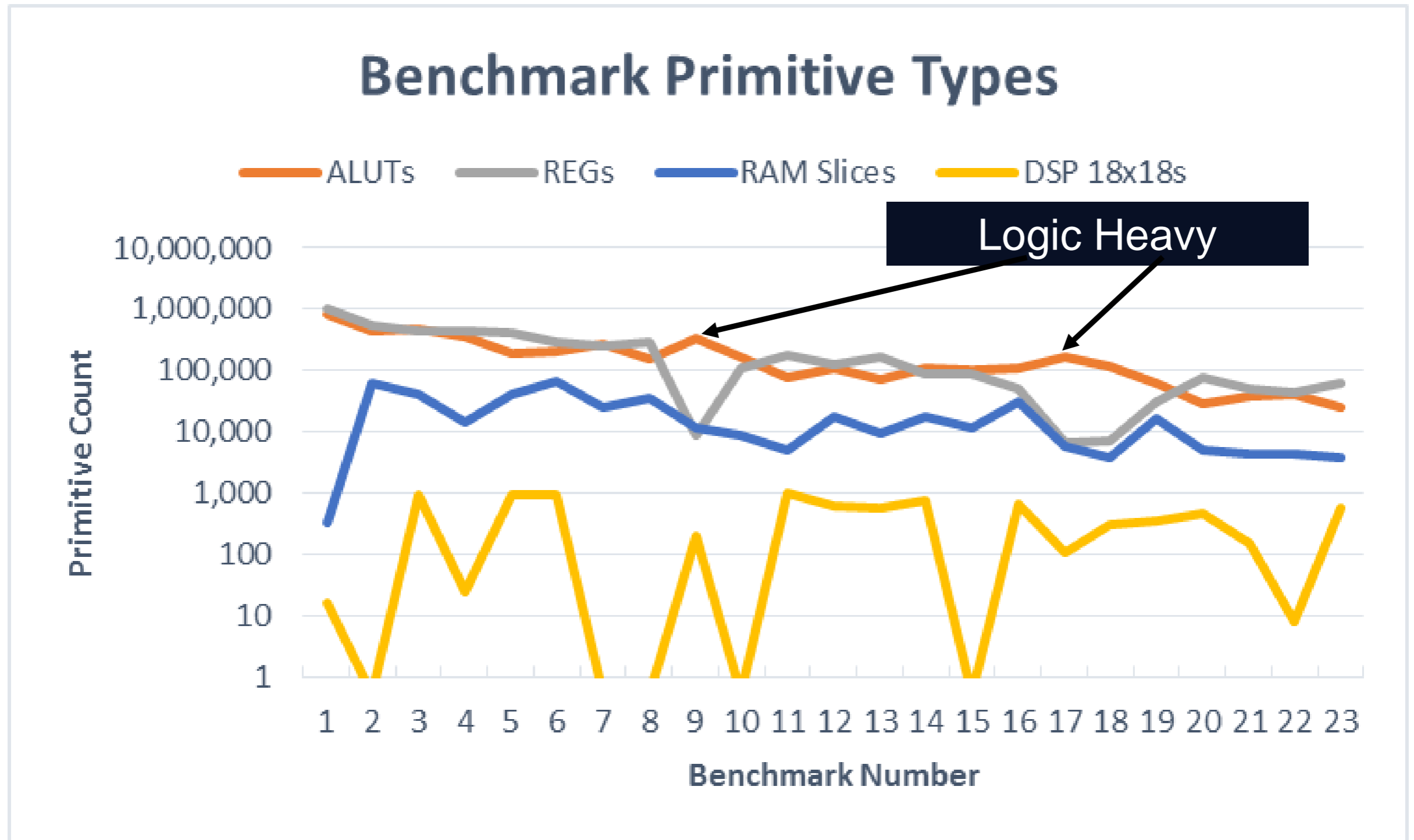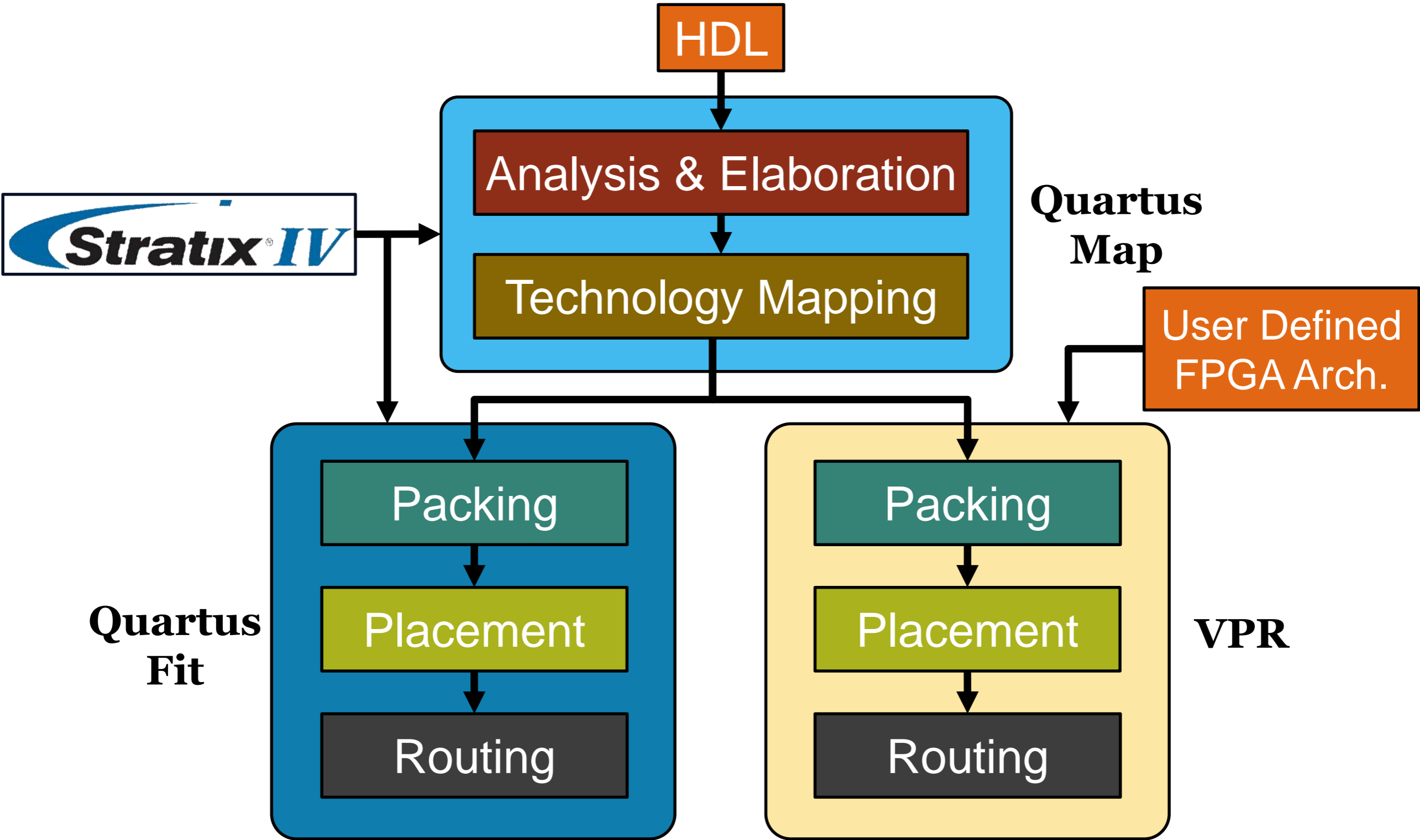
Benchmark Details
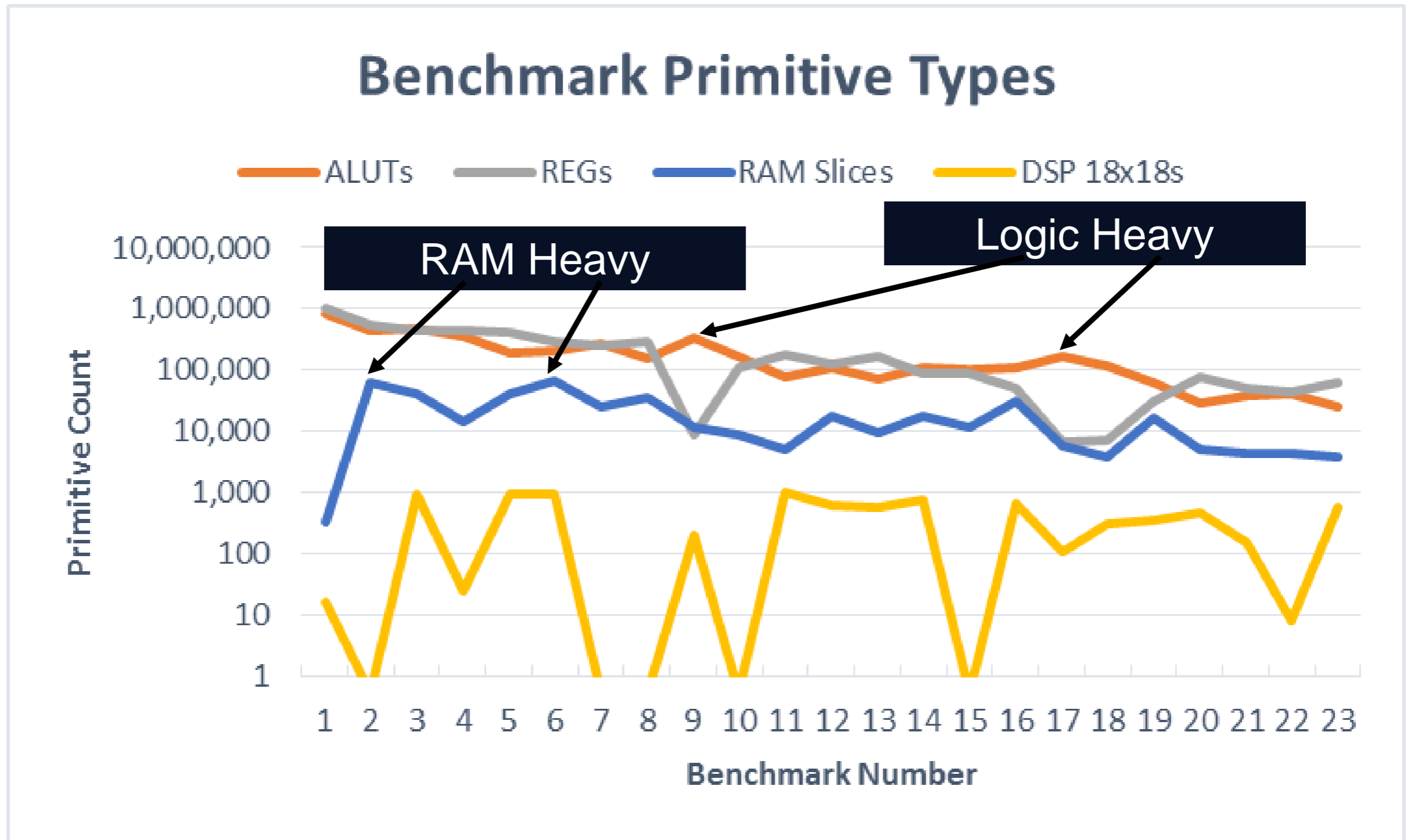
Benchmark Primitive Types

VPR and Quartus II Comparison

VPR and Quartus II Flows

VPR and Quartus II Flows

Titan Compatible Architecture

- Architecture must use same primitives as logic synthesis

- Can be grouped into arbitrary blocks

Primitive	Description
lcell_comb	LUT and Full Adder
dffeas	Register
mlab_cell	LUT RAM
mac_mult	Multiplier
mac_out	Accumulator
ram_block	RAM Slice
io_{i,o}buf	I/O Buffer
ddio_{in,out}	DDR I/O
pll	Phase Locked Loop

Stratix IV Architecture Capture
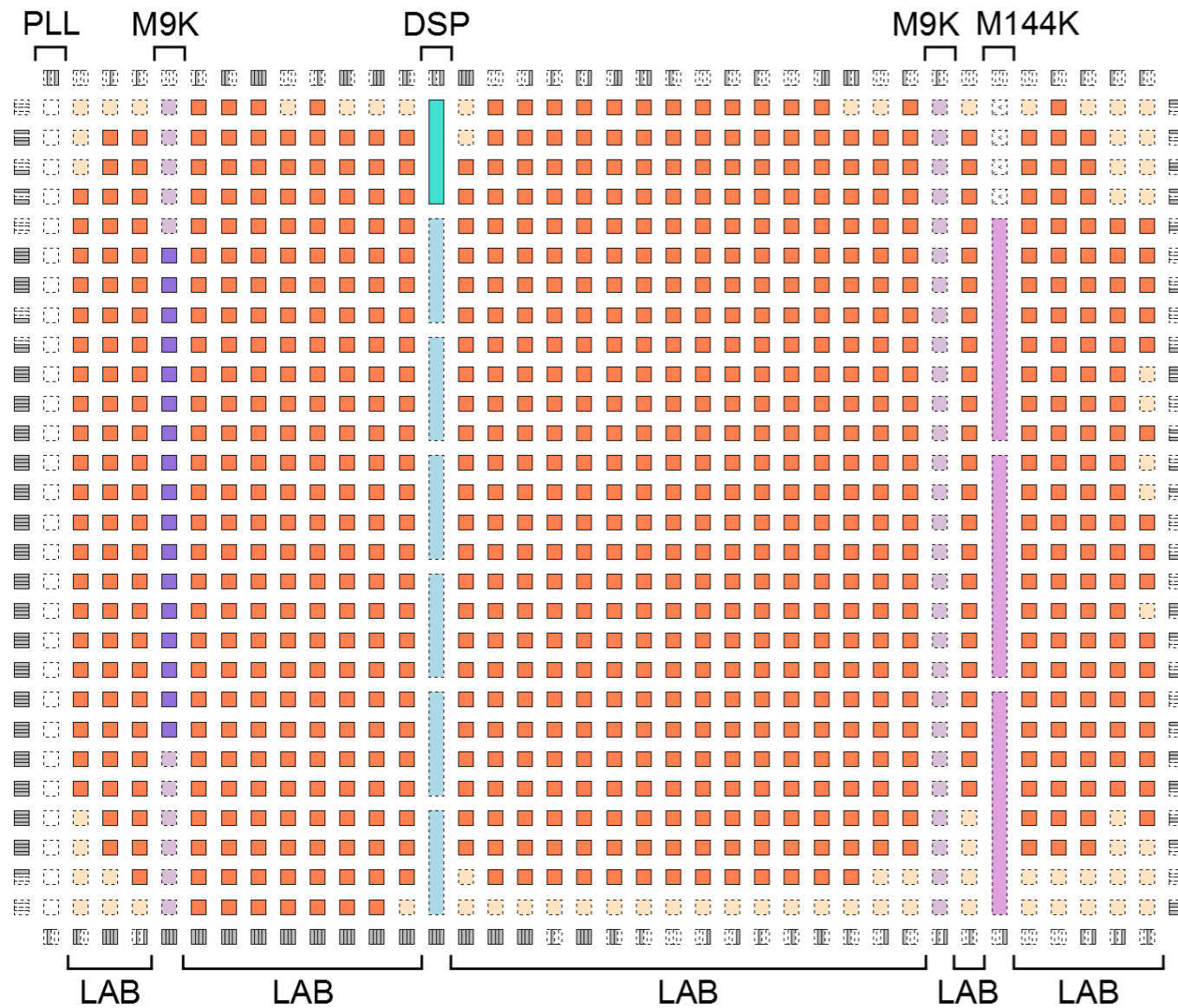
Floorplan:

- Based on EP4SE820

Fully Modeled Blocks:

- LAB

- DSP

- M9K

- M144K

Routing Network:

- Mixture of long and short wires
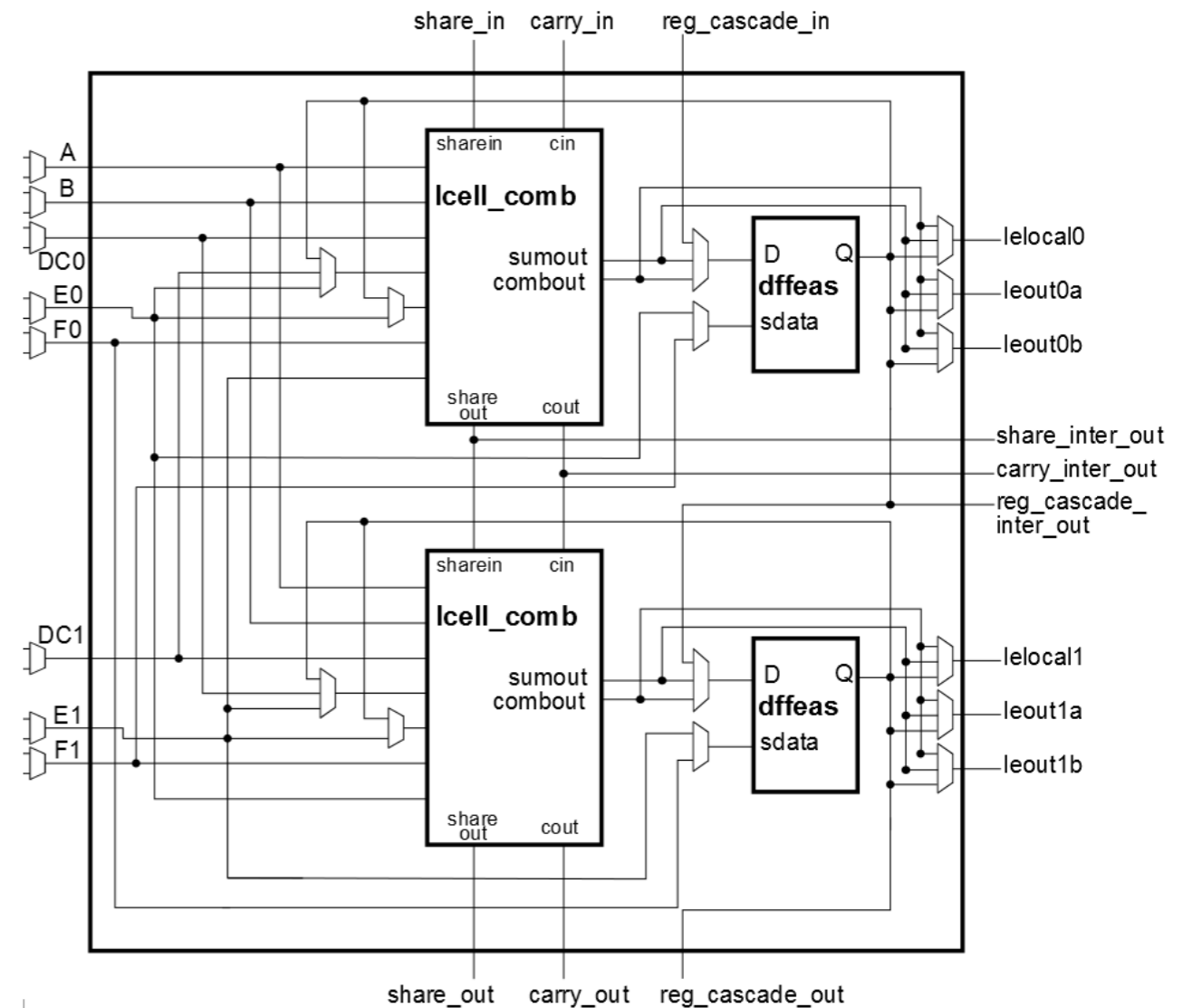
Architecture Details

LAB

- Detailed internal connectivity

- Full instead of partial crossbars

- Extra carry chain connectivity

M9K & M144K RAM Blocks

- All modes and sizes

- Approximated mixed-width modes

DSP Blocks

- All Stratix IV multiplier/accumulator modes

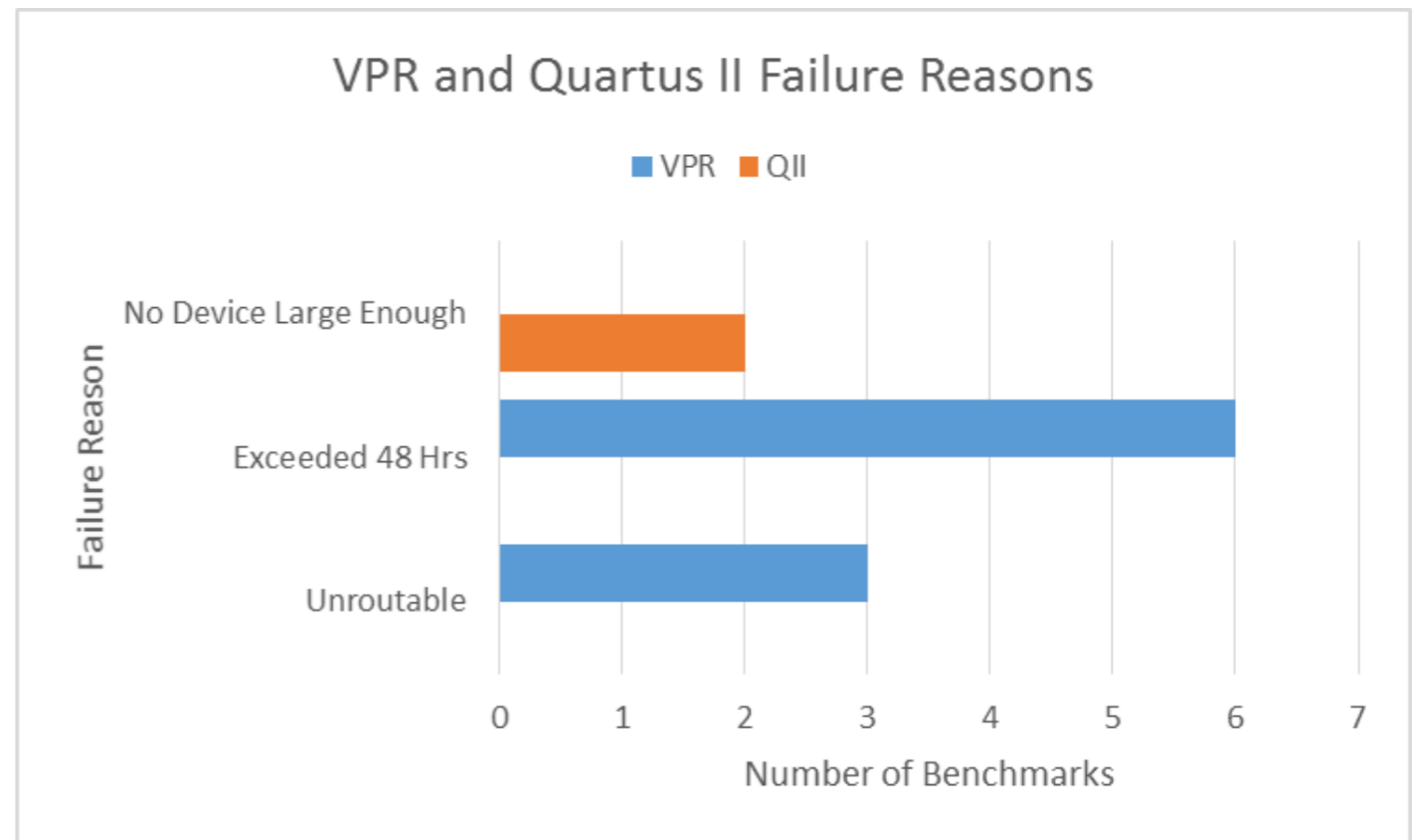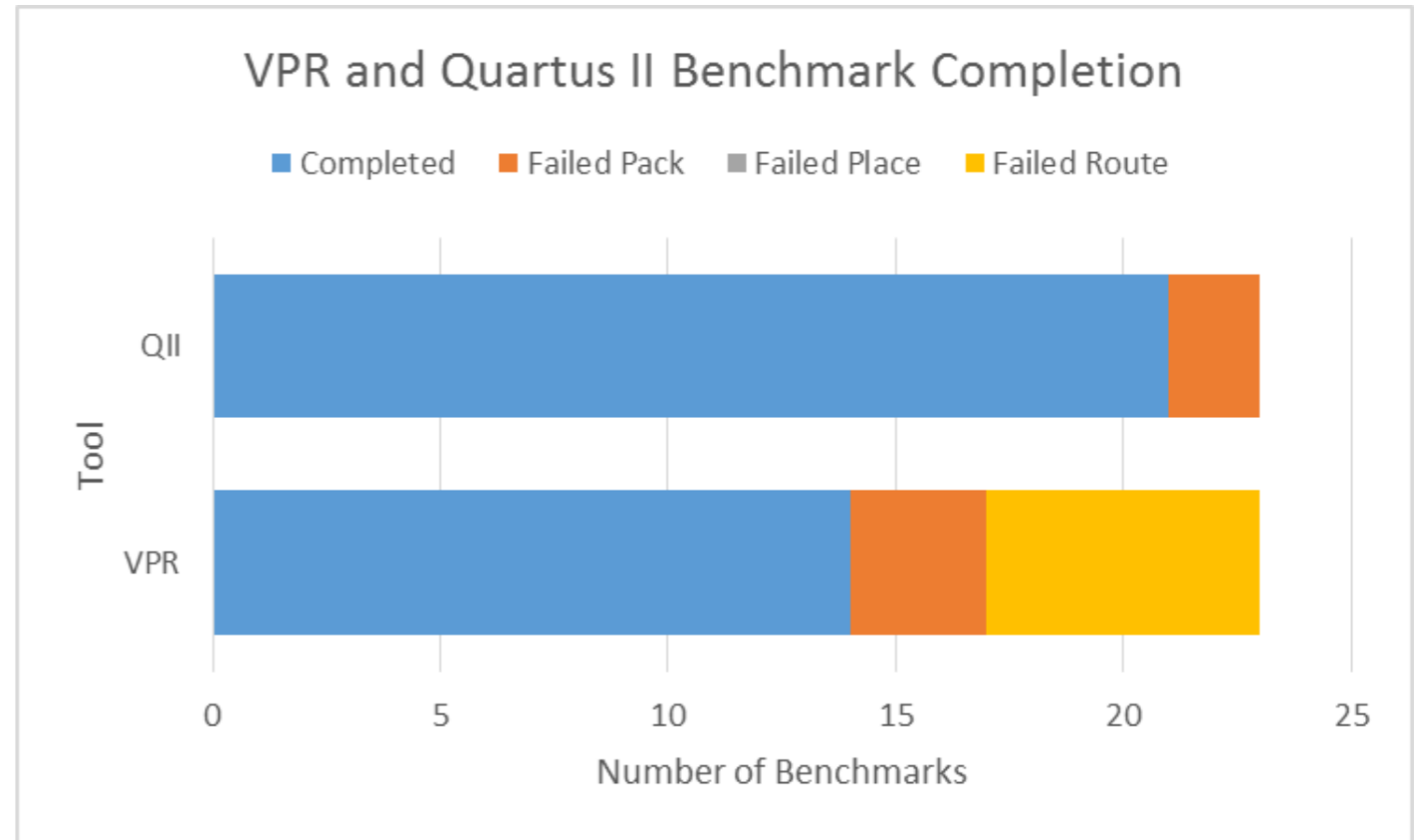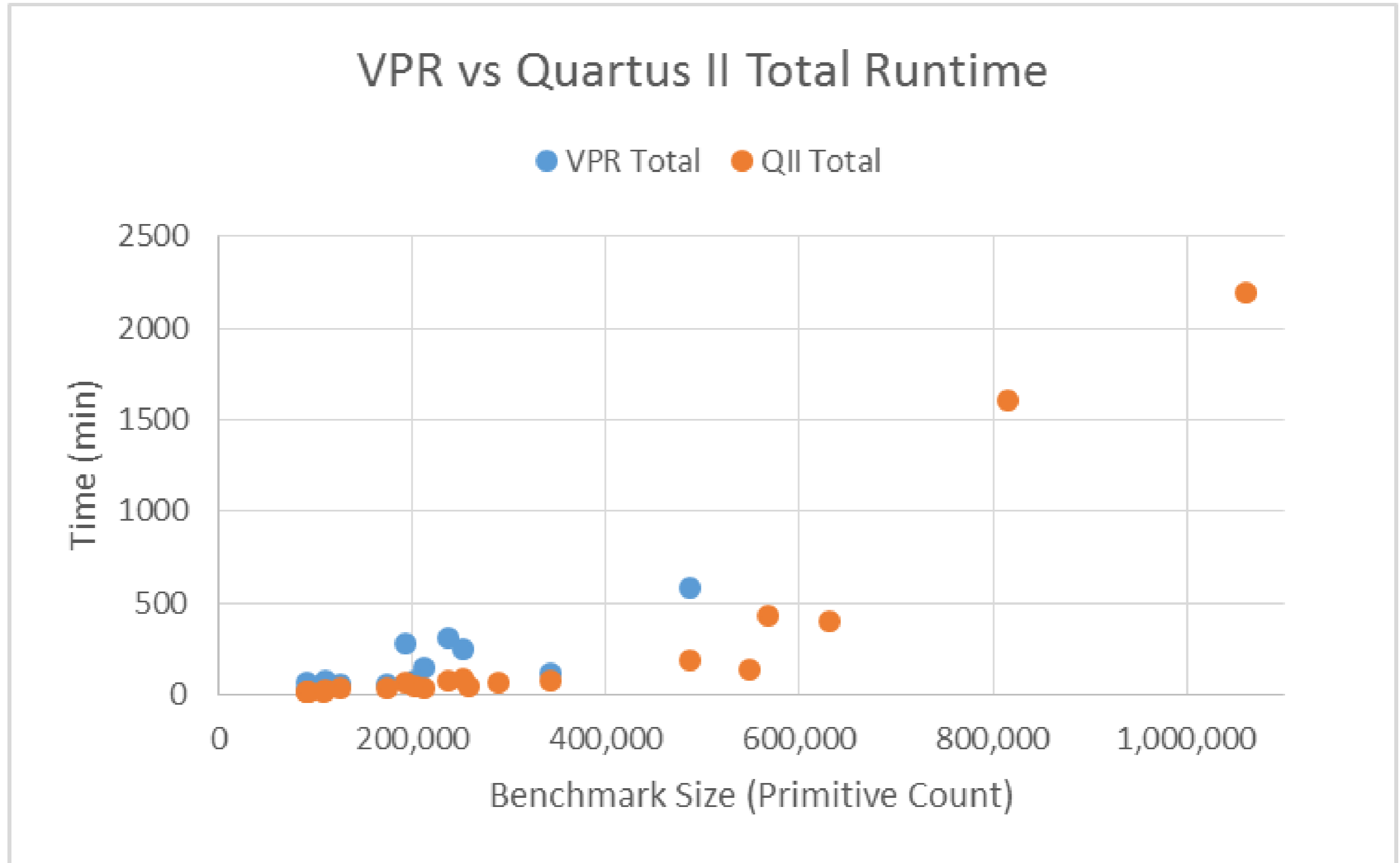- Extra routing flexibility for packing

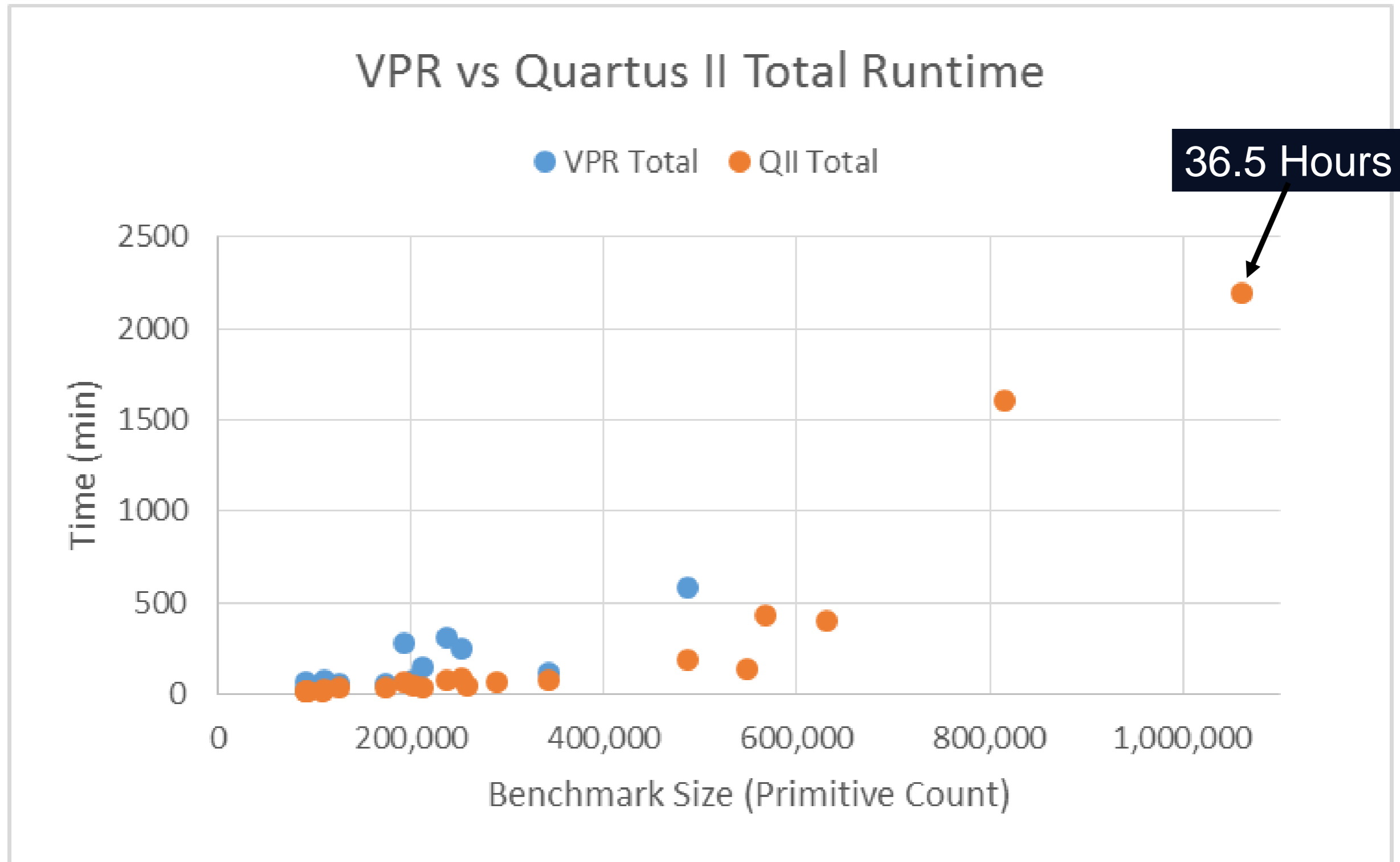**ALM Internal Connectivity**

Benchmark Completion

Tool	Benchmarks Completed
Quartus II	21/23
VPR	14/23

VPR and Quartus II Benchmark Completion

VPR and Quartus II Failure Reasons

Tool Performance vs. Benchmark Size

VPR vs Quartus II Total Runtime

Tool Performance vs. Benchmark Size

VPR vs Quartus II Total Runtime

● VPR Total   ● QII Total
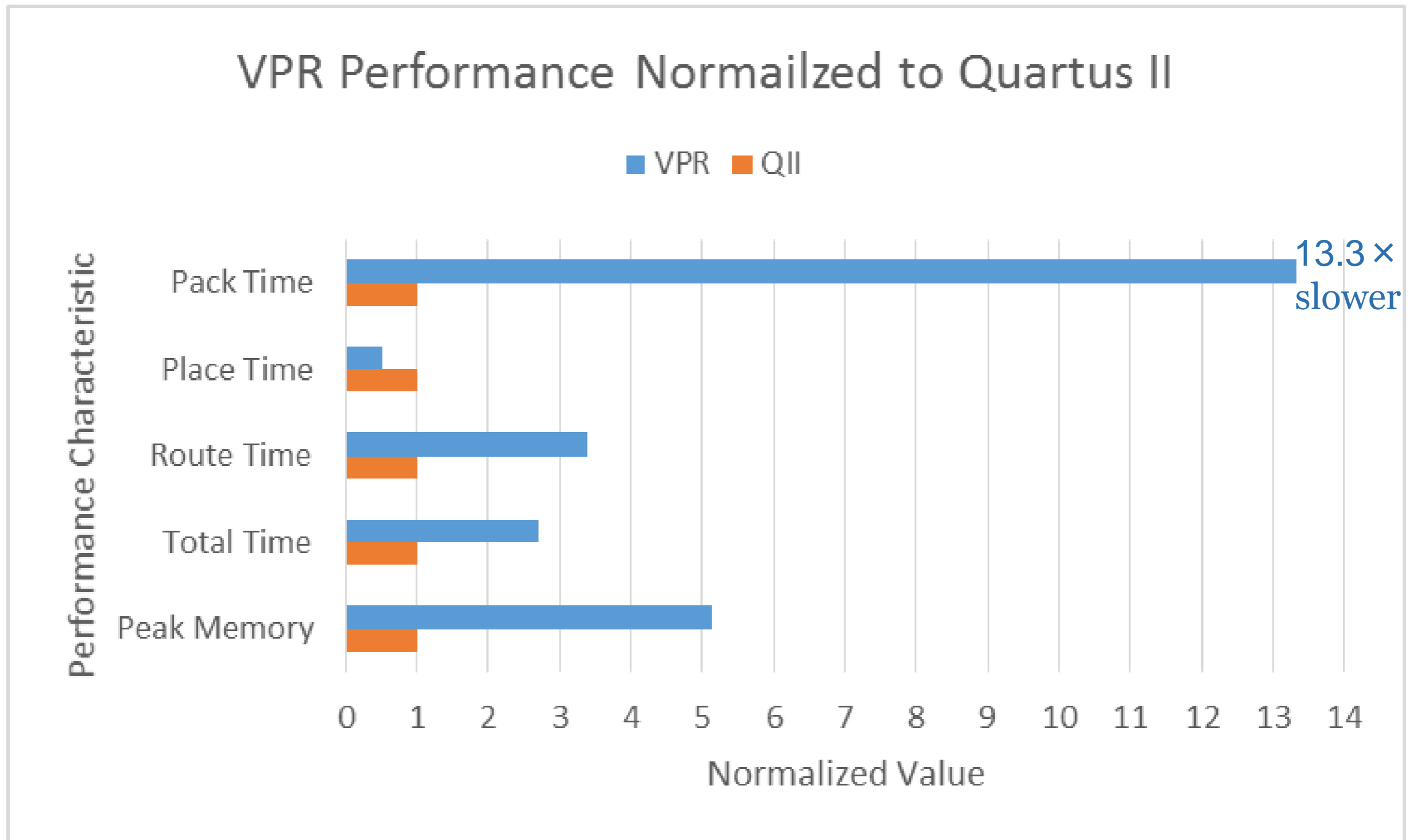
36.5 Hours

Tool Memory vs. Benchmark Size

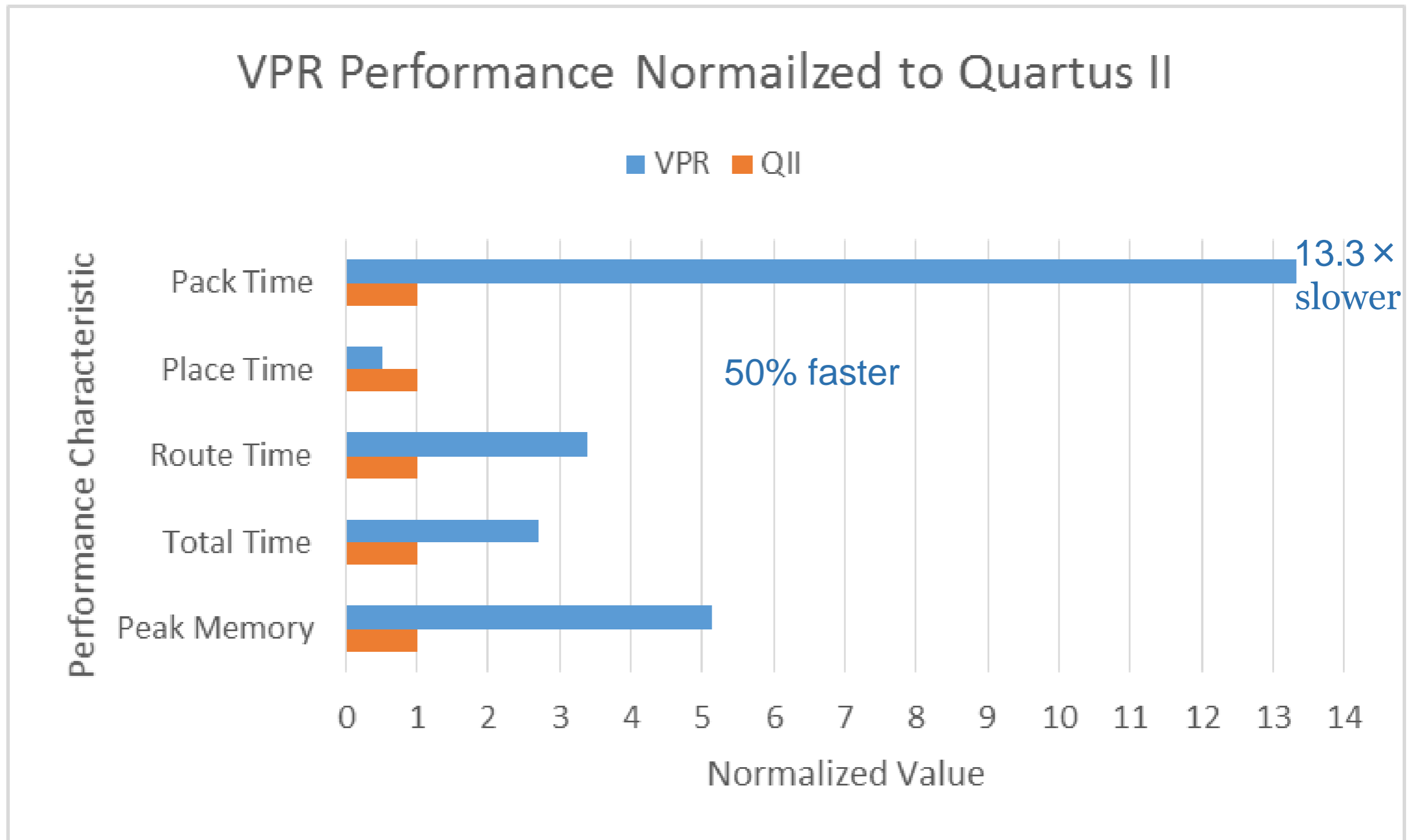# Normalized Performance

VPR Performance Normailzed to Quartus II
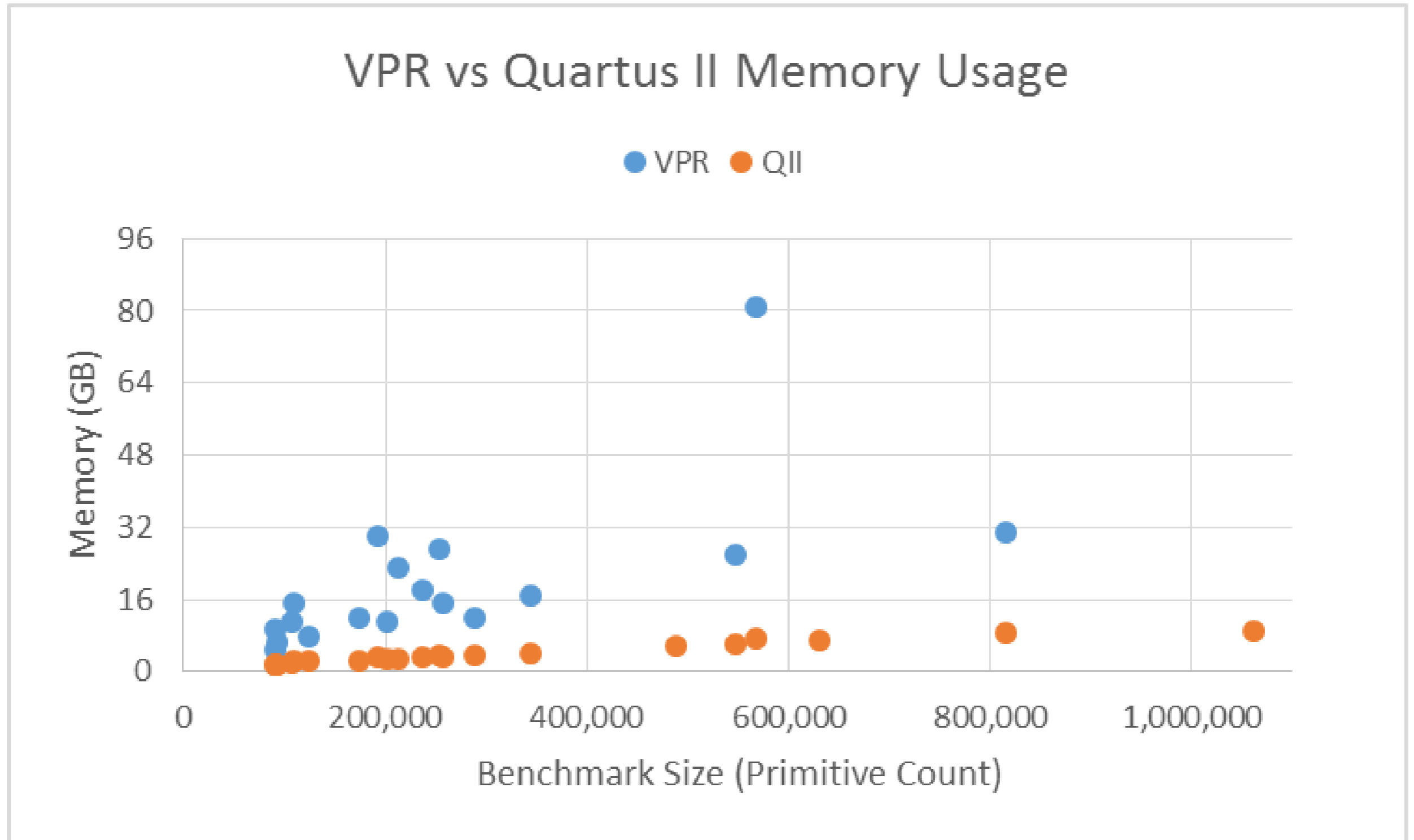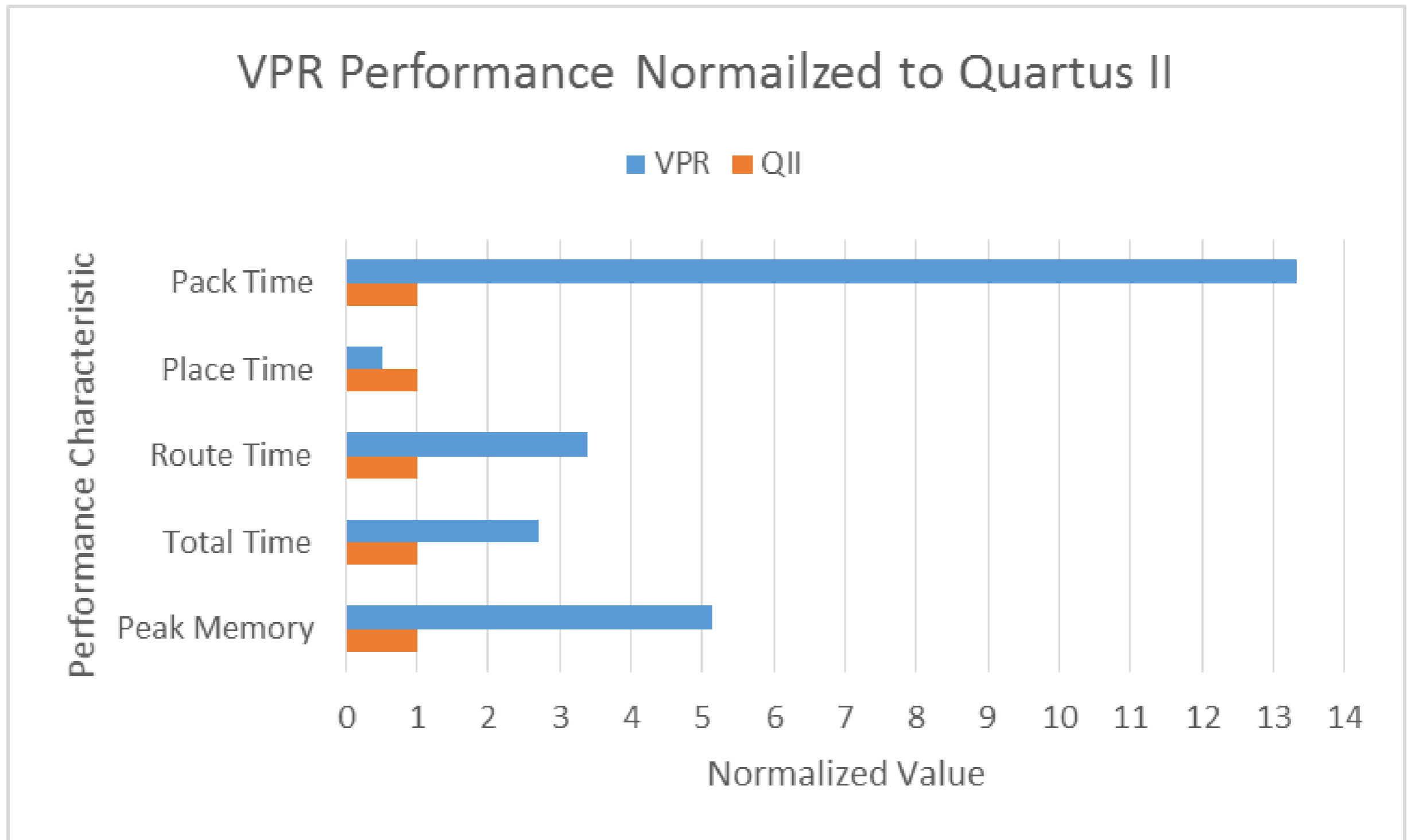
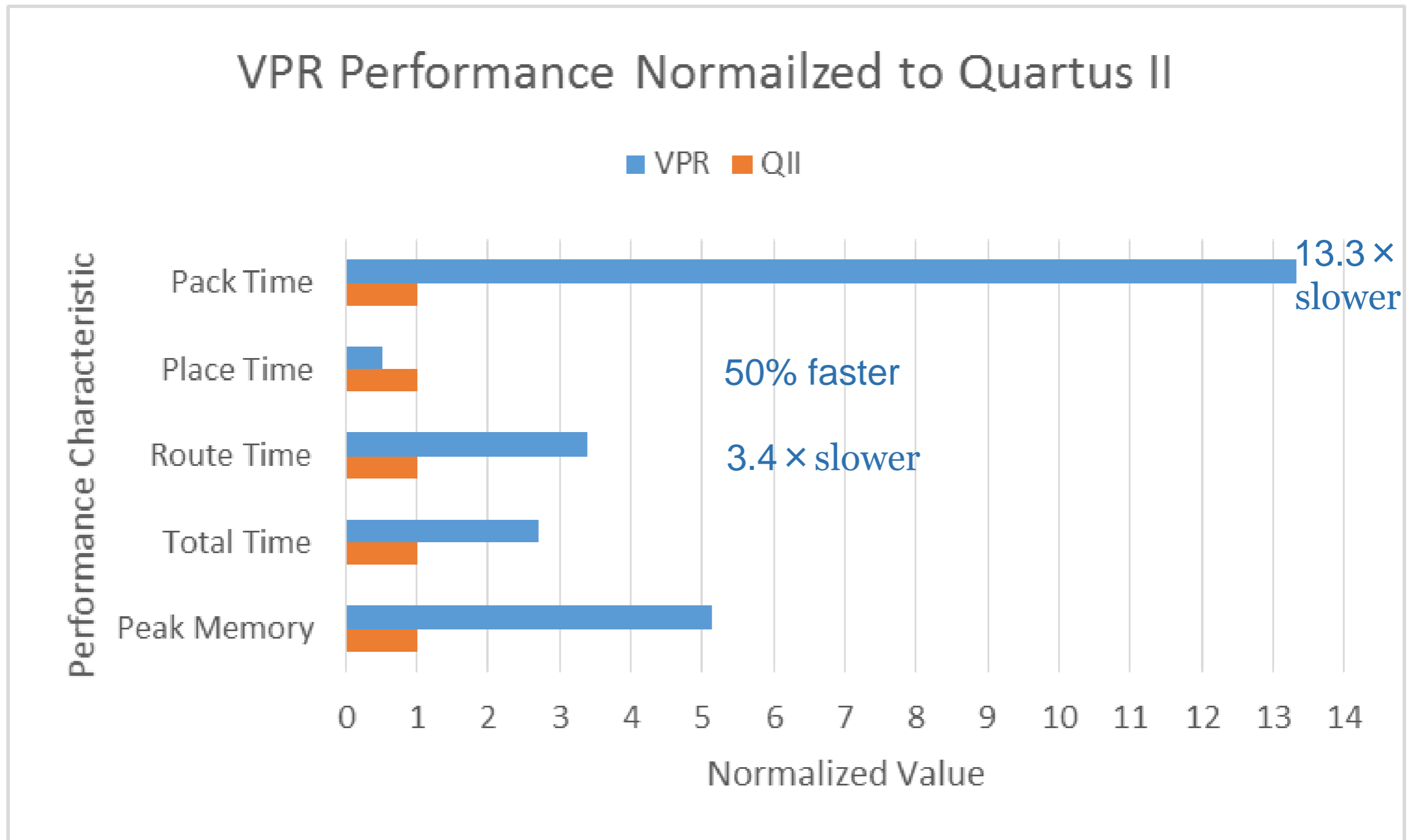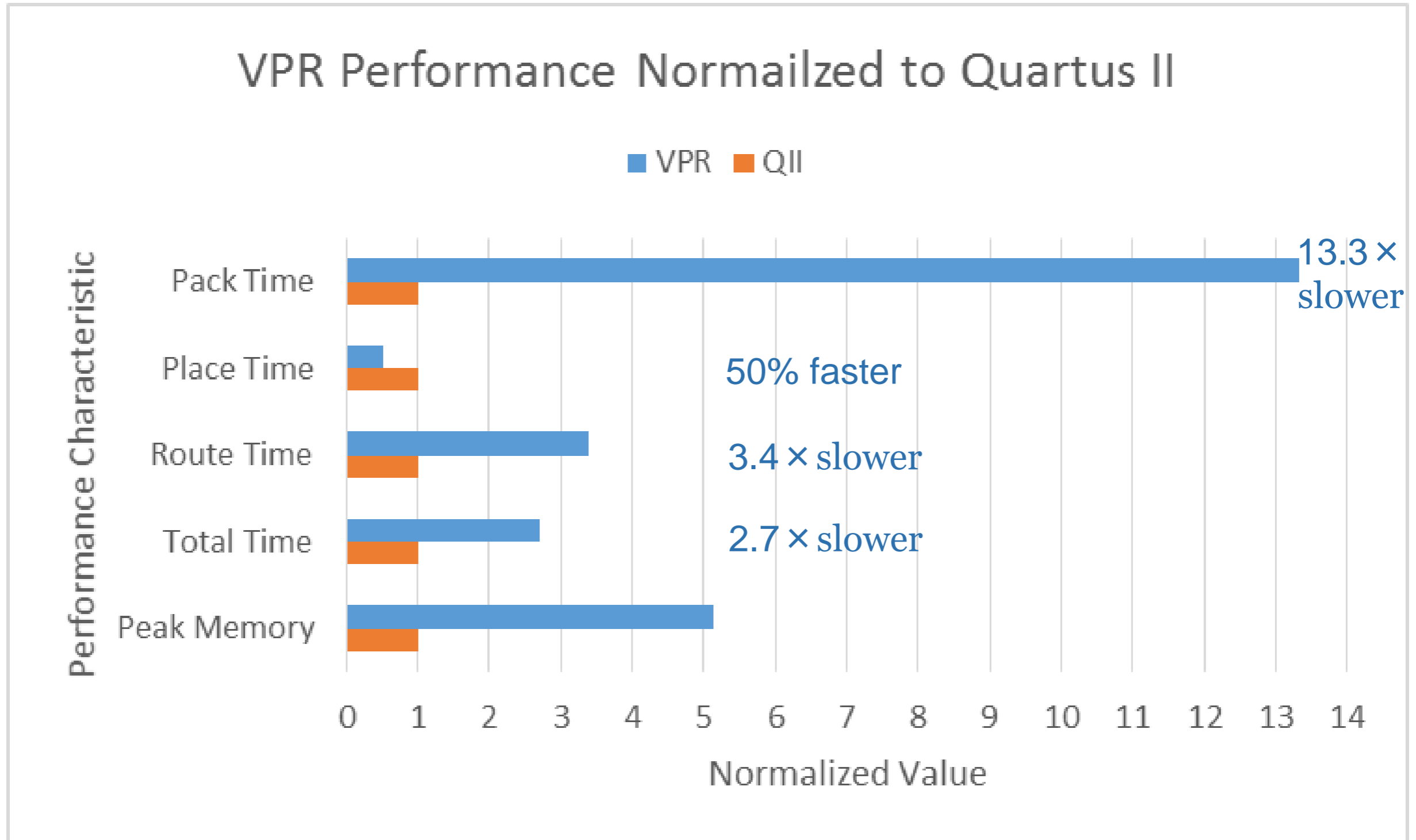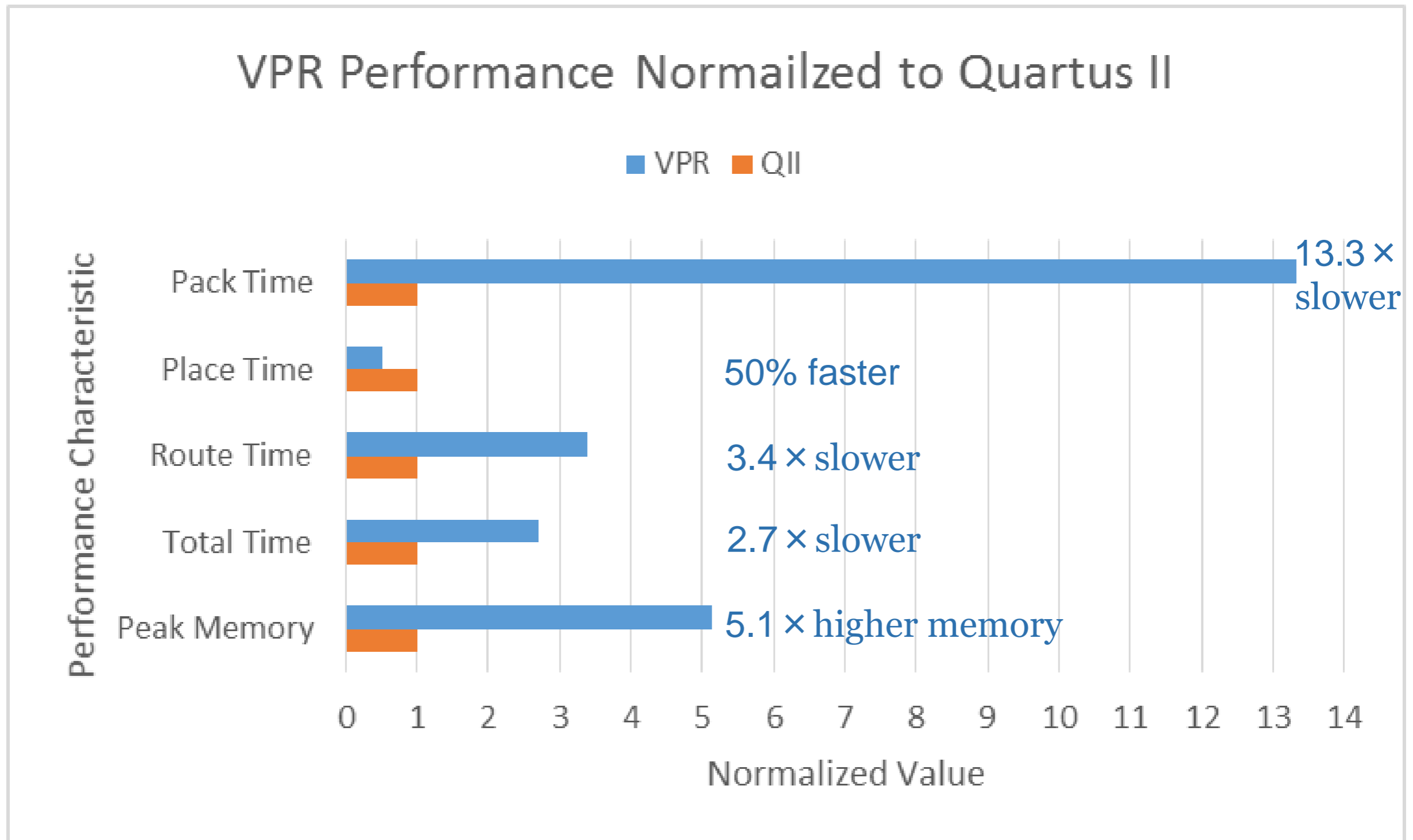# Normalized Performance

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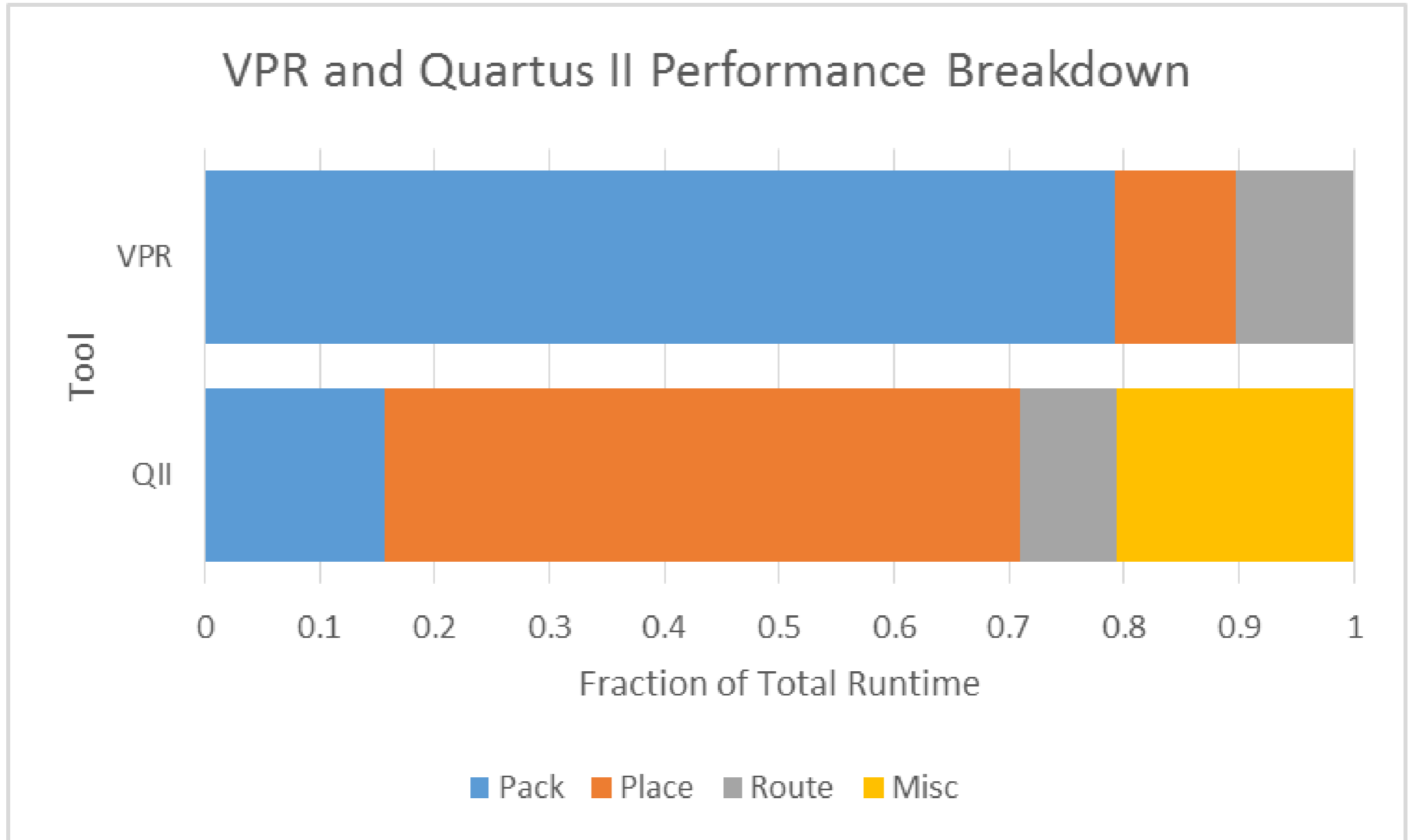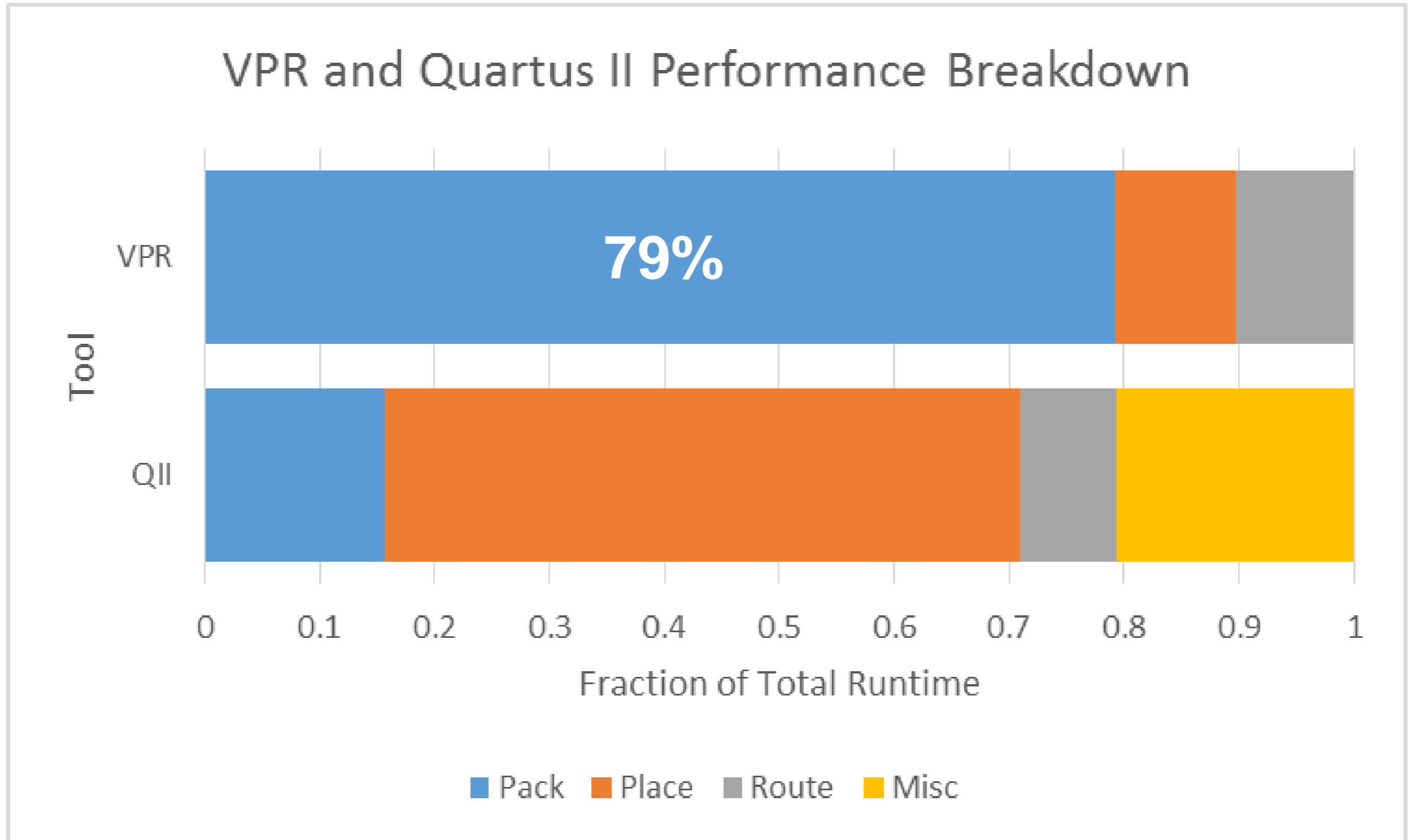VPR Performance Normailzed to Quartus II
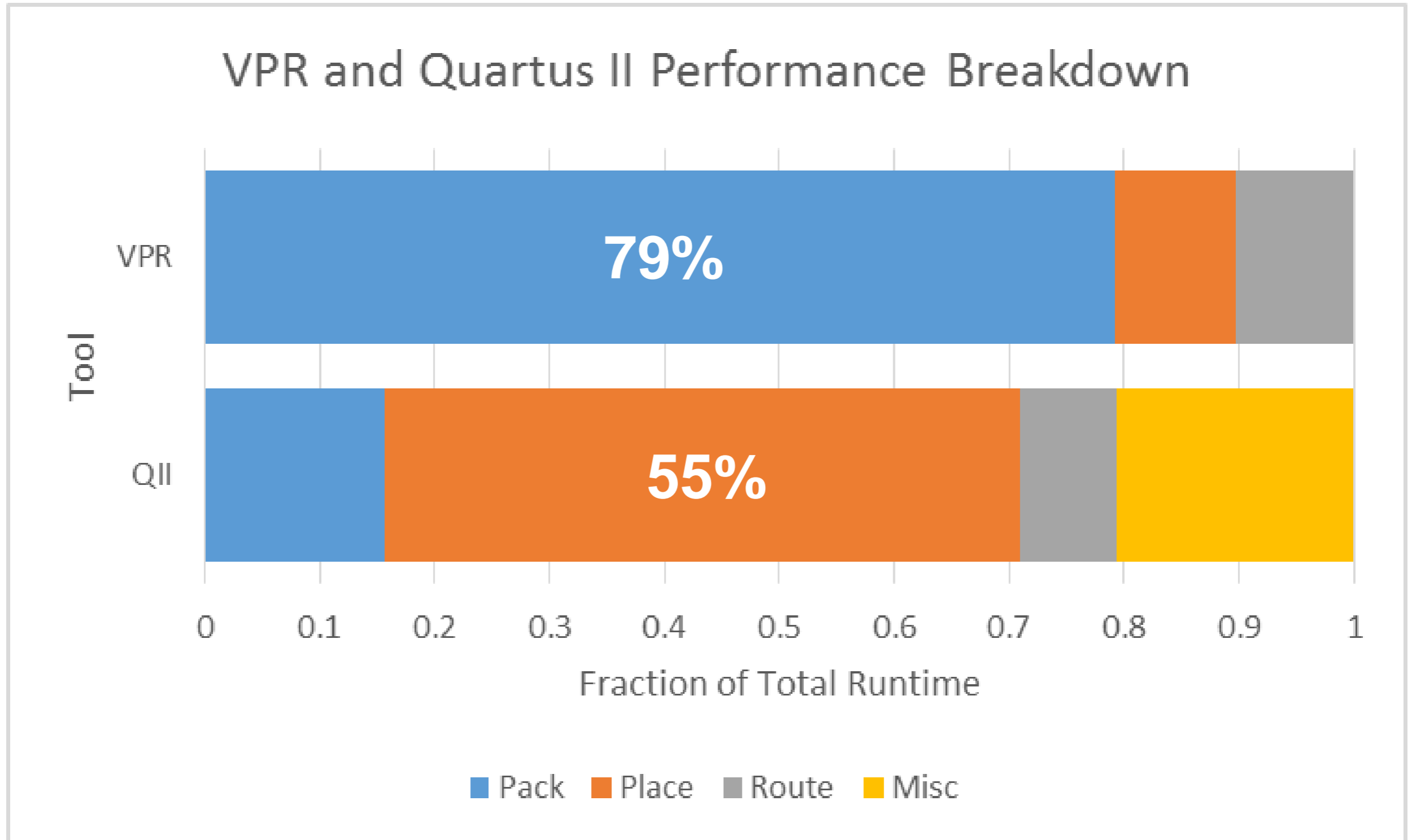
■ VPR ■ QII

13.3 × slower

50% faster

Normalized Performance

VPR Performance Normailzed to Quartus II

■ VPR ■ QII

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3.4 × slower

Normalized Performance

VPR Performance Normailzed to Quartus II

- VPR
- QII

13.3 × slower

50% faster

3.4 × slower

2.7 × slower

Normalized Performance

VPR Performance Normailzed to Quartus II

- VPR
- QII

Peak Memory — 5.1 × higher memory
Total Time — 2.7 × slower
Route Time — 3.4 × slower
Place Time — 50% faster
Pack Time — 13.3 × slower

Performance Characteristic (y-axis)
Normalized Value (x-axis): 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14

Performance Breakdown

VPR and Quartus II Performance Breakdown

Performance Breakdown

VPR and Quartus II Performance Breakdown

Tool: VPR — 79%
Tool: QII

Fraction of Total Runtime

Legend: Pack, Place, Route, Misc

Performance Breakdown

Performance Breakdown

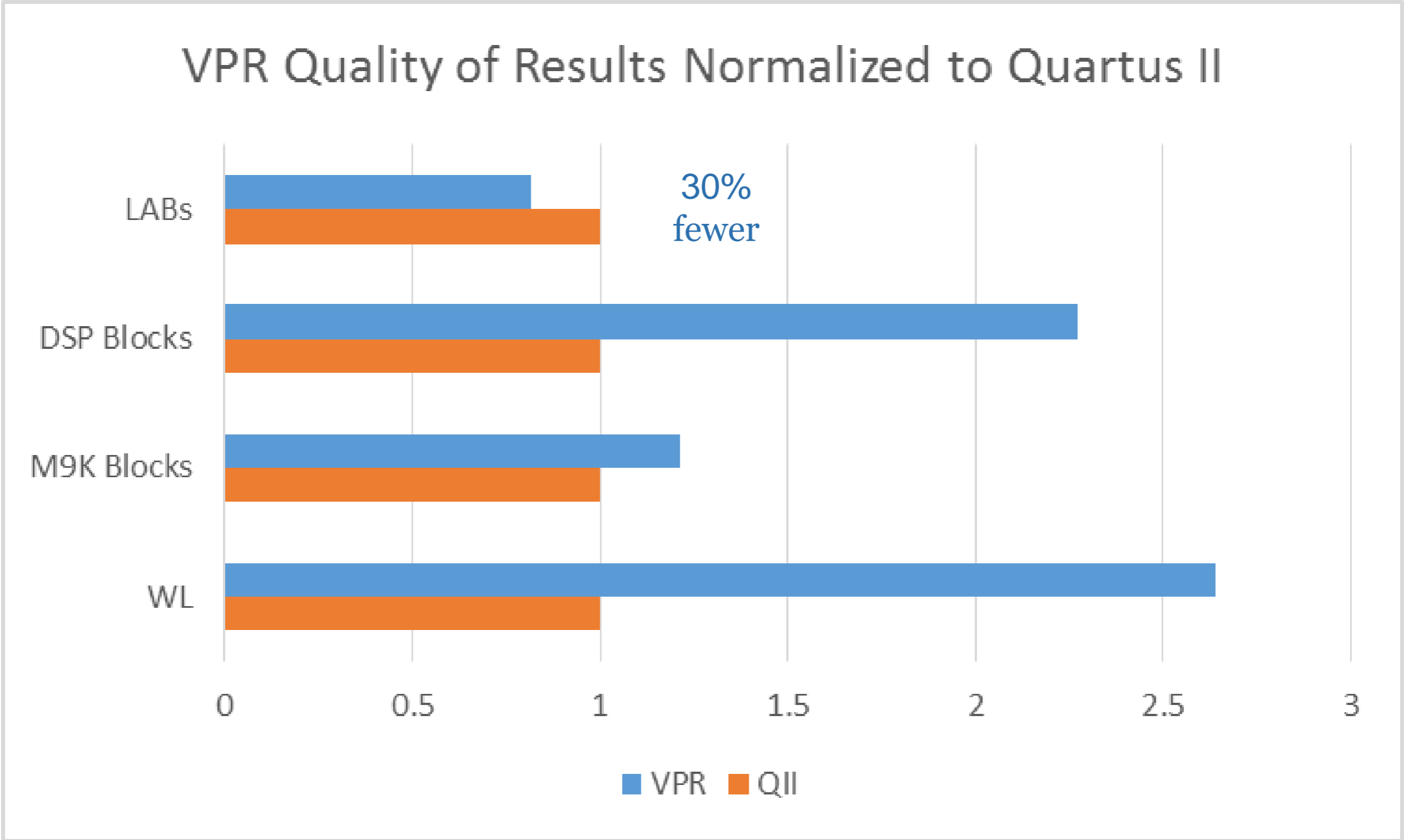VPR and Quartus II Performance Breakdown

Normalized Quality of Results
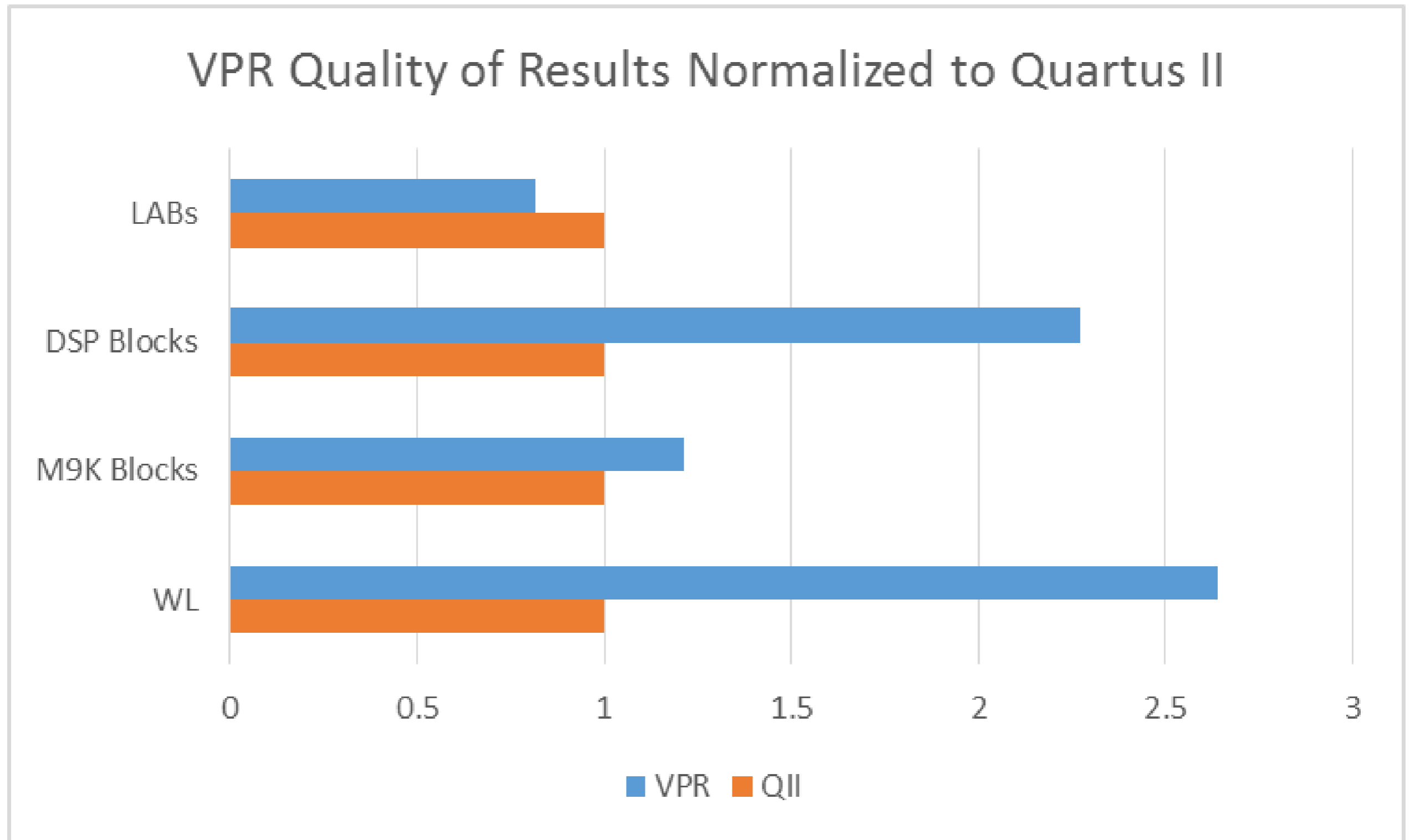
VPR Quality of Results Normalized to Quartus II

Normalized Quality of Results

VPR Quality of Results Normalized to Quartus II

Normalized Quality of Results

VPR Quality of Results Normalized to Quartus II

Normalized Quality of Results

VPR Quality of Results Normalized to Quartus II

- 30% fewer
- 2.3× more
- 1.2× more

Legend: VPR, QII
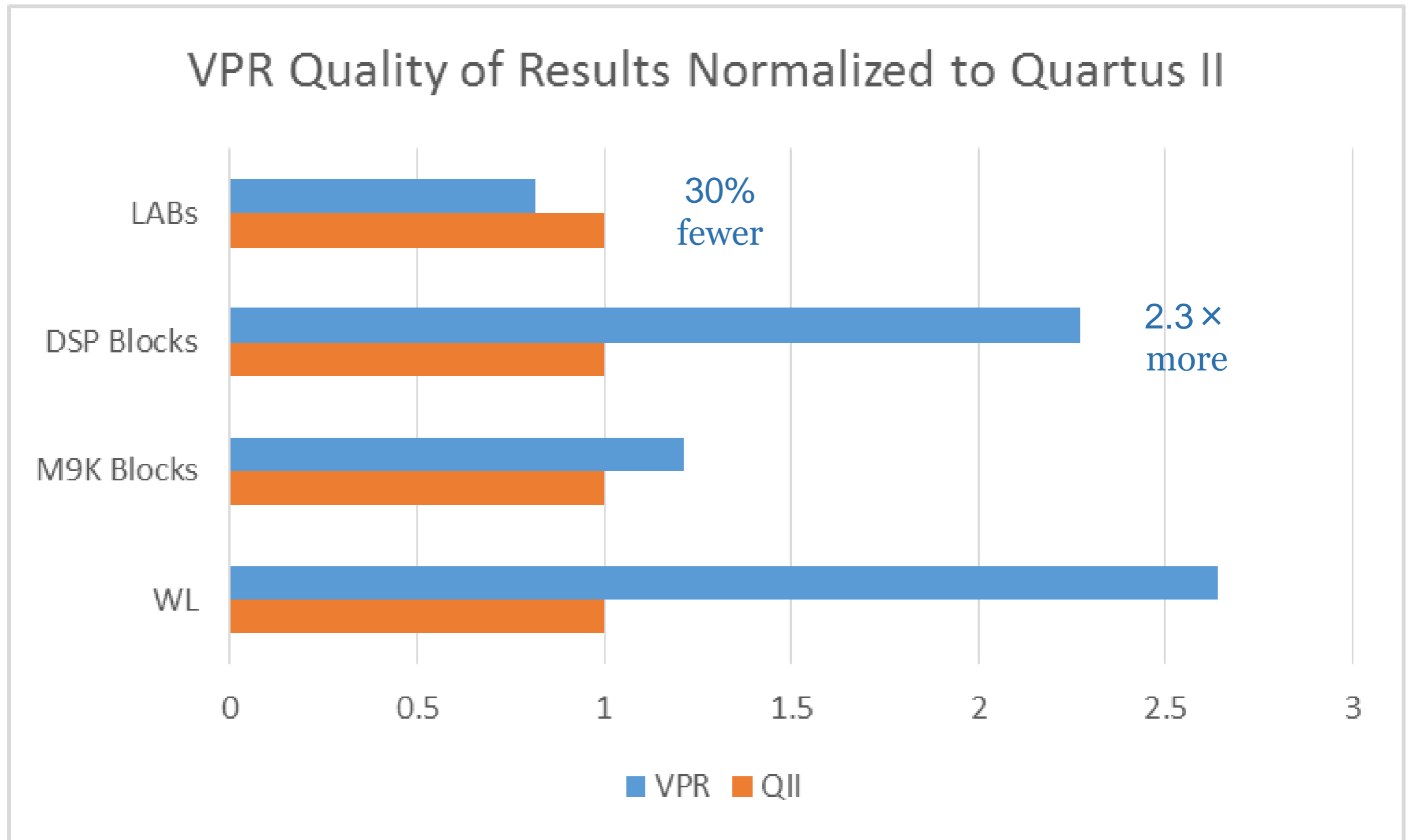
Normalized Quality of Results

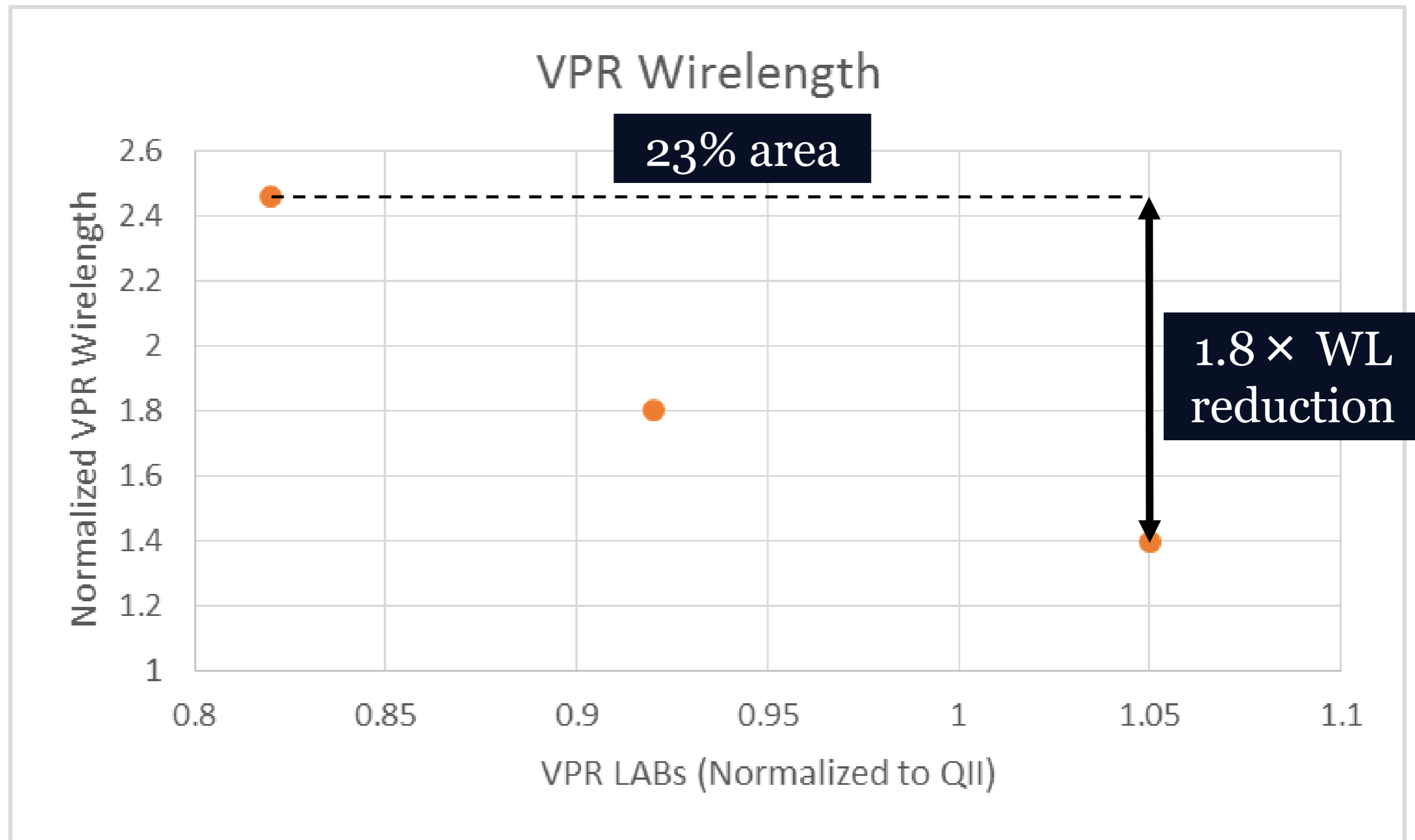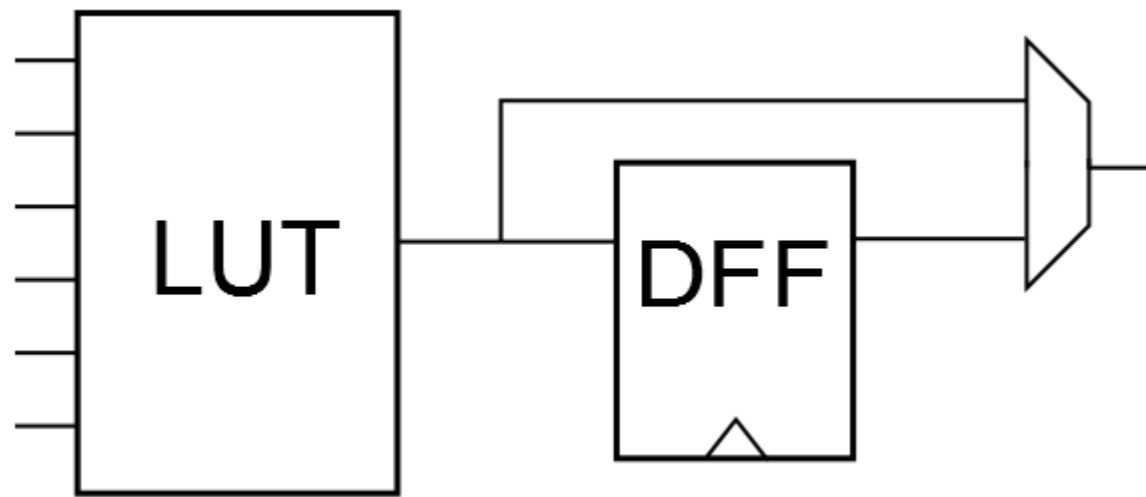VPR Quality of Results Normalized to Quartus II
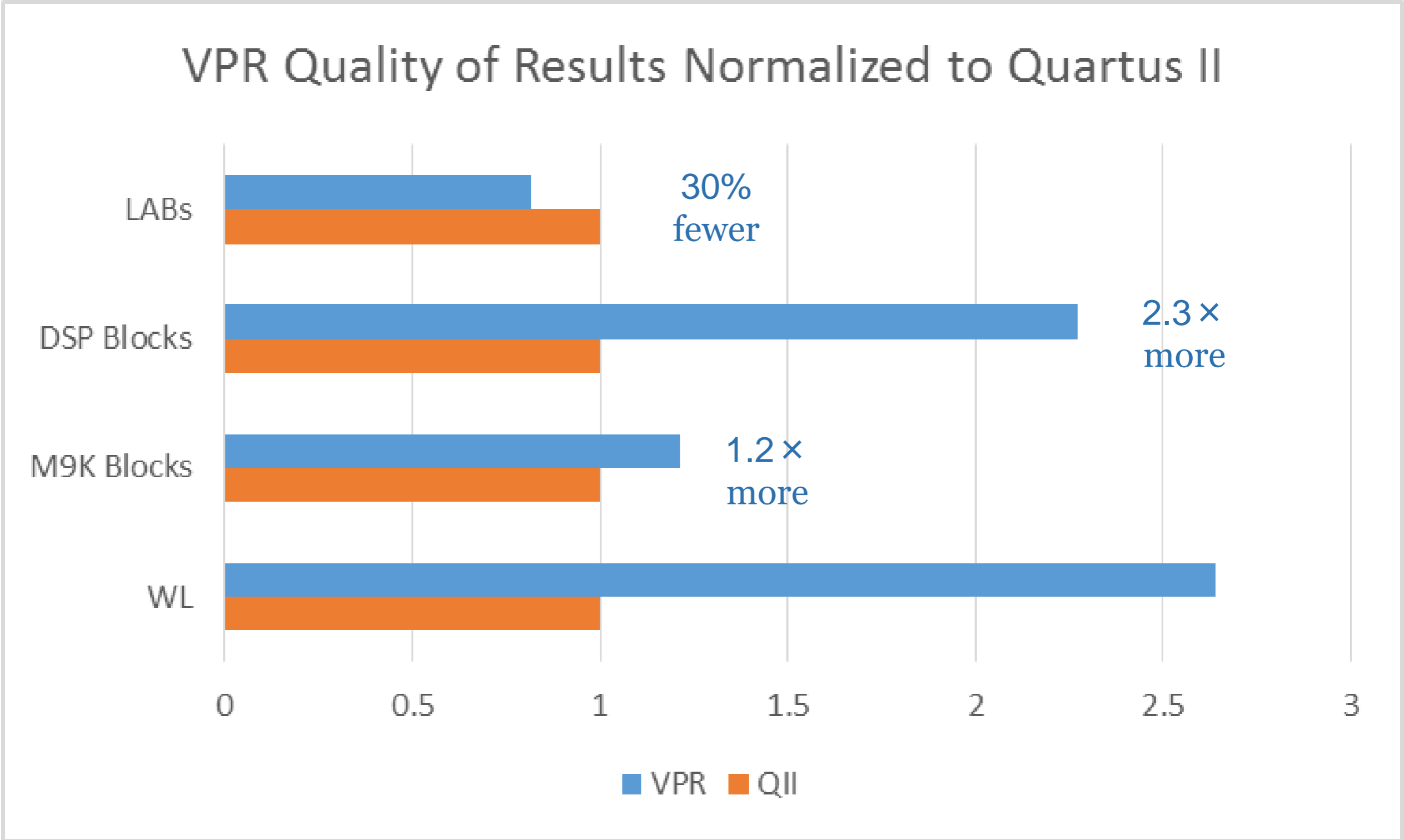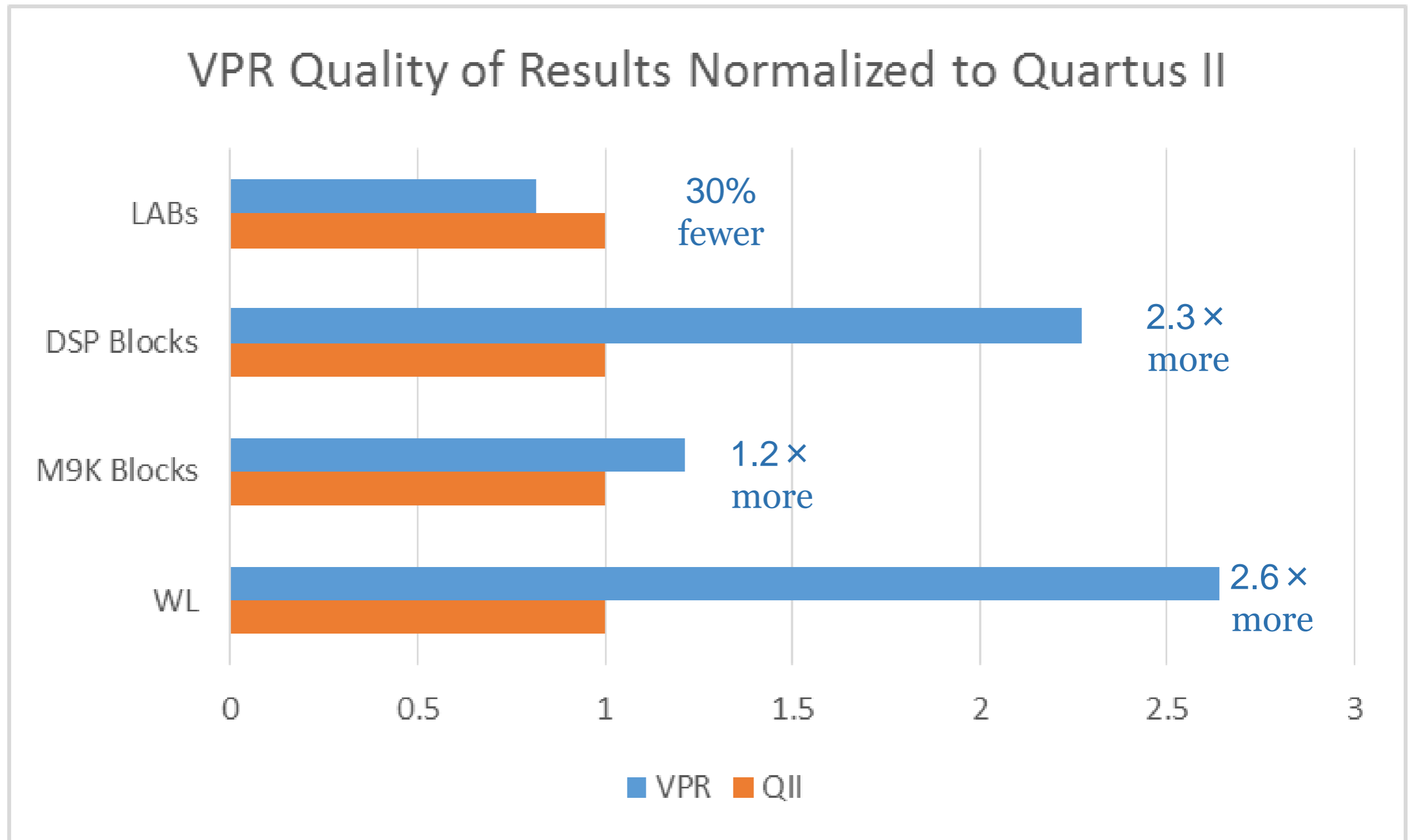
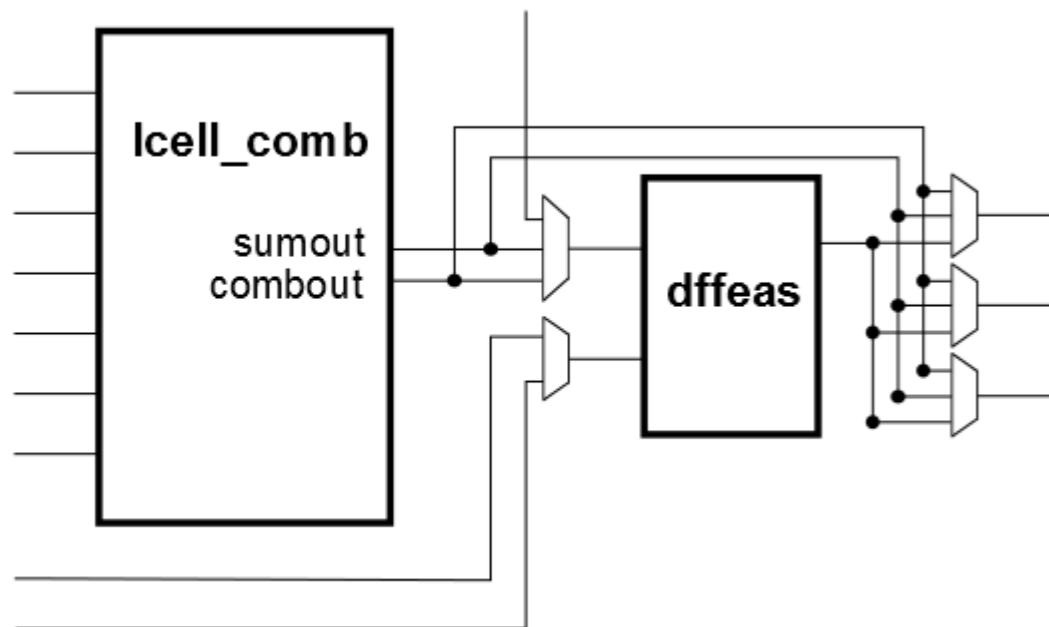# Impact of Clustering
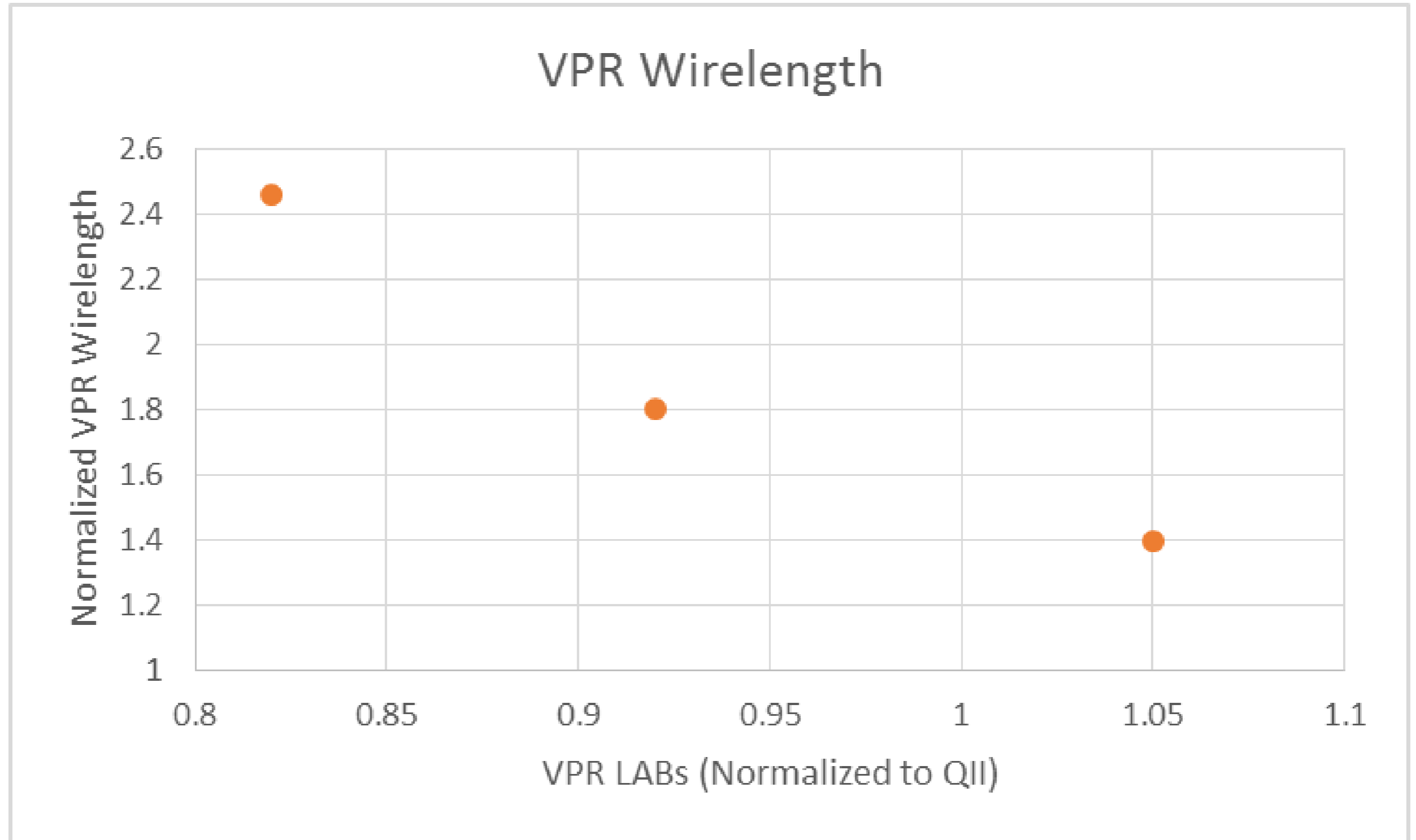
Impact of Clustering

Stratix IV & Academic LUT/FF Flexibility

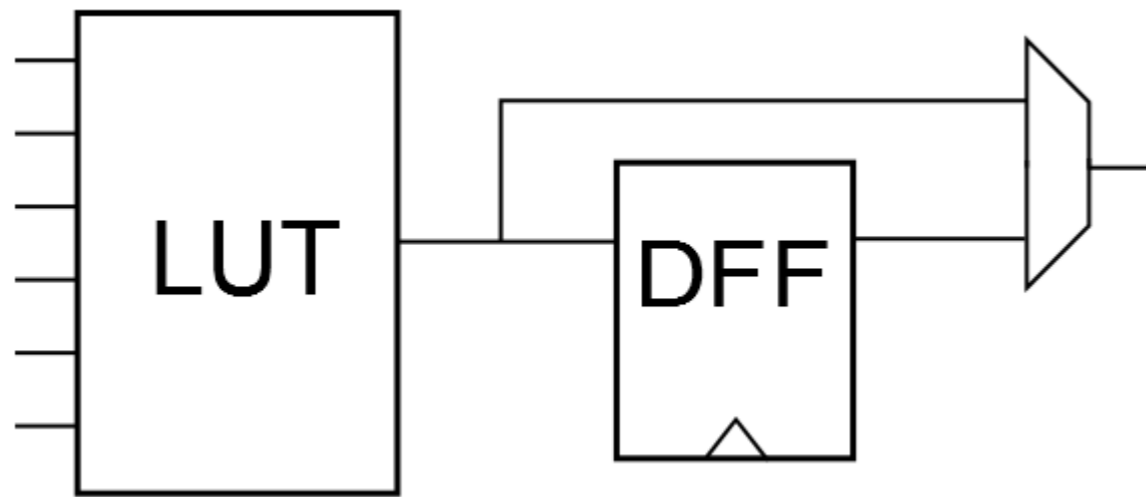**Traditional Academic BLE**

- Additional flexibility in Stratix IV architecture allows for denser packing
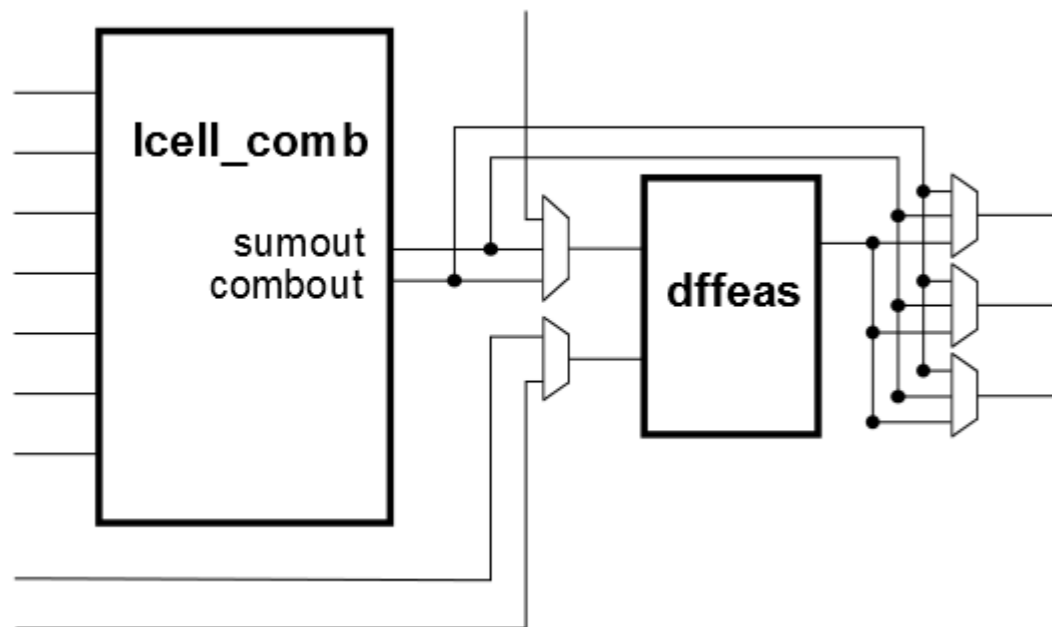
- Can be detrimental to Wirelength

Stratix IV like Half-ALM

Stratix IV & Academic LUT/FF Flexibility

Traditional Academic BLE

Stratix IV like Half-ALM

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Tight Packing, Higher Wirelength

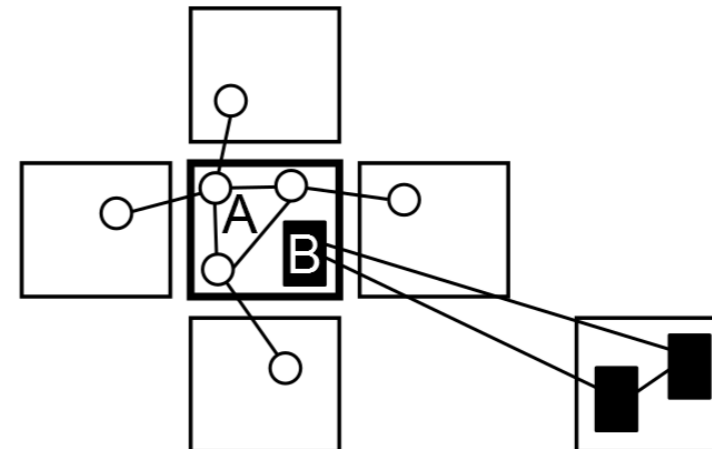# Stratix IV & Academic LUT/FF Flexibility

Traditional Academic BLE

Stratix IV like Half-ALM
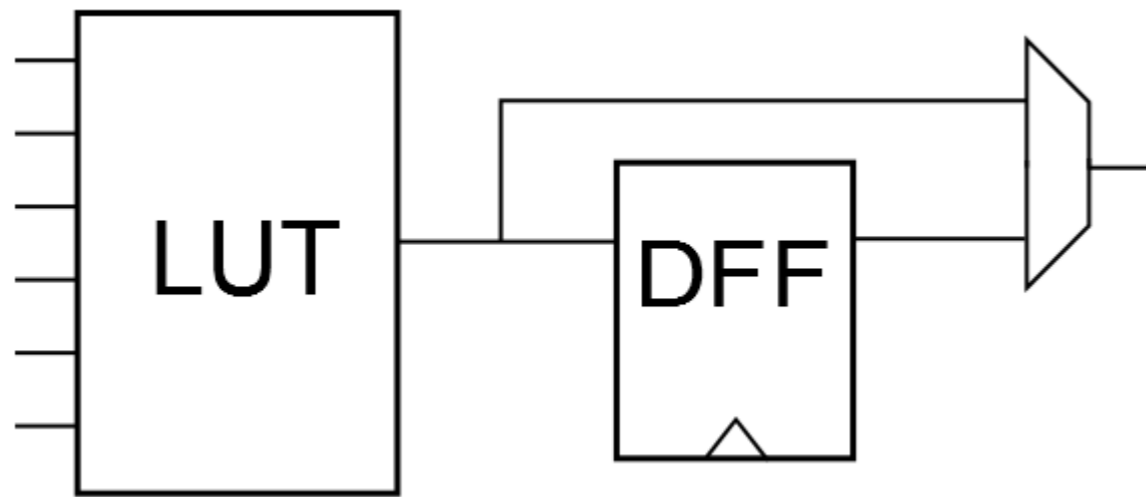
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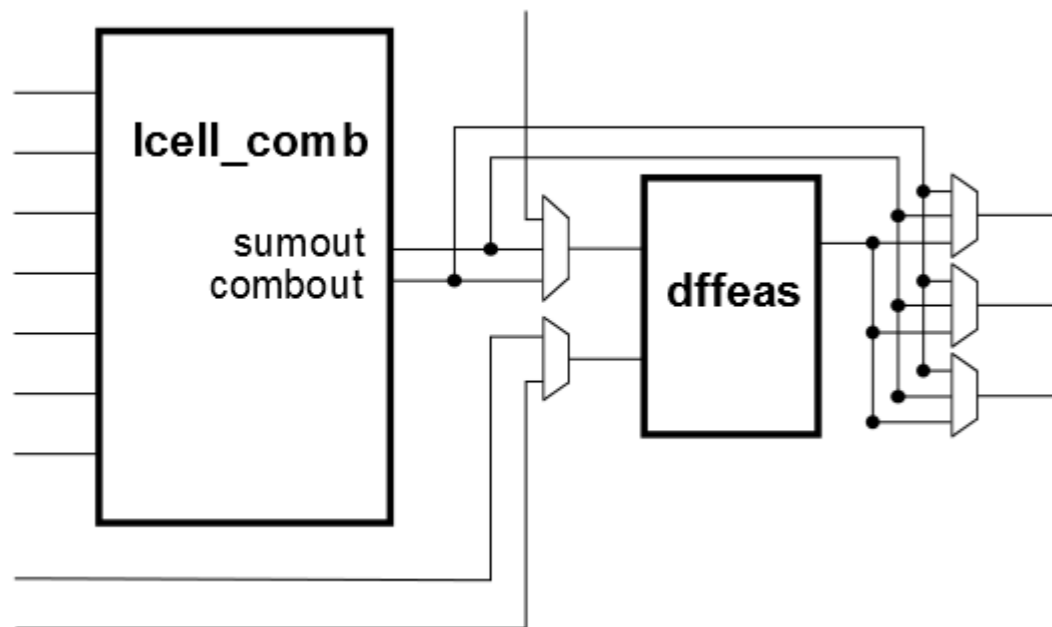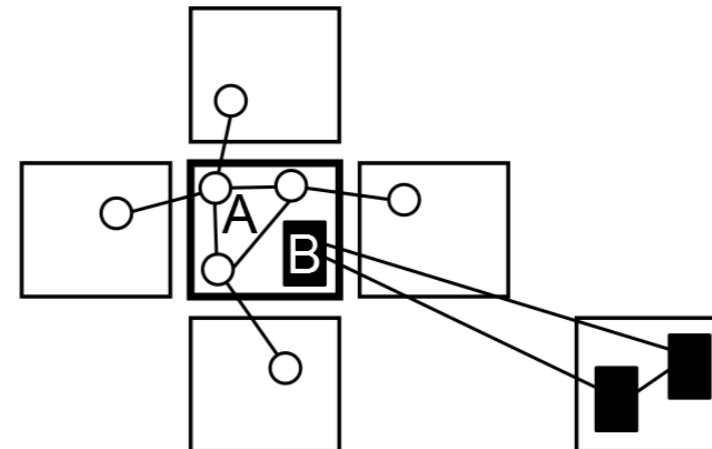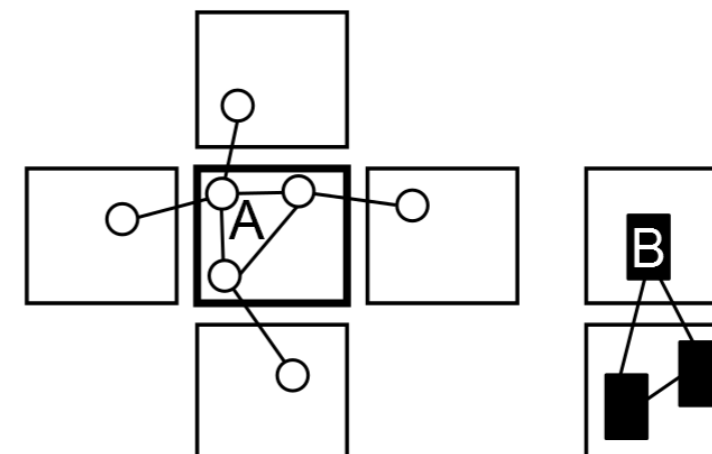
- Can be detrimental to Wirelength

Tight Packing, Higher Wirelength

Loose Packing, Lower Wirelength

Conclusion and Future Work

Conclusion

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- Titan Flow

  - Hybrid CAD Flow

  - Enables academic tools to use large benchmarks

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- Titan23 Benchmark Suite

  - Significantly improves open-source FPGA benchmarks

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- Titan23 Benchmark Suite

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- Comparison of VPR and Quartus II

  - Stratix IV architecture capture

  - VPR: 2.7x slower, 5.1x more memory, 2.6x more wire

  - Identified packing density as an important factor in wirelength

Future Work

- Timing Driven Comparison

Thanks! | Questions?

Email: kmurray@eecg.utoronto.ca

Titan Flow & Titan 23 Benchmarks:

http://uoft.me/titan

Demo Night:

From Quartus to VPR: Converting HDL to BLIF with the Titan Flow

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