ECE1352 Reading Assignment

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I-Q Quadrature Generator

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Modern communication systems use In-Phase (I) and Quadrature (Q) signals for modulation and demodulation. This requires accurate local oscillator (LO) outputs. The rapid growing mobile communication systems provide large demands on a wide range of RF transceivers in both base stations and mobile handsets. The soon to appear on the market, there will be third-generation cellular systems Universal Mobile Telecommunication System (UMTS), Universal Wireless Communications (UWC-136), and Code Division Multiple Access 2000 (cdma2000), are merged in the International Mobile Telecommunications 2000 (IMT-2000) Standard [1]–[3]. It apparently will push a lot of efforts on new chip sets with significant fast chip-rate (5MHz used in W-CDMA system and cdma2000), less power consumption, and minimal size in the new-generation handsets to have high-speed data and video on the cellular phone. The recent surge in applications of radio frequency (RF) transceivers has been accompanied with aggressive design goals: low cost, low power dissipation, and small form factor [4]. These goals also apply to the design of quadrature generators.

I. QUADRATURE SIGNAL GENERATION BASICS

Traditionally, the I–Q outputs are generated either by using a *RC-CR* phase shifter together with power-consuming phase correction circuits [5], or by running the LO at twice the desired frequency (or employing a frequency doubler) and using the I–Q outputs of a flip-flop frequency divider.

1. *RC-CR* Network

A simple example of quadrature technique is to shift signal phases by $\pm 45^0$ by using *RC-CR* network (Fig. 1). It can be easily seen that the phase differences between V_{out1} and V_{out2} is 90^0 for all frequencies. The output amplitudes are equal on at $w = 1/(RC)$. Since the absolute value of RC varies with temperature and process, the frequency varies at the point of equal-amplitude quadrature signals. The amplitudes can be equalized by means of "limiting stages, e.g. differential pairs in LO path. Amplitude limiting becomes difficult in Gigahertz circuits unless several stage are placed in cascade [6]. It turns out that the phase and gain mismatch of the chains of limiters in I and Q paths will become significant.

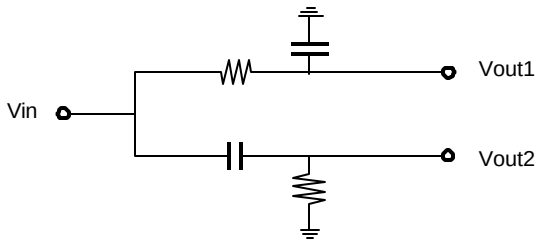

Fig. 1 Quadrature network using RC-CR circuit

Limiting stages entail "AM-to-PM conversion." In general, a nonlinear circuit with finite bandwidth exhibits a delay that depends on the input slew rate [7]. Consider the case in Fig. 2, the capacitors are added as the limited bandwidth, and other parasitics are neglected. For a small-amplitude sinusoid with frequency w applied at the input, the output differential current is also close to a sinusoid with a phase shift of $|q_1| = \tan^{-1}(R_1C_1w)$. Consider the case of a large amplitude so that M_1 and M_2 switch

rapidly at their zero crossing of V_{in}. The differential output current will be close to a square wave with a delay of $R_1C_1 \ln 2$ and the phase shift equals to $|q_2| = R_1C_1w \ln 2$. It shows that the phase shift varies from $R_1C_1w \ln 2$ to $\tan^{-1}(R_1C_1w)$ corresponding to the slew rate of the input. In the limiting process, the phase is disturbed by amplitude variation, or in other words, AM-to-PM conversion. If the limiting stages do not provide adequate bandwidth, a difference in amplitudes will translate to a phase imbalance. That's the key point of quadrature generation.

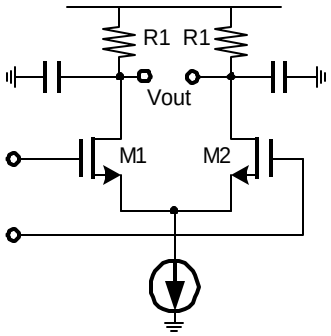

Fig. 2 Limiter with finite bandwidth

In Fig. 2, the mismatch of resistors and capacitors deviate the output phase difference, f, from 90^0. Assuming a relative resistor mismatch of a and capacitor mismatch of b, then we can express f in the vicinity of $w = 1/(RC)$ as

$$f = \frac{p}{2} - [\tan^{-1} R(1+a)C(1+b)w - \tan^{-1} RCw] \qquad (1)$$

$$= \frac{p}{2} - \tan^{-1}\frac{RCw(1+a)(1+b) - RCw}{1 + RCw(1+a)(1+b)RCw}$$
$$\approx \frac{p}{2} - \tan^{-1}\frac{a+b}{2} \qquad (2)$$
$$\approx \frac{p}{2} - \frac{a+b}{2}$$

If $a = b = 1\%$, then the pulse imbalance is equal to $3.6/(2p) \approx 0.6^0$.

It shows that the phase and amplitude imbalances in Fig. 2 do not depend on the additional load capacitance. This is because such capacitance only impacts the poles of the circuit, whereas the phase difference arises from the zero in the upper path [8]. However, capacitive paths between the two outputs do introduce phase error, demanding careful layout [8].

2. Havens' Technique

Havens' technique first splits the signal by approximately 90^0, generating V_1 and V_2, and subsequently adds and subtracts these two phases, producing V_{out1} and V_{out2} [10] as

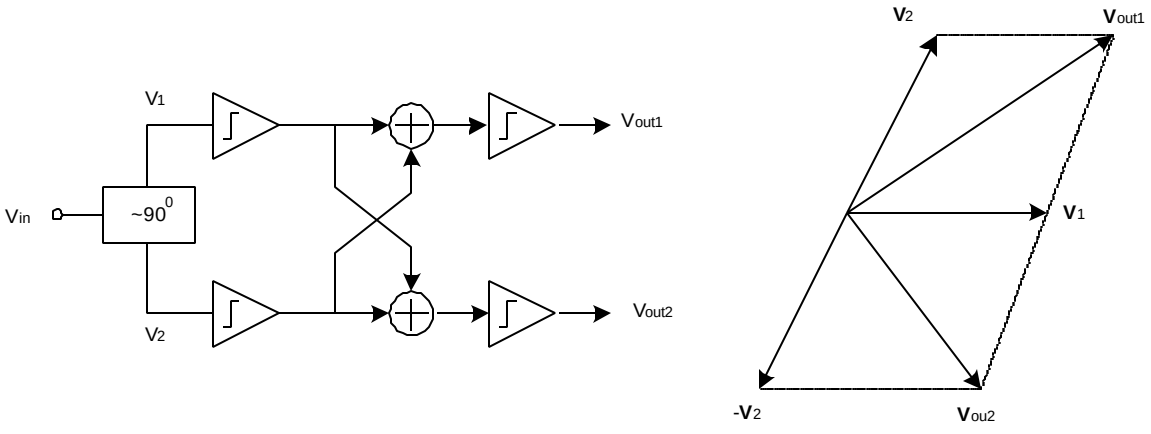

Fig. 3 (a) Havens quadrature circuit, (b) Phasor diagram

shown in Fig. 3(a). In Fig. 3(b), if V_1 and V_2 have equal amplitudes, the angle between V_{out1} and V_{out2} is equal to 90^0. This can be proved by expressing $v_1 = A\cos w\ t, v_2 = A\cos(w\ t + q)$, and then

$$v_1(t) + v_2(t) = 2A\cos\frac{q}{2}\cos(w\ t + \frac{q}{2}) \quad (3)$$

$$v_1(t) - v_2(t) = 2A\sin\frac{q}{2}\sin(w\ t + \frac{q}{2}) \quad (4)$$

The limiting stages will equalize the amplitudes of v_1 and v_2 by phase shift circuit. Moreover, the adders' outputs will have different amplitude if $q \neq 90^0$. These both applied to limiters, and AM-to-PM conversion becomes main concern.

Consider the signals that are sensed by adders shown in Fig. 3(a), and assume $v_2(t) = (A+e)\cos(w\ t + q)$, where e represents the mismatch of amplitudes. The diagram in Fig. 3(b) will be drawn as Fig. 4 and

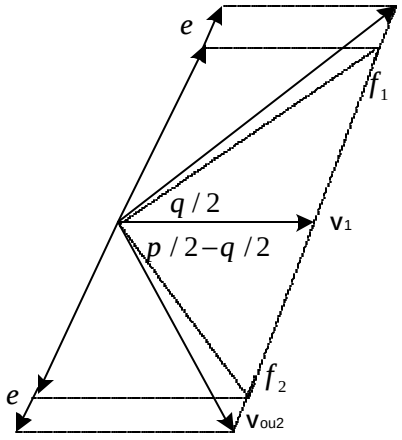

Fig. 4 Effect of amplitude mismatch in the havens circuit

$$\tan f_1 = \frac{e \sin(q/2)}{2A\cos(q/2) + e\cos(q/2)} \tag{5}$$

$$\tan f_2 = \frac{e \cos(q/2)}{2A\sin(q/2) + e\sin(q/2)} \tag{6}$$

When $e << A$, then

$$f_1 + f_2 \approx \frac{e}{2A}\left[\frac{\sin(q/2)}{\cos(q/2)} + \frac{\cos(q/2)}{\sin(q/2)}\right] \tag{7}$$

$$= \frac{e}{A}\frac{1}{\sin q} \tag{8}$$

It indicates that 1% amplitude mismatch turns out 0.6^0 of phase error.

Another amplitude mismatch in Havens topology is the capacitive coupling between the inputs of adders. When v_1 and v_2 are applied to limiting and subsequently an adder by two differential pairs, the gate-drain overlap capacitance of the transistors provide a path from I channel to Q channel to pull the quadrature phases together. This may have significant effect in the phase imbalance at the input if output impedance of the limiter is not low.

3. Frequency Division

There is another approach to generating quadrature signals by using frequency w_1. The circuit is to use a master-slave flipflop to divide a signal at $2w_1$ by a factor of 2, seen in Fig. 5. If V_{in} has a 50-50 duty cycle, then V_{out1} and V_{out2} are 90^0 out of phase. The

principle difficulty of this approach is that generation and division of the signal at $2w_1$ may consume substantial power or simply be impossible due to technology limitations. Another issue is the phase imbalance resulting from deviation of the input duty cycle from 50%. Mismatch in the signal path through the latches also contributes phase error [11].

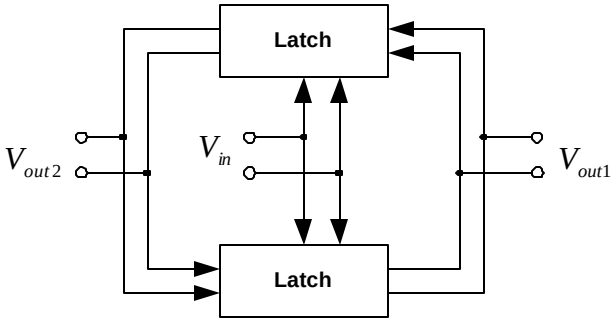

Fig. 5 Frequency divider as a quadrature generator

II. DESIGN CONSIDERATION

In modern I-Q oscillator design, alternatively complex topology adequate to tolerate high phase errors must be used. Voltage controlled oscillator (VCO) architectures that inherently produce I–Q components provide an attractive alternative.

Three design options are available to generate quadrature signals for VCOs.

1) Combination of VCO, polyphase-filter (or *R-C C-R* filter), and output buffers (or limiters) as used in, e.g.,[12], [13].
2) VCO at double frequency followed by master–slave flipflops.

3) Two cross-coupled VCOs as proposed in [14].

The first option needs four output buffers or limiters consuming a lot of power. If buffers are inserted between VCO and filters, even more power is needed; if the filters are directly connected to the VCO tank, tank capacitance is increased, leading to higher power consumption and worse phase noise [15]. Furthermore, a lot of chip area is needed, as the filters need good matching.

The second option has the smallest area. This option needs a VCO designed at double frequency, which should not consume more power, as a higher for integrated tanks at higher frequencies is achievable (Inductance scales down linearly when sizing down an integrated coil, coil capacitance scales down quadratically, so improves [15]). However, the master–slave flipflops, which have to be designed for the doubled frequency, consume too much power in current widely used CMOS technologies (0.25 m). As soon as next technology generations (0.18 m, 0.12 m) become available, this could change very rapidly. If primary design concern is low cost or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil and the area of the master–slave flipflops in submicron CMOS is negligible.

The third option comes at the cost of double VCO area. This option outperforms the other solutions in terms of power consumption, as soon as a well-designed VCO core consumes less power than the four output buffers or limiters of the first option, or as soon as the VCO core consumes less power than the master–slave flipflops designed for double

frequency needed to realize the second option. The two-core solution, furthermore, provides a very high voltage swing, which eases the design of prescaler and mixer circuits connected to the VCO. This consideration can also be extended to VCOs using external high-quality inductors. When using external inductors, a lot of current must be spent to amplify the VCO signal to drive the polyphase filters (external VCO at nominal frequency) or to drive the flipflops (external VCO at double frequency).

III. DESIGN EXAMPLE

In today's RF transceiver designs, it requires low-IF or zero-IF. It is important to offer quadrature generation at a minimal power consumption. It pushes the designers use the combination of the very low phase noise specifications with very low power consumption (battery operation), e.g. *L*C-VCOs.

A. Design for Low Power

Consider a general LC-VCO circuit as shown in Fig. 6 (a). The oscillator consists of an inductor L and a capacitor C, building a parallel resonance tank, and an active element $-R$, compensating the losses of the inductor R_L and the losses of the capacitor R_C. For easily calculated, the *L*C-tank resonator can be simplified to Fig. 6 (b). Using the energy conservation theorem, the maximal energy stored in the inductor must equal the maximal energy stored in the capacitor, then

$$\frac{CV_{peak}^2}{2} = \frac{LI_{peak}^2}{2} \qquad (9)$$

$$P_{loss} = RI_{peak}^2 = C\frac{R}{L}V_{peak}^2 \qquad (10)$$

As we know, the angular center frequency in Fig. (a) is $w_c = \frac{1}{\sqrt{RC}}$, then

$$P_{loss} = RC^2 w_c^2 V_{peak}^2 = \frac{R}{L^2 w_c^2} V_{peak}^2 \qquad (11)$$

Since the power consumption of a VCO must compensate at least the losses in the tank, we are able to see from these equations above.

1) The power loss decreases linearly for lower series resistances in the resonance tank and the increasing the inductance decreases the power loss.
2) It clearly shows that power consumption decreases *quadratically*, if the tank inductance can be increased.

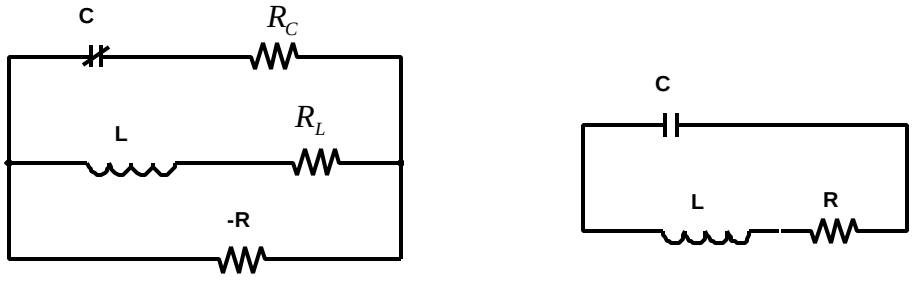

Fig. 6(a) LC-VCO, (b) LC resonator tank

B. Design for Low Phase Noise

Leeson published the following heuristic expression for the phase noise of an *L*C-VCO[10]

$$S_{SSB} = F\frac{kT}{2P_{sig}}\frac{w_c^2}{Q^2\Delta w^2} \tag{12}$$

where is the loaded quality factor of the tank, $\Delta w = 2p\Delta f$ is the angular frequency offset, and is called the device noise excess factor or simply noise factor. One obvious way to reduce phase noise is to increase $P_{sig} \propto V_{peak}^2$ or use a higher Q. With Barkhausen oscillation criterion, the phase stability definition for appears to be the most appropriate for the oscillator application and the phase stability quality factor is defined as

$$Q_{PS} = -\frac{w_c}{2}\frac{df}{dw}\Big|_{w=w_c} \tag{13}$$

simplify this by $f = 0$ at w_c,

$$Q_{PS} = \frac{L}{R}w_c \tag{14}$$

Fig. 7 shows the amplitude and phase plot for an *L*C-tank.

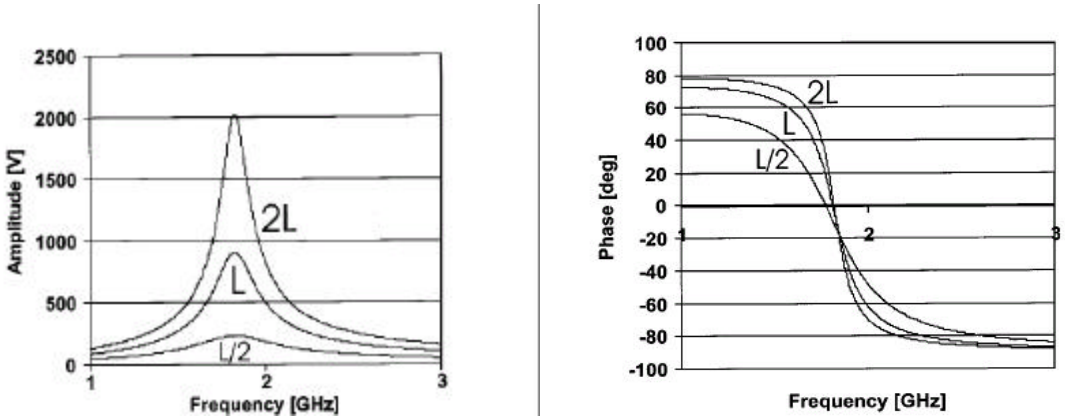

Fig. 7 LC-tank bode plot

Substituting (14) into (12)

$$S_{SSB} = F\frac{kT}{2P_{sig}}\frac{R^2}{L^2\Delta w^2} = F\frac{kT}{V_{peak}^2}\frac{R^3}{L^2\Delta w^2} \tag{15}$$

it turns out that, despite the unavoidable high series resistances in standard CMOS processes, phase noise still can be optimized.

A normalized phase noise has been defined as a figure of merit (FOM) for oscillators:

$$FOM = S_{SSB}\left(\frac{\Delta f}{f_0}\right)^2 P_{VCO} / mW \qquad (16)$$

where P_{VCO} is the total VCO power consumption. Table 1 shows recently published state-of-art in this design by phase-noise performance, power dissipation to generate quadrature signals.

VCO	**Tech.** $[mm]$	**Power** $[mW]$	**Phase noise** $[dB_c / Hz]$	**FOM** $[dB_c / Hz]$
[17]	0.7	6	-130	-177.8
[18]	0.25	24	-132	-174.1
[19]	0.8	66	-132	-171.1
[20]	0.25	32.4	-141	-181.5
[15]	0.25	20	-143	-185.5

Table 1 The State-of-art VCO circuits

IV. CONCLUSION

Quadrature generators are widely used in communication systems, especially in today's RF transceivers. Theoretically, quadrature generation techniques can be derived to three categories, *RC-CR* network, Havens' technique, and Frequency division. In order to improve the phase noise, an alternative architecture is used to produce quadrature outputs as LC-VCOs. It becomes more challenged that the design consideration is aim on

minimize the overall power consumption, size, and cost to improve the phase-noise of the circuits. In reality, designers are always in between the tradeoffs.

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