Low Voltage, Low Power CMOS Bandgap References

ECE 1352 – Reading Assignment
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1.0 Introduction

Many analog circuits require voltage references, such as A/D and D/A converters. A voltage reference must be, inherently, well-defined and insensitive to temperature, power supply and load variations. The resolution of an A/D or D/A converter is limited by the precision of its reference voltage over the circuit's supply voltage and operating temperature ranges. The bandgap voltage reference is required to exhibit both high power supply rejection and low temperature coefficient, and is probably the most popular high performance voltage reference used in integrated circuits today. However, IC design is now predominated by low power, low voltage objectives, making CMOS the technology of choice. Since the bandgap reference is bipolar in nature, solutions are required to create the reference without the use of a costly BiCMOS process. This paper examines bandgap references designed for low-power, low voltage operation.

1.1 Background

By definition a bandgap reference is a voltage reference of which the output voltage is referred to the bandgap energy of the used semiconductor. The first bandgap reference was proposed by Robert Widlar in 1971 [1]. It used conventional junction isolated bipolar technology to make a stable low voltage (1.220 V) reference.

In MOS technologies, early implementation of voltage references were based on the difference between the threshold voltages of enhancement and depletion mode MOS transistors [2]. This provides a low temperature coefficient, but the output is

not easily controlled because of the direct dependence on the doses of the ion implantation steps. Additionally, depletion mode transistors are not typically available in most CMOS processes.

It is well understood that V_{BE} is nearly complementary to absolute temperature (CTAT), that is it decreases linearly with temperature [3]. It is noted that the value of the V_{BE} is equal to the bandgap voltage of the semiconductor, V_{G0}, (in a first order sense) extrapolated to absolute zero. If a voltage that is equal in magnitude to V_{BE}, but proportional to absolute temperature (PTAT), is summed with V_{BE} we obtain a voltage equal to V_{G0}. In this way a well defined voltage reference is created that is independent of temperature.

A PTAT voltage can be obtained through the difference of two V_{BE}s biased at different current densities.

$$\Delta V_{BE} = V_T \ln\left(\frac{J_{C2}}{J_{C1}}\right)$$

A classic bipolar implementation is shown in Figure 1:

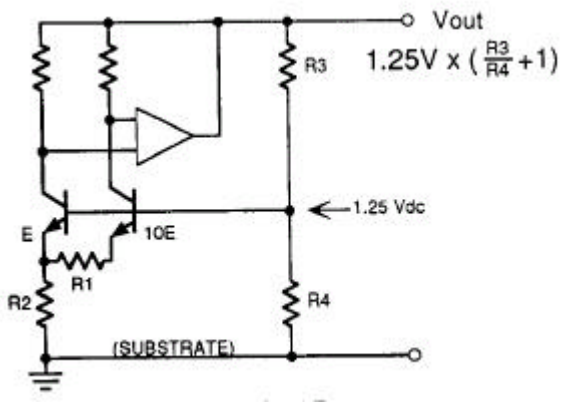

Figure 1: Brokaw (bipolar) bandgap reference circuit [1]

In a conventional CMOS process it is possible to use the parasitic substrate npn or pnp transistors in the case of p-well and n-well process, respectively as shown in Figure 2. These transistors have intrinsic limitations that arise in the development of high performance voltage references. The main drawback is the series base resistance due to large lateral dimensions between the base contact and the effective emitter region [4]. Another major source of error is the offset voltage, leading to a large variation in the output reference voltage and consequently to a very large degradation of its temperature stability [5].

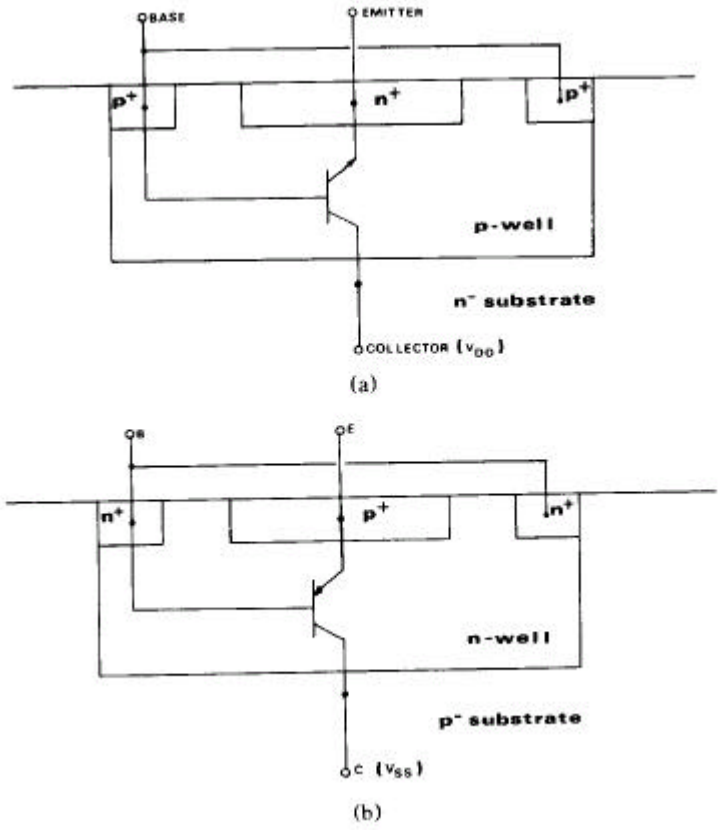

Figure 2: a) vertical npn transistor b) vertical pnp transistor [2]

The typical CMOS bandgap reference circuit is shown in Figure 3. The output reference voltage, V_{ref}, is given by:

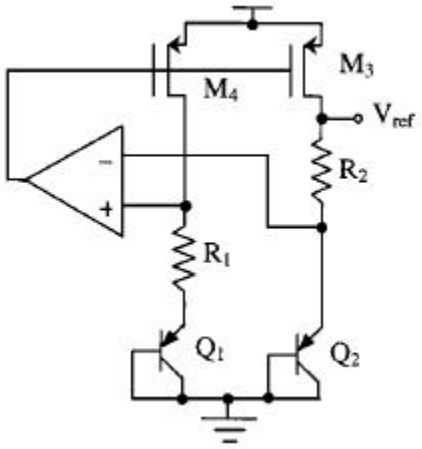

Figure 3: Typical CMOS bandgap reference [6]

$$V_{ref} = V_{EB2} + \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right)$$

where A_1 and A_2 are the emitter areas of Q_1 and Q_2. The first term is the CTAT term and the second the PTAT term. The minimum supply voltage can be expressed as:

$$\min\{V_{DD}\} = V_{ref} + V_{SDsat}$$

The value of V_{ref} is typically 1.25 volts, while V_{SDsat} ranges from 0.1 – 0.3V. Therefore, the theoretical minimum supply voltage is approximately 1.4V.

2.0 Low Voltage, Low Power Designs

As mentioned a main concern in CMOS bandgap references is the offset problem. The large offset reduces the accuracy of the output voltage. Laser trimming is has been utilized as a solution, but its costs are prohibitive. [7] shows that the dominant term of the output voltage is indeed a function of the offset voltage and to achieve improved accuracy, the offset must be reduced. They propose the circuit in Figure 4. Its operation is based on the standard bandgap reference circuit, however it

employs a chopped opamp. Transistors M10, M11, M13, and M15 act as input choppers of the applied voltage difference at IN+ and IN-. The offset from M2 and M3, the input pair, as well as the offset from the current mirror pair, M6 and M7, are cancelled by the second chopper, M19, M20, M21, and M22. Due to the transposition at the third chopper M27, M28, M29, and M30 the offset of the current sources M12 and M13 are also eliminated. Thus M31 provides the bandgap referenced output voltage. Simulations show that the use of chopping techniques reduces the spread of the output voltage to 3.2mV as compared to 32mV without chopping. The total power consumption is measured to be 7.5μW.

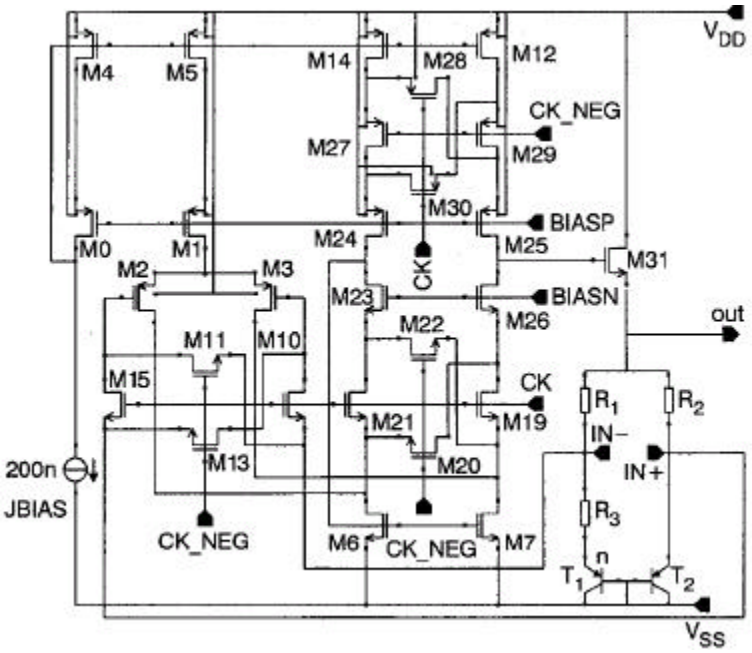

Figure 4: Low voltage BGR proposed by [7]

Standard BGR topology as discussed earlier, has a nonscalable output of approximately 1.25V. The supply voltage of a nearly discharged battery is only about 0.9V. The possibility of a 0.9 BGR is investigated in [8], where they propose two alternative topologies.

The first technique operates by summing two currents with opposite temperature dependence on a resistor. The resistor value controls the reference voltage that is generated. The second technique sums two voltages that are first attenuated. Resistive voltage dividers are used for the determined attenuation factor.

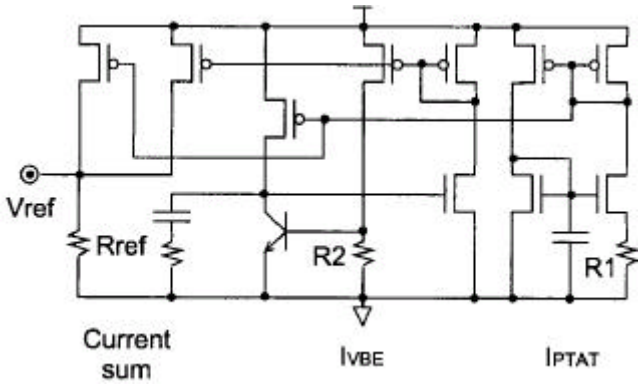

Figure 5: Current summing BGR [8]

The circuit that sums the two currents is found in Figure 5. It is composed of three subcircuits. The first generates the PTAT current; the second mirrors the current to another transistor, which generates the other component. The last subcircuit consists of a resistor whose function is to sum the currents and convert it to the desired voltage reference level. The minimum supply voltage required for correct operation is 0.7, the voltage of the forward biased diode, and the drain to source voltage of the output transistor of the current mirror driving it. The drain to source voltage can be as low as 0.2V. In this way a low voltage BGR can be generated.

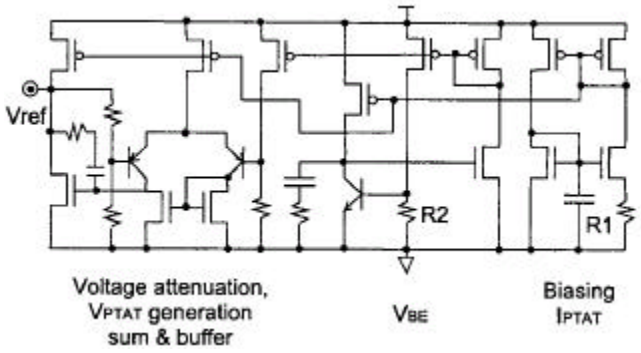

Figure 6: Voltage summing BGR [8]

Figure 6 shows the second circuit, which is also composed of three subcircuits. The only difference between the current summing BGR and the voltage summing BGR is the third subcircuit. The third section is composed of a differential amplifier in a non-inverting feedback loop. The offset voltage from the use of unmatched bipolar transistors generates the PTAT component. The applied diode voltage is not the full base-emitter voltage, as in a standard BGR, but a fraction. The minimum supply voltage of one path is V_T plus a V_{CEsat}, plus the source to drain voltage of the tail current generator. The second path's minimum supply voltage is a V_{BE} plus the minimum voltage of the tail current generator plus the output voltage of the V_{BE} generator. This value is equal to 1V with the the technology that was used in this study.

The experimental results in Figure 7 show the output voltage versus the supply voltage and the temperature dependence of the current summing circuit. The output voltage was found to vary by less the 0.5% over the 0.9V to 2.5V range. In the same range the temperature dependence varied by 2%.

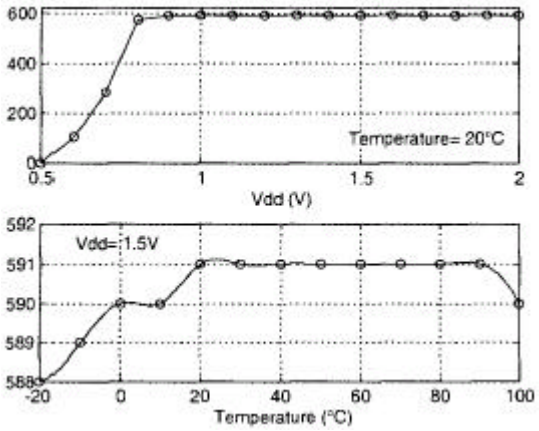

Figure 7: a) V_{ref} vs V_{dd} b) V_{ref} vs Temperature [8]

A third method of low power, low voltage BGR design is through the use of dynamic threshold MOS (DTMOS) devices. As we have seen the bandgap for low power applications can be made to appear smaller through resistive subdivision, but it is at the expense of area. The bandgap can also be made to appear smaller if the junction is in the presence of an electrostatic field. The bandgap is lowered by the electrostatic field. This method can be implemented by replacing the normal diodes with MOS diodes that have interconnected gates and backgates. These devices are DTMOS devices; a cross-section is shown in Figure 8. The use of a P-DTMOS device results in a V_{G0} of 0.6V and the temperature gradient of V_{GS} is approximately –1mV/K. These values are half the typical values of a standard BGR.

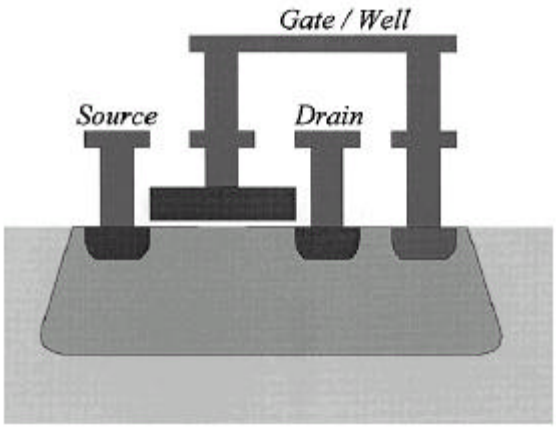

Figure 8: DTMOS cross-section [9]

A DTMOS BGR can be designed using the same topology of a standard CMOS BGR. Figure 9 demonstrates such a circuit. The circuit consists of a folded-cascode opamp and matched resistors with unequal value. The DTMOS diodes are shown with the gate-backgate connection. The input stage also utilizes DTMOS transistors, which allows operation at low supply voltages. The opamps's output stage, shaded, uses a low voltage current mirror. Correct operation of this opamp was verified for supply voltages down to 0.7V. The circuit's temperature dependence is shown in Figure 10. The variation over the range, -20°C to 100°C, is just 4.5mV.

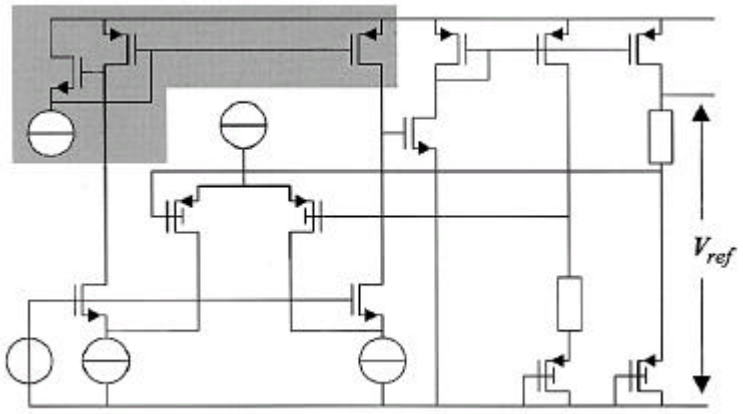

Figure 9: Low Voltage DTMOS BGR [9]

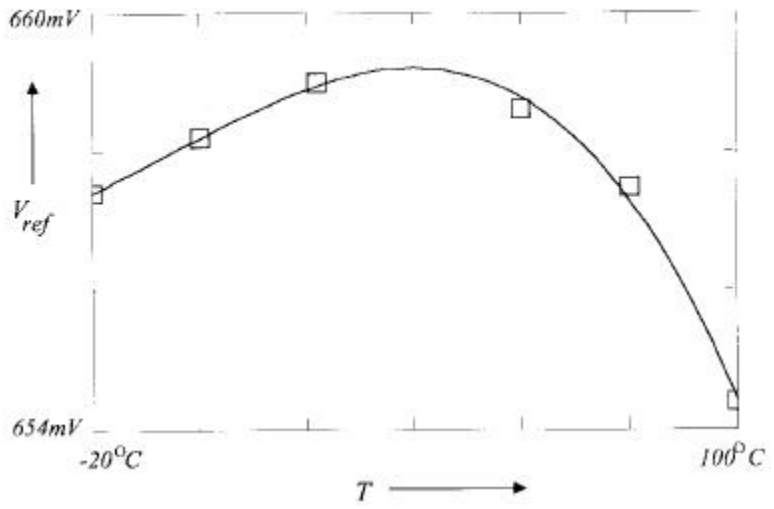

Figure 10: V_{ref} vs. Temperature [9]

Several other low voltage CMOS BGRs are proposed in [10],[11], [6], and [12]. They are all based on a resistive divider network. [10] first proposed the circuit in Figure 11 and it is shown that the reference voltage is defined as:

$$V_{ref} = R4\left(\frac{V_{f1}}{R2} + \frac{dV_f}{R3}\right) \equiv V_{ref\_prop}$$

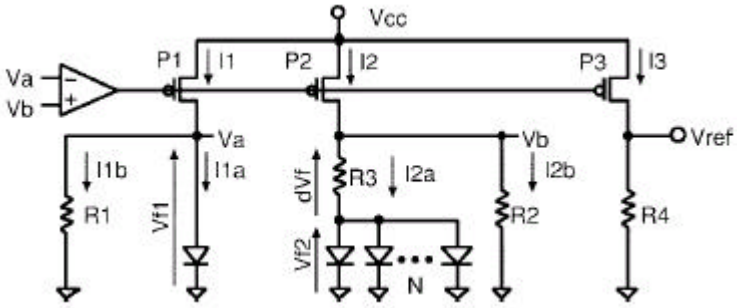

Figure 11: Circuit proposed by [10]

Further, if the resistor and diode parameters for the proposed BGR are the same as a conventional BFR, V_{ref}_prop can be simplified to:

$$V_{ref\_prop} = \frac{R4}{R2} V_{ref\_conv}$$

Experimental results are plotted in Figure 12. V_{ref} is 515mV ± 1mV from 2.2 to 4 V at 27°C; and 515mV ± 3mV from 27 to 125°C. The supply voltage was limited to 2.1V, due to the transistors available in the technology available. However, simulation showed that the minimum supply voltage is approximately 0.84V.

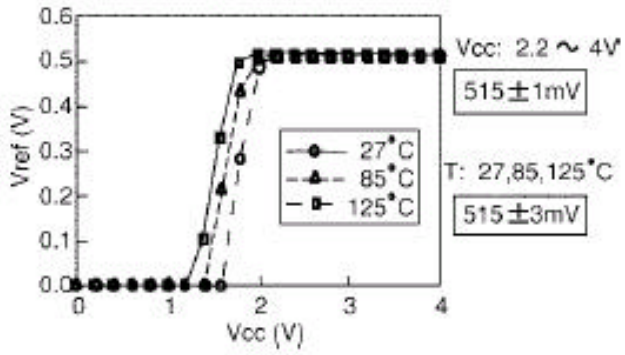

Figure 12: Experimental results from [10]

[11] seeks to improve the design found in [10] through several modifications. The use of cascode devices improves the output impedance of the current sources. By improving the output impedance the sensitivity of V_{ref} to the supply voltage is decreased. Resistors R1 and R2 of Figure 11 are replaced with series equivalents. The addition of nodes V3 and V4 improve the ability of the opamp to operate in sub-1V conditions. The proposed circuit is found in Figure 13. The circuit was simulated through -20°C to 100°C and supply voltages of 0.95V to 1.50V. The curves are found to have a spread of less than 0.24%.

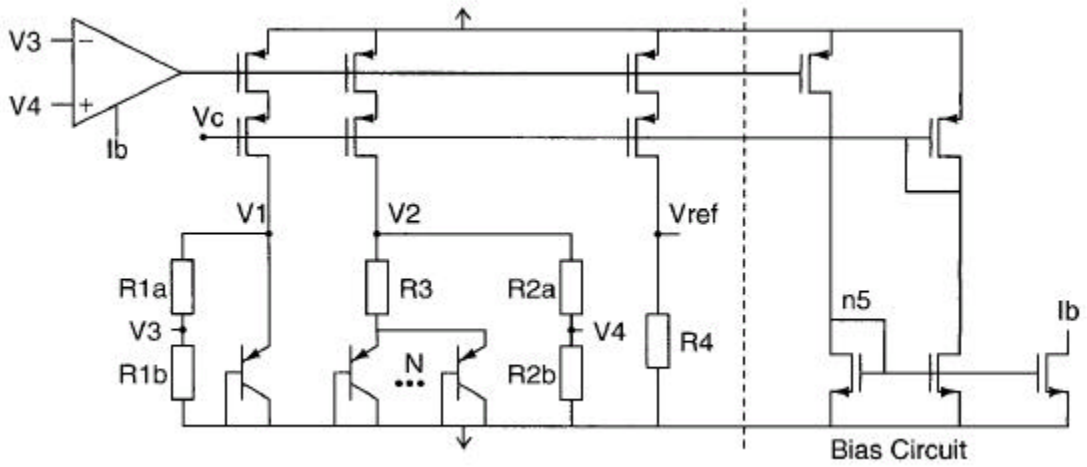

Figure 13: Circuit proposed by [10]

[6] proposes another improvement to [10] with the circuit depicted in Figure 14. Resistors are used in place of the input differential stage of the opamp.

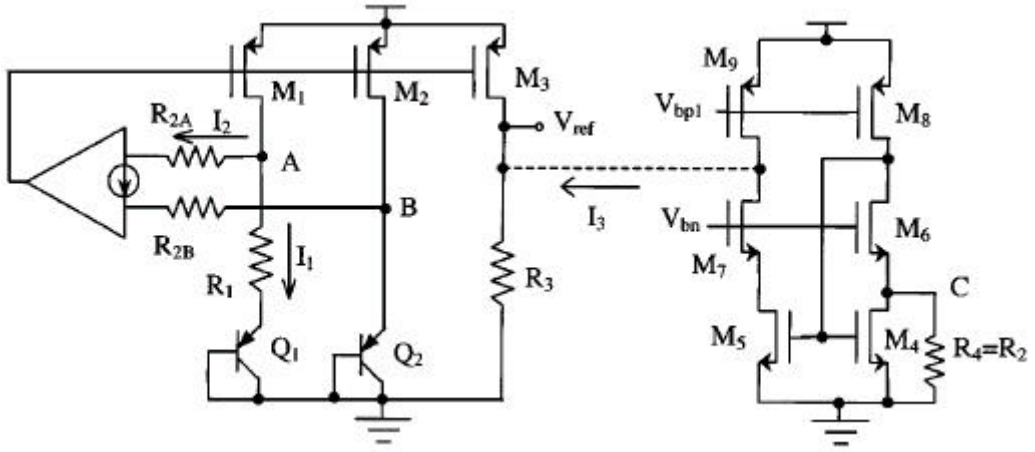

Figure 14: Circuit proposed by [6]

They are used to obtain a PTAT current by sensing the voltage difference and the current is summed with a current complementary to V_{EB} to obtain the reference voltage. This technique is based on the use of a transimpedance amplifier. The reference voltage for this circuit is given by:

$$V_{ref} = R_3 \cdot \left[\frac{1}{R_1} \cdot V_T \ln\left(\frac{A_1}{A_2}\right) + \frac{V_{EB2}}{R_2} - \frac{Vb}{R_2} \right]$$

Again, similar to [10] the value of V_{ref} can be changed by choosing different values of R_1, R_2, and R_3. Experimental results for a V_{ref} of 1V were shown to be accurate within ±1% over 0°C to 100°C, untrimmed and ±0.3% with R_1 trimmed.

[12] also suggests improvements to the circuit in [10]. The motivation for the improvements is that the differential amplifier in [10] has MOS depletion transistors in the input stage. These devices are not used in standard processes and result in higher process and characterization costs. PMOS transistors in weak inversion are proposed in place of the depletion mode transistors of [10]. The new circuit is shown in Figure 15. As the supply voltage is decreased below 1.4V the input devices enter weak inversion. The BGR remains biased correctly as long as the supply is at least 0.9V, below which the loop gain is insufficient. A second circuit (Figure 16) proposed uses an NMOS topology with PMOS level shifters to provide the correct common mode voltage to the input stage. The circuit is unable to operate with a supply voltage as low as the first, but it does not require a startup circuit for correct biasing at power-on. The supply voltage is limited to approximately 1.4V.

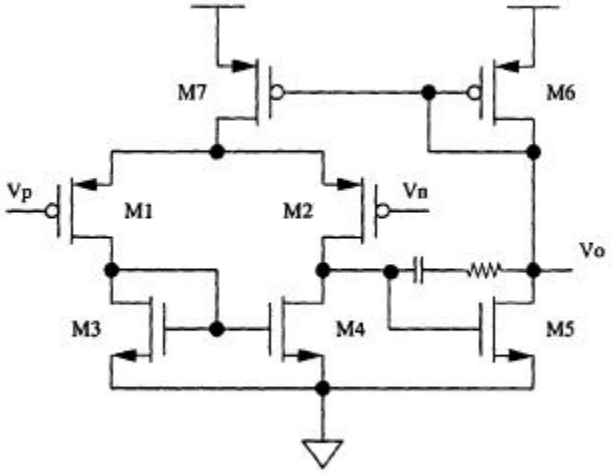

Figure 15: Weak inversion PMOS opamp proposed in [12]

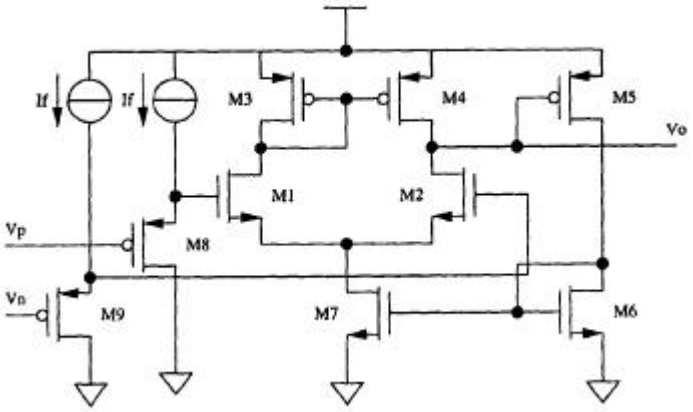

Figure 16: NMOS opamp with level shifters [12]

3.0 Future Issues

Low power, low voltage design remains a concern as device technology continues to scale downward. Supply voltages decrease as feature sizes shrink. Thus, the downward pressure will continue to present challenges to low voltage (sub-1 volt) bandgap reference design.

A bandgap reference itself is not a signal processing circuit, but the noise at its output can be very disadvantageous for signal processing circuit that, for example, refer their bias quantities to the bandgap reference voltage. Noise performance is critical in many designs, therefore, low noise BGRs are increasingly important for low power, low voltage designs.

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