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Nov 15, 2002

ECE 1352F

Phase Noise of VCOs

0. ABSTRACT

The main purpose of this paper is to present simplified first order noise analysis techniques as applied to ring VCOs. The scarcity of literature on the topic as well as industry trends made me decide to focus solely on the ring oscillator topology. Most of the published work in this area has been done by B.Razavi. A.Hajimiri has done quite a lot in the theoretically more advanced and general VCO noise analysis.

The paper begins by a brief motivation for low phase noise VCOs, and a few short comments on three VCO classes.

Presented next are simplified linear, first-order phase noise and jitter analyses that nevertheless provide significant insight into the governing noise mechanisms with very reasonable accuracy. Certain low noise VCO design and simulation issues are looked at next. The following section provides a brief look at the underlying time-variant oscillator theory and cyclostationary statistics needed for a more rigorous phase noise treatment of a general VCO. Further insight is offered into VCO design, including the ring oscillator topology.

Lastly, conclusions are provided.

1. Need for Low Phase Noise VCOs

Phase noise results in spectral impurity of the VCO output frequency. This is manifested as unwanted jitter impacting the timing accuracy in applications where precise phase alignment is required. In cases where frequency translation is performed, the SNR is affected by the introduction of energy at unwanted phase noise frequencies close to the carrier.

High-speed digital circuits like microprocessors and memories utilize phase locking at the board-chip interface to align the on-chip clock to the system clock. Usually fabricated on the same substrate and typically operating from global supply and ground busses, a PLL will suffer from substrate and supply noise. This noise is seen in form of jitter as already mentioned, primarily through various mechanisms in the VCO. The fact that a myriad of high-speed digital, analog and RF circuits utilize PLLs for frequency synthesis, clock recovery, skew suppression and communication channel jitter reduction demonstrates the need for low phase noise VCOs.

2. Comparison of Oscillator Types

A. Harmonic Oscillator

A harmonic oscillator is equivalent to two energy storage elements, operating in resonance, producing a periodic output signal. The resonant element can be an LC-tank or a quartz crystal. Resonant circuit-based VCOs are known to have excellent jitter performance. Analysis of noise in resonant-based VCOs is well developed in literature, and design techniques for realizing low jitter performance are well understood. An example LC-oscillator is shown in Fig. 0. There are a few

disadvantages for monolithic implementation of this circuit; 1) both the control and the output signals are single-ended making the circuit sensitive to supply/substrate noise; 2) the required inductor and varactor Q is usually greater than 20 → off-chip components are needed. Another possibility is the use of integrated inductors that are generally large and exhibit low Q factors due to resistive losses. Advances in processing certainly allow the use of integrated inductors for certain, but not all applications.

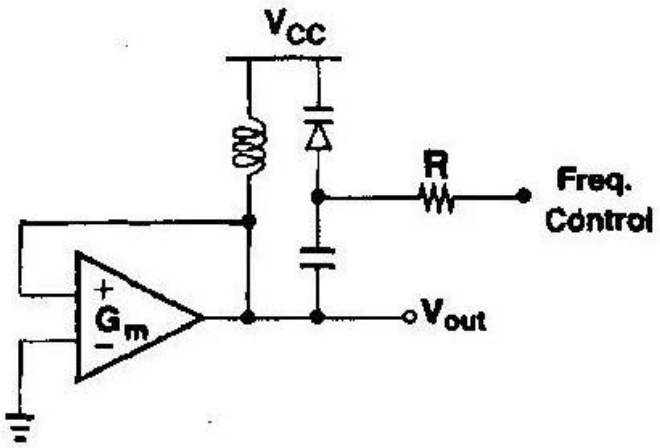


Fig. 0

B. Relaxation Oscillator

A relaxation oscillator is equivalent to one energy storage element, with additional circuitry that senses the element state and controls its excitation to produce a periodic output signal. The jitter performance of this type of oscillator is worse than that of the harmonic oscillator, but the circuit is suitable for monolithic integration.

C. Ring Oscillator

The trend toward large-scale integration and low cost makes monolithic oscillators very desirable. Due to their speed and ease of integration, ring oscillators are

increasingly being used as voltage controlled oscillators. Some examples where they find use are in clock recovery phase-locked loops for serial data communication, disk drive clock recovery, clock frequency multiplication, oversampling analog-to-digital converters… However, it was only in the mid-nineties that more rigorous phase noise analyses appeared along with experimental verifications of their predictions.

3. Noise Shaping in a Linear Oscillatory System

When a circuit begins to oscillate, the amplitude grows until it is limited by some nonlinear mechanism. In typical configurations, the open-loop gain of the circuit drops as signal swings become large thus preventing further growth of amplitude.

Presented next is the derivation of the noise shaping function assuming the oscillator is a linear feedback system as shown in Fig 1.

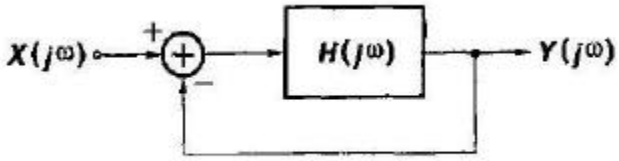


Fig. 1

The transfer function for the system in fig. 1 is presented as:

$$\frac{Y}{X}(jw) = \frac{H(jw)}{H(jw)+1} \qquad (1)$$

The denominator of (1) goes to infinity for a circuit oscillating at w_0 if $H(jw_0) = -1$. For frequencies close to the carrier frequency, i.e., $w = w_0 + \Delta w$, the open loop transfer function can be approximated as $H = H_0 + \Delta H$ assuming Δw is small.

$$\therefore\ H(jw) = H(jw_0) + \Delta w \frac{dH}{dw} \quad \Rightarrow$$

$$\frac{Y}{X}\left[j(w_0 + \Delta w)\right] \approx \frac{-1}{\Delta w \dfrac{dH}{dw}} \quad , \qquad \text{assuming } \left|\Delta w \frac{dH}{dw}\right| << 1 \qquad (2)$$

which is true for most practical cases.

From (2), we conclude that the noise power spectral density is shaped by

$$\left|\frac{Y}{X}\left[j(w_0 + \Delta w)\right]\right|^2 = \frac{1}{(\Delta w)^2 \left|\dfrac{dH}{dw}\right|^2} \qquad (3)$$

This is shown in Fig. 2

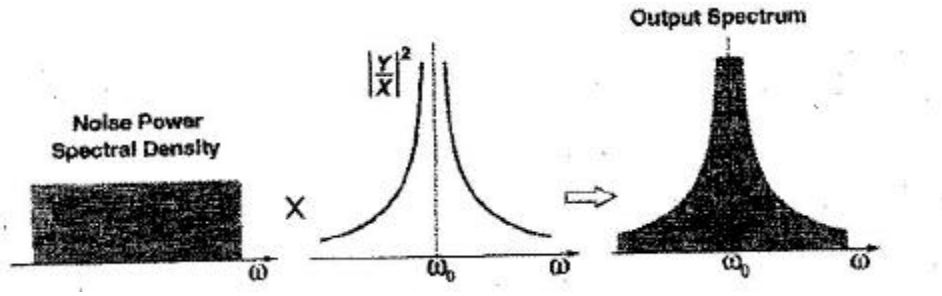
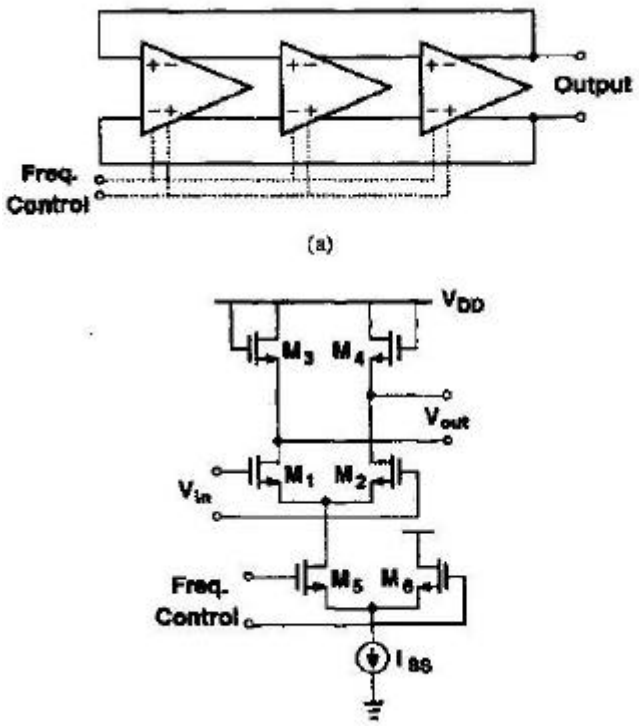


Fig 2.

As already mentioned above, the noise shaping function was derived using a linear-time-invariant model of the oscillator that is an inherently time-variant, linear system, if amplitude limiting is ignored, [10]. The validity of this approach is discussed in [1]. The key point to bear in mind is that (3) is a simple model that yields reasonable accuracy. One model will not be appropriate for any oscillator type, therefore the designer needs to understand when this model is applicable and when it is not. Its accuracy must ultimately be checked through simulations.

4. CMOS Ring Oscillator – Phase Noise Approach

A fully differential three-stage ring oscillator is shown in Fig 3a. Both the control and the output signals are fully differential to achieve high common-mode rejection.



(b) possible implementation of one ring oscillator stage

Fig 3.

Fig 4. depicts a linearized VCO model that can be used for first-order phase noise analysis.

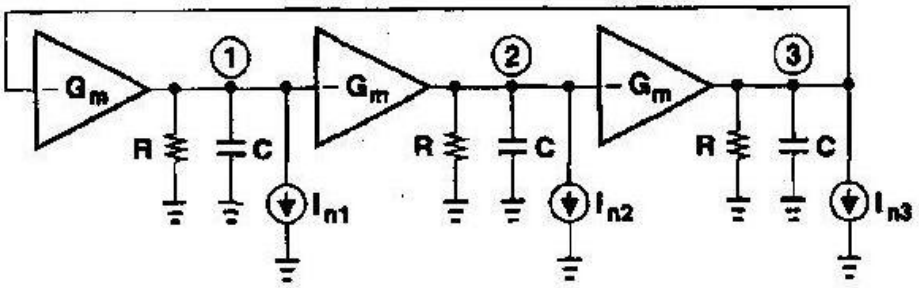


Fig 4.

The model consists of the stage output resistance R, load capacitance C, equivalent stage transconductance Gm and input-referred current noise sources injected into all nodes. The noise sources incorporate both thermal and shot noise.

Since each stage is represented as a first-order linear system, its transfer function can be expressed as $H_{1,2,3}(jw) = \dfrac{-Gm \cdot R}{1 + j\dfrac{w}{w_0}}$ where $Gm \cdot R$ is the dc stage gain and w_0 the oscillation frequency. Recalling that to sustain steady oscillations, total loop-gain equal to unity and total phase shift around the loop of 360^0 at w_0 are necessary. This implies that each stage contributes 120^0 of phase shift resulting in $w_0 = \dfrac{\sqrt{3}}{RC}$. The stage transfer function now becomes, $H_{1,2,3}(jw) = \dfrac{-Gm \cdot R}{1 + j\sqrt{3}\dfrac{w}{w_0}}$. Since $\left|H(jw_0)\right| = 1$ is the second oscillation condition, it implies that $Gm \cdot R = 2$. Finally, the total open-loop transfer function of the three-stage ring oscillator can be written as $H(jw) = \dfrac{-8}{\left(1 + j\sqrt{3}\dfrac{w}{w_0}\right)^3}$.

It follows from (3), that if a noise current I_{n1} is injected into node 1, its power spectrum is shaped by:

$$\left|\frac{V_1}{I_{n1}}[j(w_0 + \Delta w)]\right|^2 = \frac{R^2}{27}\left(\frac{w_0}{\Delta w}\right)^2 \qquad (4)$$

This equation is key to predicting various phase noise components in the ring oscillator.

4.1 Linearized Model Issues

The model presented in Fig 4. was an oversimplification of the oscillator. Oscillator stages turn on and off during the oscillation period suggesting that Gm, R and C parameters are not constant as assumed in the derivation of (4). Secondly, the linear model doesn't predict mixing effects resulting from nonlinearities, and thirdly it doesn't account for cyclostationary device noise behavior. The cyclostationary behavior, i.e., periodically time varying statistics (mean, autocorrelation…) result from the fact that the circuit bias conditions are a function of time.

4.2 Additive Noise

The additive noise is the noise due to sources I_{n1-3} that can directly be added at the output. Assuming equivalent noise sources and a noise frequency close to w_0 such that the stage gain $\approx$ unity, the total contribution of I_{n1-3} at the output is

$$\left|V_{ntot}\left[j(w_0+\Delta w)\right]\right|^2 = \frac{R^2}{9}\left(\frac{w_0}{\Delta w}\right)^2 \overline{I_n^{\,2}} \qquad (5),$$

where $\overline{I_n^2}$ represents both thermal and shot noise. The profile of (5) suggests that additive noise is significant only at frequencies close to w_0.

4.3 High-Frequency Multiplicative Noise

Circuit nonlinearity when successive stages turn off during oscillations causes noise components to be multiplied by the oscillator signal. The output signal can always be modeled by higher order polynomial terms such as

$$Vout = a_1 \cdot Vin + a_2 \cdot Vin^2 + a_3 \cdot Vin^3 + \ldots + a_n \cdot Vin^n$$

The input signal in presence of noise can be written as $Vin(t) = A_0 \cos w_0 t + A_n \cos w_n t$. Substituting Vin(t) into the expression for Vout, we see that frequency mixing occurs. In case of a fully differential configuration, $a_2 = 0$, so that only the Vin^3 term is significant yielding $Vout_3 a \;\; a_3 A_0^2 A_n \cos(2w_0 - w_n)t$. The high-frequency multiplicative noise effect is most significant for w_n close to w_0. This is illustrated in Fig 5.

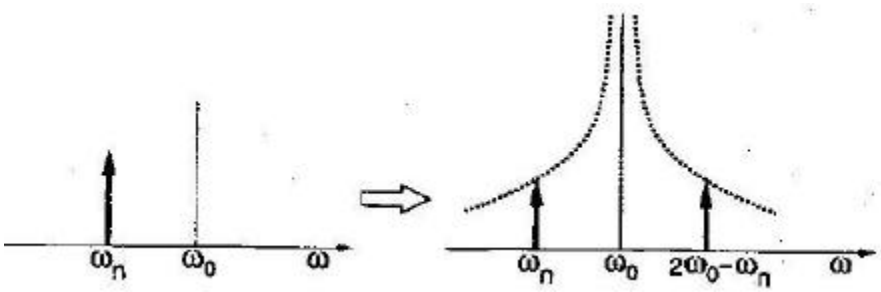


Fig 5.

4.4 Low-Frequency Multiplicative Noise

In stage implementation of Fig 3b. the ring oscillator frequency of oscillation is a function of the tail current. Any noise in the current source will manifest itself at the output as frequency modulation. In this case, low frequency $1/f$ noise is of most concern.

Assuming that the output voltage takes the shape of an FM modulated signal, stemming from a sinusoidally modulated oscillator free running frequency and classically expressed by $Vout(t) = A_0 \cos\left(w_0 t + \frac{Kvco}{w_m} I_m \sin w_m t \right)$, where w_m is the frequency of the modulating noise signal, then using a small angle approximation ,i.e., $Kvco \cdot I_m / w_m << 1$,

$$Vout \approx A_0 \cos w_0 t + \frac{A_0 I_m Kvco}{2w_m}\left[\cos(w_0 + w_m)t - \cos(w_0 - w_m)t\right], \qquad (6)$$

(6) represents frequency convolution and is depicted in Fig 6.

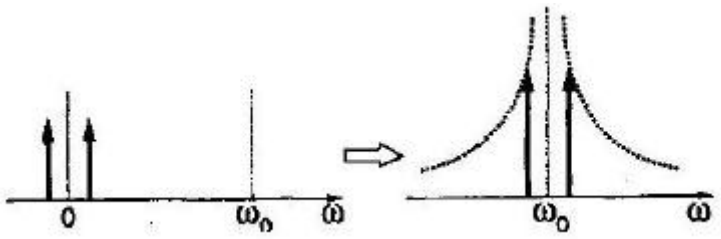


Fig 6.

From Fig. 6 it becomes obvious that $1/f$ noise contribution at low frequencies becomes extremely significant for two reasons. First, the amplitude of the two delta functions at $\pm w_m$ will be higher (due to the $1/f$ noise profile). Second, the smaller the spacing $w_0 \pm w_m$, the higher the amplitude of the noise shaping function will be. These two effects are multiplicative thus accentuating the low-frequency noise at the output.

5. CMOS Ring Oscillator – Timing Jitter Approach

In this section two additional oscillator noise sources will be presented, namely the supply and substrate noise whose effects are traditionally expressed and analyzed in the time domain in terms of signal edge uncertainty – timing jitter.

One of the commonly used figures of merit for oscillators is the cycle-to-cycle jitter illustrated in Fig 7.

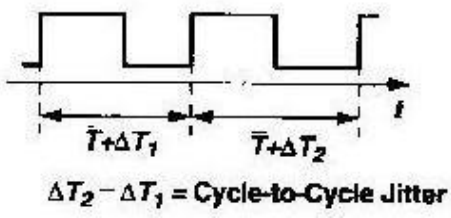


Fig 7.

The rms value of this timing error is given as $\Delta T_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}(T_{n+1} - T_n)^2}$ and represents the rms difference between two consecutive periods.

5.1 Phase Noise/Jitter Relation

Phase noise and jitter are frequency domain and time domain quantities representing the oscillator frequency uncertainty. As demonstrated in [2], the two quantities can be related by $\Delta T_{cc}{}^2 \approx \frac{4p}{w_0{}^3} S_f(w)(w - w_0)^2$ where $\Delta T_{cc}{}^2$ represents the cycle-to-cycle jitter variance and S_f is the noise shaping power spectral density function.

5.2 Jitter due to Supply/Substrate Noise

There are two major effects that convert the supply and substrate noise to jitter. Depicted in Fig 8. are the nonlinear MOS drain capacitances Cdb, whose capacitance is a function of Vdd and Vsub. The second effect is the finite common-mode rejection of the stage inverter.

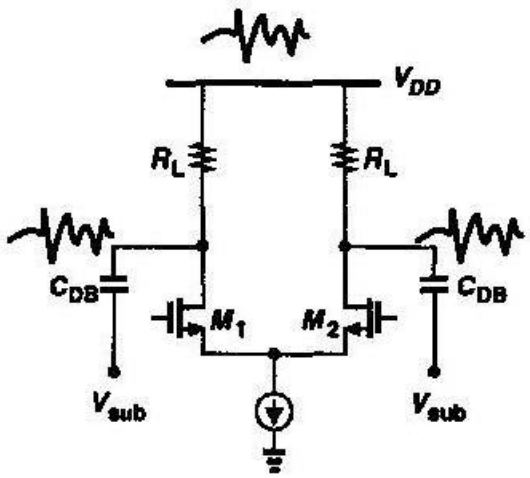


Fig 8.

As the drain junction capacitances vary with noise on supply/substrate, they modulate the frequency of the ring oscillator. An oscillator under the influence of such environmental noise can be thought of as a VCO having different control voltages. The variation of oscillation frequency with a control voltage can be described by a sensitivity function Kvco as follows: assuming the modulating control voltage is a small sinusoidal disturbance of the form $\Delta V_m(t) = V_m \cos w_m t$ and recalling that the VCO frequency is ideally given by $f_{out} = f_0 + K_{vco} \cdot V_{cont}$, it follows that the frequency change generated is $\Delta f_o(t) = V_m K_{vco} \cos w_m t$. The change in frequency as a function of time can be converted into an equivalent change in period as a function of time that can be further used to determine the autocorrelation function. In [2], using the cycle-to-cycle jitter variance defined in terms of its autocorrelation function, it is shown that the cycle-to-cycle jitter is given by $\Delta T_{cc} = \frac{V_m K_{vco}}{f_0^2}\sqrt{1-\cos(w_m / f_0)}$ → for $f_m << f_0$ we have

$$\Delta T_{cc} \approx \frac{V_m K_{vco} w_m}{\sqrt{2} f_0^3} \qquad (7)$$

From (7) it is evident that the jitter equation is a function of noise amplitude, noise frequency, oscillator frequency and the sensitivity function K_{vco}. The sensitivity can be extracted from simulations by sweeping the supply and substrate voltages and observing the influence on output frequency. It is further reported in [2], that the single-ended ring oscillator has a much higher sensitivity to supply/substrate noise than the differential design which is an expected result. Coupled with the fact that differential designs have much better common-mode rejection, a fully differential ring oscillator, such as that of

Fig 3. is preferred. It is also interesting to note that jitter is directly proportional to supply/substrate noise amplitude (within a few hundred mV) and frequency.

5.3 Low Jitter Oscillator Design

5.3.1 Input Transistor Gate Width

A slightly different approach was taken in [3], where the cycle-to-cycle jitter was shown to be inversely proportional to the tail current and the overdrive voltage. It follows that for low jitter designs, the overdrive voltage should be as large as possible within the allowable limits of course. This can be achieved by a large tail current and low aspect ratio. In [2], the gate width effect on jitter was formulated differently. There, the input transistors' widths were varied while an independent load capacitance was adjusted so that the oscillation frequency was kept constant at all times. This resulted in an optimal input transistor width, w_{opt}, at which the corresponding jitter was minimum. For values greater than w_{opt} the jitter increases.

The method used in [2] is interesting because it compares various transistor width effects at the same oscillation frequency, thus setting a common reference point for the comparison. It can further be analyzed as follows: for the sake of argument we can represent the internal node capacitance as $C_i = C_{out(i)} + C_{in(i+1)} + C_{load}$ where $C_{out(i)} \approx C_{db} + C_{gd}$, and $C_{in(i+1)} \approx C_{gs} + C_{gd}$, and C_{load} is the adjustable capacitor to keep the oscillation frequency constant. Now, assuming that the transistor width is scaled by k, then both the $C_{in(i+1)}$ and $C_{out(i)}$ will roughly scale by k since $Cgs \approx WLCox$ (not exactly equal due to fringing effects) and $C_{db} \approx WLdiffusionCj + 2 \cdot WCjsw$ (assuming

$W >> Ldiffusion$). This means that the input and output capacitance sum at the internal node will increase by $(k-1)(C_{in(i+1)} + C_{out(i)})$. In order to keep the oscillation frequency the same, C_{load} needs to be decreased by $(k-1)(C_{in(i+1)} + C_{out(i)})$. Therefore the sum $C_{out(i)} + C_{in(i+1)} + C_{load}$ is always constant. If we now define the node capacitance sensitivity ratio $l = \frac{nonlinear\_cap}{linear\_cap} \approx \frac{C_{db}}{C_{tot}}$ we see that as the width is increased by k, the ratio l is increased by k as well. Since the nonlinear capacitor contribution grows as the width is increased, the output frequency is modulated more strongly due to supply/substrate noise and we expect to see larger resulting jitter which is exactly what is reported in [2]. This result also matches what has been reported in [3], except that it points to an optimal width rather than 'as low as possible' width.

5.3.2 Power Consumption

Using the result from [3], the jitter can be minimized by increasing the tail current Iss, thus increasing the power consumption. This result was to be expected. It can further be illustrated as follows: if we assume that N identical oscillator outputs are added in phase and that they exhibit only the device electronic noise, then the signal power will be increased by N^2 and the noise power will be increased by N since all the noise sources are uncorrelated (resulting noise voltage a $\sqrt{N}$). This thought-experiment shows that if power is increased by N, the power-to-noise ratio is increased by N. On the other hand if we consider the same scenario with supply/substrate noise we note that signal power will increase by N^2, but so will the noise power since the same supply/substrate noise affects each oscillator → noise is correlated. The important

conclusion is that that supply/substrate noise effect on jitter is relatively independent of the power consumption. Therefore, the supply/substrate induced jitter must be eliminated by circuits with improved positive/negative power-supply rejection. This can be accomplished by using fully differential stages and by using cascode current sources if there is enough voltage swing available. Also, the supply/substrate jitter can be decreased by careful layout techniques such as guard rings, low resistance/inductance supply lines…

5.3.3 Effect of the Number of Stages

In applications where the required oscillation frequency is considerably lower than the technology maximum speed, a ring oscillator with more than three stages can be used. If the oscillation frequency is determined by both the parasitic and load capacitances, as described in section 5.3.1, the three-stage design is better. If an n-stage design is designed to oscillate at f_0, the 3-stage design would want to oscillate at $\frac{N}{3} f_0$ if all other conditions are the same. In order to reduce the 3-stage design frequency to that of the n-stage design, we can accomplish that by increasing the load capacitance. In doing so, we decrease the effect of the parasitic nonlinear capacitor at the internal nodes, thus making these nodes less susceptible to supply/substrate voltage variations which results in lower jitter.

6. Simulation

The time-varying nature of oscillators prohibits the use of standard small-signal ac analyses used in SPICE. For this reason, simulations must be performed in the time domain. It is further recommended in [1] to use sinusoidal noise sources as for example square wave noise source may result in an incorrect spectrum exhibiting coherent sidebands due to errors in interpolation. To simulate the phase noise effects, noise sources at a frequency offset w_n are injected at various circuit nodes and the spectrum is constructed for each case. The linear superposition of all resulting spectra yields the final total output spectrum.

Finally in [1], a first order method is presented that roughly accounts for the cyclostationary noise behavior, by replacing the sinusoidal noise current source by a nonlinear voltage-controlled noise current source. The reported difference between the two scenarios was 0.5dB.

7. Time-Variant Oscillator Approach

In [10], a more advanced oscillator model is introduced. It starts by noting that in an oscillator, each noise perturbation affects both the amplitude and the phase of the output signal. Being time-variant, this effect depends on the time at which the impulse is applied. Therefore a model is used where the input is a current or voltage impulse and the corresponding output is the excess phase generated. For example, in a parallel LC tank, a current impulse at the input only affects the voltage across the capacitor with no effect on the current through the inductor. This results in an instantaneous change in the tank voltage and hence a shift in the amplitude and phase depending on the time of

injection. For a linear capacitor, the instantaneous voltage change ΔV is equal to $\Delta q/C$, where Δq is the total charge injected by the current impulse. As already mentioned the change in amplitude and phase due to the input impulse is time-variant. If the impulse is applied at the peak voltage across the capacitor, it will result in an instantaneous amplitude change, but there will be no phase shift. On the other hand, if the impulse is applied at a zero crossing, it has a maximum effect on the excess phase, $f(t)$, but a minimum effect on the amplitude, $A(t)$. The current impulse at $t = t$ generates a step change in phase. For a small injected charge, the phase shift is proportional to the injected charge → $\Delta f = \Gamma(w_0 t)\frac{\Delta V}{V_{\max}} = \Gamma(w_0 t)\frac{\Delta q}{q_{\max}}$ where $V_{\max}, q_{\max}$ are the maximum voltage swing and its corresponding charge. The function $\Gamma(x)$, is the time-varying, frequency and amplitude independent proportionality factor, called the impulse sensitivity function, ISF. It determines the sensitivity of the oscillator to an impulse input by describing the amount of excess phase shift generated at any point in time. Various oscillators therefore exhibit different ISFs. The important point to note is that the current-phase transfer function is linear for small injected charge, even though the active elements may be strongly nonlinear. Device nonlinearity does however directly affect the shape of the ISF which results in different influences on phase noise. Therefore, for a small charge injected, the equivalent system phase responses can fully be characterized using their linear time-variant phase unit impulse responses:

$$h_f(t,t) = \frac{\Gamma(w_0 t)}{q_{\max}} u(t-t).$$

The phase response, $f(t)$, can be found by convolving the impulse-phase response with the current/voltage input disturbance, i.e.,

$$f(t) = \int_{-\infty}^{\infty} h_f(t,t) \cdot i(t) dt = \int_{-\infty}^{t} \frac{\Gamma(w_o t)}{q_{\max}} i(t) dt \ , \qquad (8)$$

It is shown in [10], that since the ISF is periodic, it can be expanded into Fourier series by

$$\Gamma(w_0 t) = \sum_{n=0}^{\infty} c_n \cos(n w_0 t + \Theta_n)$$

By exchanging the order of integration and summation, it can be shown that individual contributions to the total excess phase, for an arbitrary current input, can be identified in terms of various Fourier coefficients of the ISF. The result is that perturbations in the vicinity of integer multiples of the carrier frequency most significantly affect the total excess phase, $f(t)$. The above theory predicts that flicker noise, weighted by the coefficient c_0 produces a $1/f^3$ phase noise region and the weighted white noise terms give rise to a $1/f^2$ phase noise region. The result of this more involved analysis is that extra phase noise regions exist and that their contribution at low frequencies is much higher than that of flicker noise alone, which is important in oscillator low-frequency multiplicative noise resulting from the current source modulation. The ISF is most conveniently found through simulations.

An added complication in analyzing general VCOs is the fact that some of the random noise sources change periodically in time, i.e., they are cyclostationary. For example the channel noise of a MOS device operating in an oscillator is cyclostationary because periodically time-varying gate-source voltages modulate the drain noise power. A

cyclostationary current $i_n(t)$ can be expressed as $i_n(t) = i_{n0}(t) \cdot a(w_0 t)$, where $i_{n0}(t)$ is a white stationary process and $a(w_0 t)$ is a deterministic periodic function describing the noise amplitude modulation and is referred to as the noise modulating function, NMF.

7.1 Ring Oscillator from a Time-Variant Perspective

The ring oscillator Q is very poor since the energy stored in the node capacitances is reset every cycle. The energy restoration to the resonator occurs during the edges which are the worst possible times. These factors account for, as stated in [10], terrible-noise performance. As a consequence, ring oscillators are found only in the most non-critical applications, such as wide-band phase-locked loops whose dynamics clean up the spectrum.

From the ISF analysis of the excess phase, assuming correlated noise sources, it follows that the ISF is zero except at dc and multiples of the oscillation frequency. Every effort should therefore be made to maximize the correlations of supply/substrate noise. This can be achieved by proper layout techniques, by making the delay stages as similar as possible.

Another interesting result of the ISF analysis regards the choice of the single-ended versus differential oscillator design. It is found that the phase noise of the single-ended design is independent of the number of stages, whereas that of the differential design is not. For a given power consumption, the single-ended design outperforms the differential design since its power dissipation occurs on a per transition basis, whereas that of its differential counterpart is independent of the number of transitions. In reality,

the differential topology is still preferred due to its lower sensitivity to the supply/substrate noise and lower noise injection into other circuits on the same chip.

Since jitter is independent of the number of delay stages in a single-ended design, a larger number of stages will reduce jitter for a given oscillation frequency and power consumption, especially if good symmetry is not achieved and the process has a large flicker noise. For differential designs, where jitter increases with the number of stages, optimal jitter performance will be achieved with a three or four stage design. This is in agreement with conclusions drawn in [2].

8. Conclusions

There are a few contradictions between references used in this paper. For instance, in [2] it is claimed that supply/substrate noise is a much greater contributor of jitter in ring oscillators, whereas [3] has focused on device electronic noise, providing the argument that supply/substrate noise can be minimized by careful design and layout. I would tend to agree more with results presented in [2], due to the fact that designs are becoming more integrated, more complex with voltages scaled down and frequencies scaled up, I would expect supply/substrate to be quite noisy, if not noisier. Also, device transconductances are decreasing with new technologies, thus decreasing thermal noise, further accentuating the effect of supply/substrate noise.

Another contradiction found was between [10] which claims that ring oscillators have very poor phase noise characteristics and are thus used in non-critical applications, whereas in [6], their potential is rated as excellent. Given that the work presented in [10] is much more rigorous and more recent it is probably more valid.

Lastly, a refutation of high-frequency multiplicative noise described in [1] was presented in [10].

Despite the apparent shortcomings, the linearized approaches [1]-[6] have all shown good agreement between predicted, simulated and experimental results. In [1], for instance, less than 0.2dB discrepancy was obtained between the linearized model and simulations for two three-stage VCO topologies (ring-oscillator and relaxation oscillator). Excellent predicted versus simulated jitter characteristics have been reported in [2]-[3] using linear models. The key point to remember is that the linearized model is not a panacea. It provides good agreement for ring oscillators of the topology as shown in Fig 3. and perhaps certain relaxation oscillators. Even within the realm of ring oscillators, if the delay stage circuit is significantly changed one must make sure that the model is still applicable. Also, as the number of stages increases, the model of section 4. loses accuracy. It was reported in [1], that the discrepancy between the predicted and simulated results grew from 0.2dB to 1dB for a four stage design and to 6dB for an eight stage design. Therefore, it is up to the designer to understand the design and carry out the necessary verifications. Nevertheless, the linearized method is still very attractive due to its simplicity. It can be used as an excellent analysis starting point, almost for back-of-the-envelope calculations. Simulations ultimately show whether it is adequate or more advanced techniques, namely ISF and cyclostationary statistics need to be evoked. For an LC-tank VCO, time-variant methods must be used, as one simply cannot get away with the linearized models.

9. References

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