ECE 1352F

RF IMAGE-REJECT RECEIVERS

Submitted to

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by

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November 15, 2002

TABLE OF CONTENTS

1.0 INTRODUCTION

The recent growth of wireless applications has resulted in an increase in demand for low-power, low-cost wireless receivers. As a result, much work has gone into developing highly integrated receivers in CMOS that minimize the number of off-chip components. A major obstacle in achieving this is the inherent image problem present in heterodyne architectures.

To understand the origin of the image, consider the analog mixer shown in figure 1. Its function is to convert the incoming signal from radio frequency (RF) to a lower intermediate frequency (IF) to relax the requirements of the subsequent channel-select filter. To achieve this, the input signal, $\cos(\omega_{RF}t)$, is multiplied by a local oscillator, $\cos(\omega_{LO}t)$ to obtain a sinusoid at frequency $\omega_{IF} = \omega_{RF} - \omega_{LO}$.

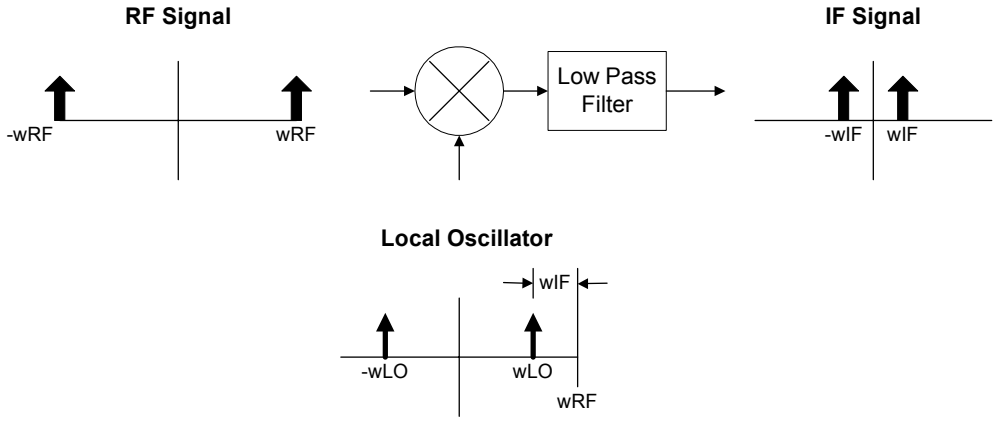

Figure 1 – Function of an Analog Mixer

Now consider the same input signal with an additional frequency component located at $\omega_{image} = \omega_{RF} - 2\omega_{IF}$, as illustrated in figure 2. Due to the properties of sinusoidal multiplication, both input components are converted to the same intermediate frequency. Once this mixing has occurred, the undesired input component, called the "image", effectively corrupts the desired signal and cannot be removed.

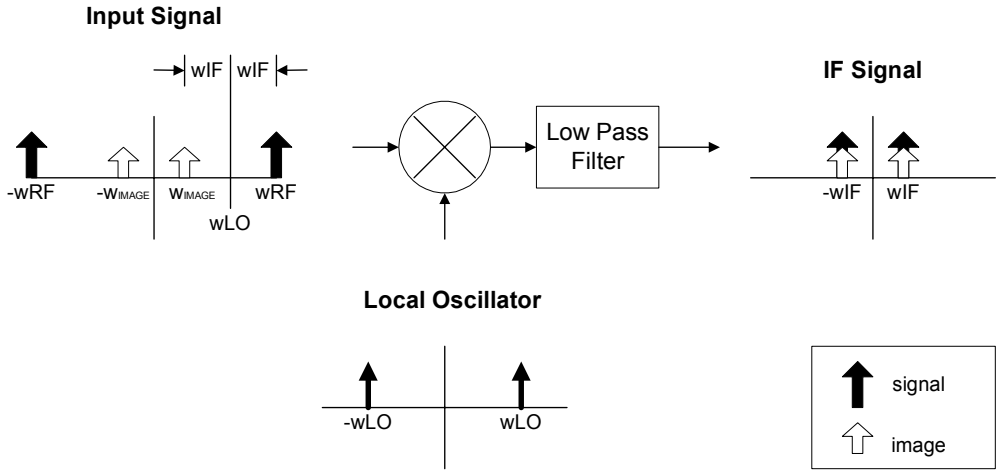

Figure 2 – Image Corruption of Desired Signal due to Mixing Operation

To alleviate the image problem, traditional homodyne and heterodyne receivers employ an explicit image-reject filter to suppress the image before mixing. Since the Q-factor requirements of this filter are extremely high, off-chip solutions such as surface acoustic wave filters are the conventional choice for this application. However, these filters have high power consumption and require off-chip implementation, which impedes the trend towards low-power, fully monolithic receivers. This has motivated RF designers to seek other techniques of rejecting the image [1].

This paper presents current techniques in the development of RF image-reject receivers. Section 2 reviews the fundamentals of basic image-reject architectures. Section 3 describes a novel, digitally-tuned image-reject receiver, while Section 4 suggests future trends in this area.

2.0 IMAGE-REJECT ARCHITECTURES

The basic objective of an image-reject receiver is to process and suppress the image-tone without utilizing an explicit, external filter. A useful metric to quantify the degree of image rejection in a receiver is the image rejection ratio (IRR), which is defined by:

$$IRR = \frac{desiredSignalLevel}{imageSignalLevel}$$

Typical wireless standards, such as DCS-1800, require an IRR of 1000 (60dB). In the ideal case, the image signal level is equal to zero, and IRR = ∞.

The following sections describe various image-reject receiver architectures and their strengths and limitations. Section 2.1 and 2.2 explore the basic Hartley and Weaver architectures, respectively, while section 2.3 presents a self-calibrating architecture that employs negative feedback.

2.1 Hartley Architecture

The Hartley architecture is the most basic image-reject architecture and is shown below in figure 3. The incoming RF signal is mixed with quadrature outputs of the local oscillator signal, namely $\sin\omega_{LO}t$ and $\cos\omega_{LO}t$, and fed through a low pass filter. The signal at node X, as illustrated in figure 4, is then shifted by 90 degrees by a RC-CR

network and then added with the signal at node B. It can be seen that the sum of A and B results in cancellation of the image, and leaves only the desired signal.

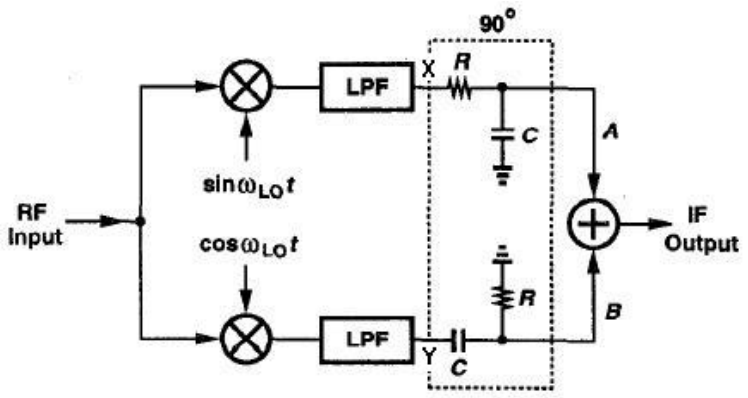

Figure 3 – Hartley Architecture [1]

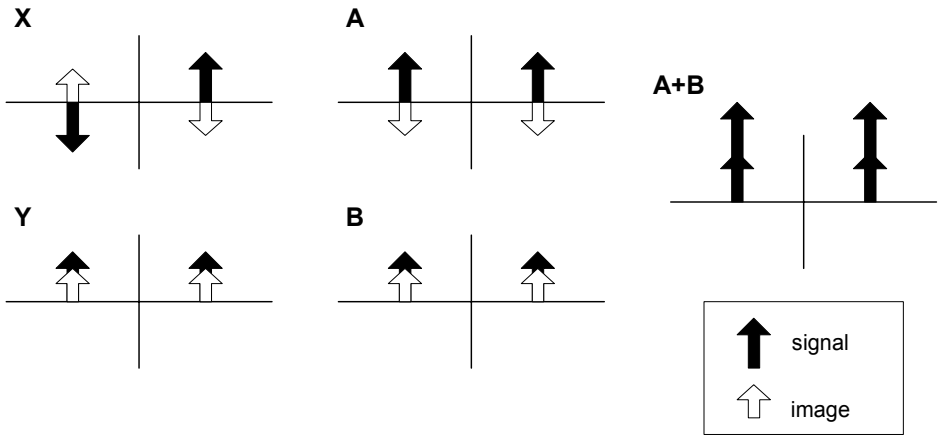

Figure 4 – Internal Signals of the Hartley Architecture

The principal drawback of the Hartley architecture is its sensitivity to mismatches [1]. If the gain and phase of the two signal paths are not perfectly balanced, the image is only

partially cancelled. Sources of mismatch include I/Q generation errors and the inaccuracy of R and C parameters due to process and temperature variation.

2.2 Weaver Architecture

To alleviate the mismatch problem associated with the 90-degree shift network in the Hartley architecture, the network can be replaced with a second quadrature mixing stage. The resulting topology is the Weaver architecture, which is illustrated in figure 5.

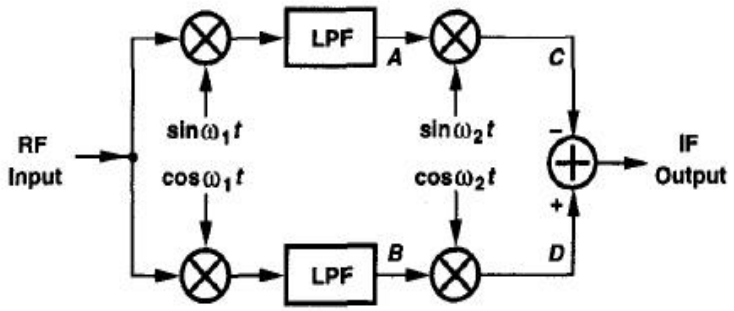

Figure 5 – Weaver Architecture [1]

The Fourier representations of the signals at nodes A to D are shown in figure 6. It can be seen that the second-stage quadrature mixers produce outputs whose difference cancels the image, while maintaining the desired signal.

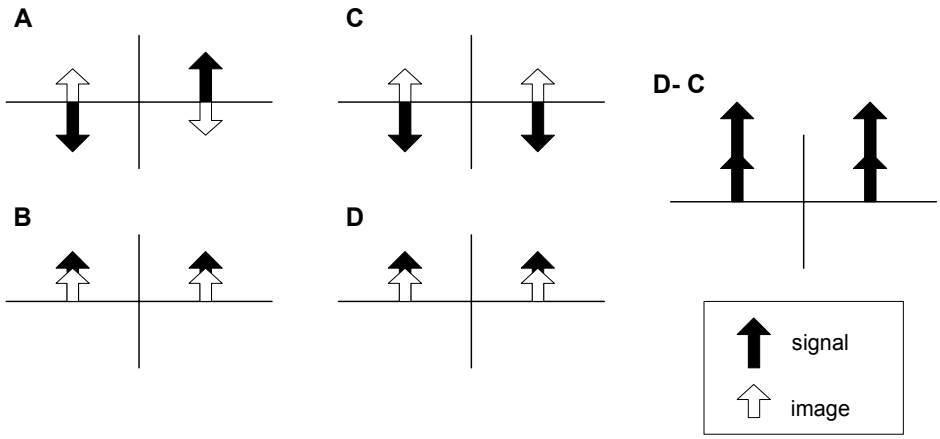

Figure 6 – Internal Signals of the Weaver Architecture

By avoiding the RC-CR network, the Weaver architecture achieves greater image rejection despite process and temperature variations [1]. However, because the circuit still depends on the precise cancellation of the image-tone through subtraction, gain and phase mismatches between the signal paths are still a critical problem.

The Hartley and Weaver architectures eliminate the need for an explicit image-reject filter, but their performance degrades considerably in the presence of gain and phase mismatches. A more convenient form of the IRR is given by [2] in terms of the phase mismatch, θ, and the relative gain mismatch, ΔA/A, between the two quadrature signal paths:

$$IRR = \frac{4}{\theta^2 + (\Delta A / A)^2}$$

where it is assumed that θ << 1 rad and ΔA << 1.

Basic Hartley and Weaver architectures, which depend on good layout techniques to ensure optimum matching, typically have image rejection ratios in the range of 30-35dB. This is far below the 60dB required by most wireless standards. As a result, much effort has gone into minimizing mismatches in the signal paths.

2.3 Self-Calibrating Architecture

Introduced in [2] by Montemayor and Razavi, the following topology determines the phase and gain mismatches of a Weaver architecture, and drives their magnitudes towards zero through use of a negative feedback loop. A simplified system diagram highlighting the generation of the phase error signal is shown in figure 7. The two mixers in the auxiliary path produce the signal, $\cos(\omega_{IF}t)$, which is mixed with the output voltage, V_{out}, to obtain the phase mismatch. The phase error signal obtained is given by $V_\theta = AV_m\sin(\theta/2)$, where A is the nominal voltage gain of each quadrature path, and V_m is the amplitude of the image-tone [2].

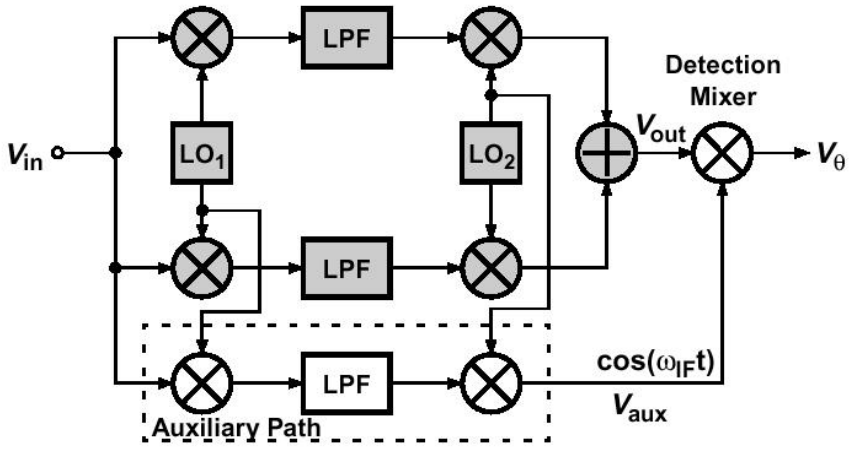

Figure 7 – Generation of the Phase Error Signal [2]

The phase mismatch information provided by V_θ can now be utilized in a feedback loop incorporating variable delay cells that adjust the signal or local oscillator phases [2]. This occurs during calibration, in which LNA_1 is disabled, and S_1 and LNA_2 are turned on. A calibration tone is then applied at V_{cal}, and the delay cells (denoted by Δ) are varied differentially to force the phase mismatch towards zero. After the feedback loop settles, S_1 and LNA_2 are turned off and the final value of V_θ is stored dynamically across the capacitor. This is apparent in the full system diagram shown in figure 8.

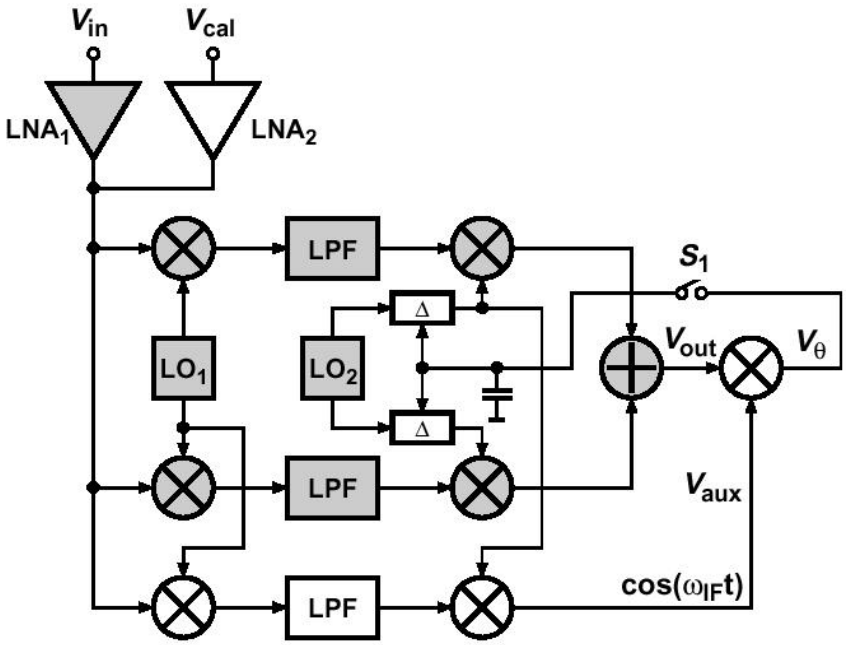

Figure 8 – Image-Reject Receiver with Phase Calibration Loop [2]

An apparent problem with this image rejection technique is the need to periodically refresh the value of V_θ stored on the capacitor. Furthermore, the power consumption increases by an overwhelming 62% (from 105mW to 170mW) when switched from

normal mode to calibration. Nonetheless, it is shown experimentally in [2] that addition of the negative feedback loop improves the IRR of the receiver from 17dB to 57dB. This is a considerable improvement over traditional “open loop” architectures.

3.0 IMAGE-REJECT RECEIVER WITH SS-LMS CALIBRATION

In [3], a novel image-reject receiver using digital tuning is presented. Based on the Weaver architecture, gain and phase mismatches are calibrated simultaneously by a sign-sign least mean square (SS-LMS) algorithm [3]. The system diagram is shown in figure 9.

Sections 3.1 to 3.3 describe the three main components added to the Weaver image-reject topology: the SS-LMS adaptation circuit, the variable delay cell, and the variable gain cell. Section 3.4 discusses the improvements of this topology over traditional image-reject architectures.

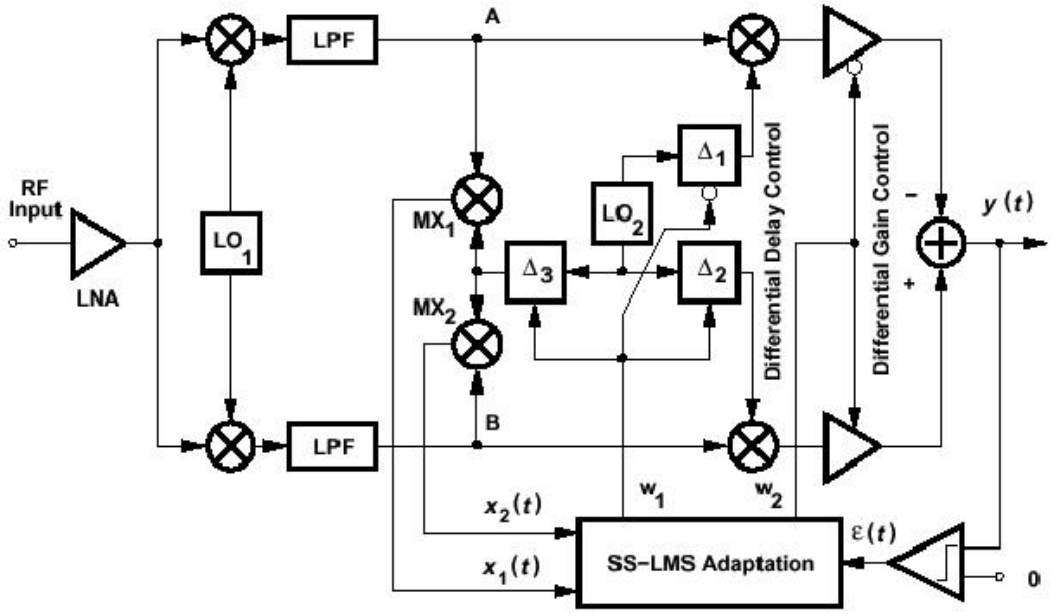

Figure 9 – Image-Reject Receiver with SS-LMS Calibration [3]

3.1 Sign-Sign Least Mean Square Adaptation Circuit

The SS-LMS adaptation circuit is responsible for adjusting the variable gain and variable delay cells so as to minimize the mismatches in the quadrature signal paths. In calibration mode, the difference of the two signal paths, y(t), is fed into a comparator to generate the error term, ε(t). Two additional mixers, MX_1 and MX_2, downconvert the signals at points A and B to generate $x_1(t)$ and $x_2(t)$, respectively. Using these three inputs, the circuit updates the control coefficients w_1 and w_2, according to the LMS algorithm given by [3]:

$$w_{1,2}[(m+1)T] = w_{1,2}[mT] + 2\mu\varepsilon[mT]x_{1,2}[mT]$$

where μ is the step-size and *m* is the discrete-time parameter. This process is repeated in discrete time steps until ε(t) = 0. At this point, the optimal values of w_1 and w_2 are finalized and the calibration procedure is terminated.

The implementation of this circuit is shown in figure 10. Note that because the LMS algorithm is replaced by the sign-sign LMS algorithm, only the signs of ε(t) and x(t) are multiplied. This significantly reduces the hardware complexity and power consumption of the circuit by allowing large digital multipliers to be replaced by XOR gates [3]. The XOR gates, in combination with the up/down counters, act as digital integrators, which vary the value of w_1 and w_2 according to the error term.

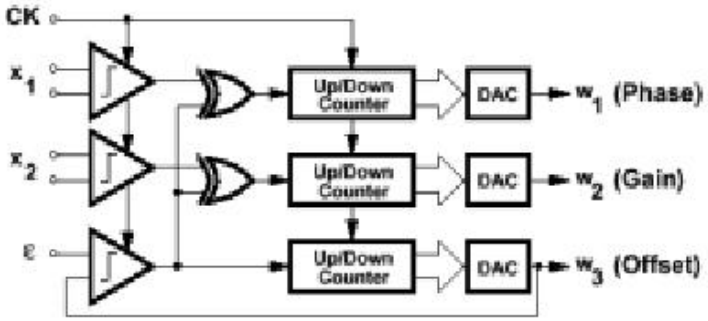

Figure 10 – SS-LMS Adaptation Circuit [3]

3.2 Variable Delay Cell

The variable delay cells, Δ_1, Δ_2, and Δ_3, are implemented using the circuit shown in figure 11. This circuit interpolates between the phases of a slow signal path ($M_{1,2,3,4}$) and a fast signal path ($M_{5,6}$), and produces an output signal that is the weighted sum of the two path delays. By applying the local oscillator signal to V_{in}, and the control signal w_1 to V_{ctrl}, the gain in each path can be adjusted to obtain the desired output delay.

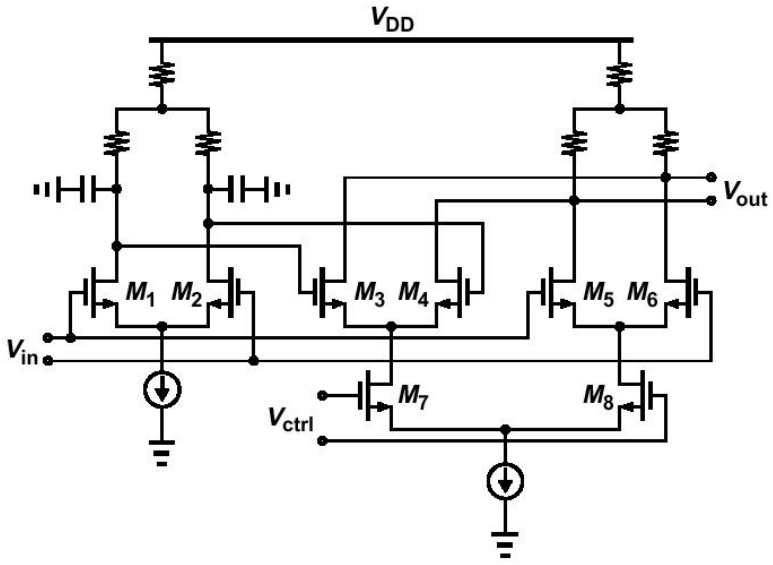

Figure 11 – Variable Delay Cell [2]

3.3 Variable Gain Cell

The variable gain cells use a fully differential, Gilbert Cell topology as shown in figure 12. Each cell consists of a main mixer, a variable gain mixer, and a gain control block. By differentially varying V_G with the SS-LMS coefficient, w_2, the overall gain of the cell can be controlled.

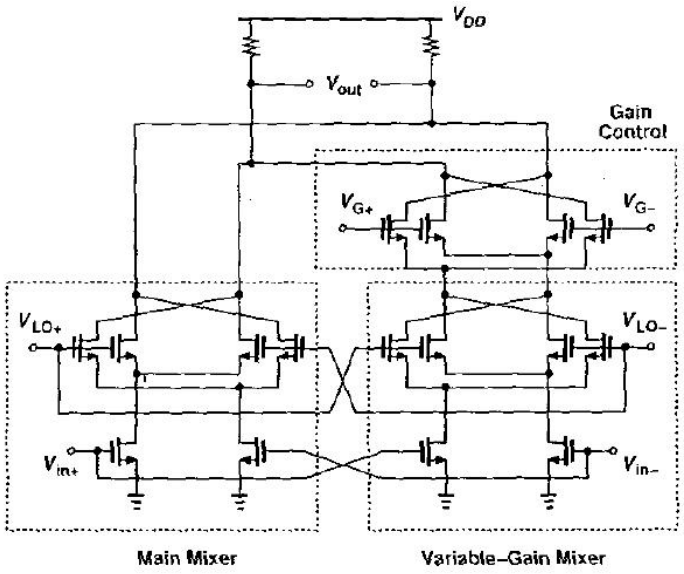

Figure 12 – Variable Gain Cell [3]

3.4 Improvements

Digital calibration offers several advantages over its analog counterpart. First, the mismatch control signals are constantly available from the SS-LMS adaptation circuit, which eliminates the need for periodic refreshing. This is essential in CDMA systems that must receive continuously [3]. Second, the additional power required during calibration over normal operation dramatically decreases. The circuit consumes 50mW during normal reception and 55mW during calibration [3]. This translates to a 10% power

increase compared with a 62% increase in the case of analog tuning. Finally, the circuit achieves the same IRR of 57dB while consuming only half as much power.

4.0 CONCLUSION

The demand for fully monolithic wireless receivers has fueled the development of new image-reject architectures that eliminate the need for explicit, off-chip filters. The novel CMOS image-reject receiver presented in [3] achieves this by digitally tuning out gain and phase mismatches to obtain superior image rejection. Current trends suggest the further use of digital tuning techniques to provide accurate, low power solutions that will enable greater receiver integration [4].

Future challenges in this area include the issue of recalibration. The need for recalibration is inevitable due to changing external conditions during transmission [4]. For TDMA systems, simply bounding calibration times to fit within idle time slots is sufficient. However, this would not work for CDMA systems that must receive continuously [3].

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