Eliyahu Zamir (961339780)

Low Voltage Standard CMOS Opamp Design Techniques

Student name: Eliyahu Zamir
Student number: 961339780
Course: ECE1352F
Proffessor: Khoman Phang

1.Abstract

In a never-ending effort to reduce power consumption and gate oxide thickness, the integrated circuit industry is constantly developing smaller power supplies. Today's analog circuit designer is faced with the challenges of making analog circuit blocks with sub 1V supplies with little or no reduction in performance. Furthermore, in an effort to reduce costs and integrate analog and digital circuits onto a single chip, the analog designer must often face the above challenges using plain "vanilla" CMOS processes. This paper will examine some of the specific challenges of, and proposed solutions to, designing one of the most popular and widely used analog building blocks, the Operational Amplifier (Opamp).

2.Introduction

Opamps are among today's most widely used circuit blocks. They can be used as summers, integrators, differentiators, comparators, attenuators and much more. Defined generally, an Opamp is a high-gain differential input amplifier [1]. Designers have been trying to integrate these versatile circuit blocks into the rest of their circuitry since the mid-1960s [2]. The µA709 was the first Opamp designed on an integrated circuit.

In an effort to reduce cost and space and improve performance, designers are integrating more and more circuit blocks, both analog and digital, onto a single chip. In order to reduce power dissipation, it is advantageous, at least for digital circuit blocks, to implement these "mixed-signal" chips in a standard CMOS process. In a

further effort to reduce power dissipation in digital circuit blocks, it is advantageous

to reduce the supply voltage Vdd. For a standard CMOS inverter, power dissipation

may be expressed as [3]:

$$Pavg = C_{load} \times Vdd^2 \times f_{clk} \qquad\qquad (2.1)$$

In an effort to increase the intrinsic gain of CMOS devices, the trend in the

MOSFET design industry is to shrink the gate oxide thickness, T_{ox}. Unfortunately, as

T_{ox} is reduced, the MOSFET device's tolerance for high voltage levels at the gate is

also reduced. This means that, for reliability purposes, it is advantageous to reduce

the maximum voltage supply Vdd.

This trend in reducing the supply voltage means that analog designers face

challenges such as reduced input common mode range, output swing and linearity.

Part of the problem is that V_{T0} does not scale in a linear fashion with the reduction in

minimum device length. V_{T0} is given by the following expression:

$$V_{T0} = V_{fb} + 2\boldsymbol{f}_F + \left(4e\boldsymbol{e}_r N_a \boldsymbol{f}_F\right)^{\frac{1}{2}} \frac{1}{C_{ox}} \qquad\qquad (2.2)$$

Most of the values in equation 2.2 remain relatively constant as minimum process

lengths and supply voltage are scaled down. Therefore, a decrease in V_{T0} can usually

only be brought about by a decrease in N_a or by an increase in C_{ox}. Unfortunately for

the designer, V_{T0} does not tend to decrease at the same rate as Vdd.

Some fabs do offer low V_{T0} processes specially suited for analog blocks.

However, they tend to cost more than standard CMOS processes. It is therefore

desirable to use low voltage design techniques, in order to be able to implement

analog circuit blocks using standard CMOS processes.

This paper will discuss techniques for implementing low supply voltage Opamps

using a standard CMOS process. It will begin by presenting some of the more

traditional low voltage Opamp design techniques, such as the folded cascode

structure. The paper will then present some more recent developments in Opamp

design, such as Floating Gate CMOS (FGCMOS) and Bulk driven input stages.

3. Low Voltage Opamp Solutions

3.1. Folded Cascode Opamp

The typical differential pair, shown in figure 1, normally consists of 2 transistors

connected in a common source amplifier configuration. The differential gain of this

amplifier is given by:

$$A = -gm_{1,2}R_{out} \hspace{4cm} (3.1.1)$$

In an effort to increase the gain of this differential pair, it can be connected in

cascade with a common gate amplifier, as shown in figure 2. This is known as a

cascode configuration. Its differential gain is given by:

$$A_{cascode} = A_{commonsource} \times A_{commongate}$$
$$A_{cascode} = -gm_{1,2}r_{o(1,2)} \times gm_{3,4}r_{o(3,4)}$$

(3.1.2)

This very large gain comes at a price. The extra transistors $M_{3,4}$ require an extra

Veff from the total supply headroom budget. If however $M_{3,4}$ are chosen as PMOS

devices and placed in the folded cascode configuration, shown in figure 3, then at the

cost of some extra current, this configuration takes up the same amount of voltage

headroom as that of the simple differential pair shown in figure 1.

In the case of an NMOS input differential pair, the input transistors must have a

bias high enough so that the tail current source transistor remains in the active region.

In the case of a PMOS input differential pair, the input must be biased low enough so

that the tail current source transistor remains in the active region. In other words,

$$V_{cm(\min)} = Veff + |Vt| \leftarrow NMOS$$
$$V_{cm(\max)} = Vdd - (Veff + |Vt|) \leftarrow PMOS$$

(3.1.3)

Given a typical modern process with a Vtn=0.5V and a Veff of 0.2V, this means

that the minimum input common mode voltage is limited to about 0.7V. This

configuration is clearly not suitable for sub 1V supply applications. One solution is to

use a complementary input differential pair, such as the one suggested Roewer et al

[5].

The complementary input Opamp discussed in the above paper is shown in figure 4. The input of this Opamp has both an NMOS and a PMOS differential pair. In effect, there are two Opamps at the input, as shown in figure 5. The output signals from these Opamps are then summed together using a class-AB output stage formed by transistors $M_{7,8}$. When the input common mode level approaches ground, the NMOS input devices turn off, leaving only the PMOS input devices to contribute gain to the Opamp. When the input common mode level approaches Vdd, the PMOS devices turn off, leaving only the NMOS devices to contribute gain to the Opamp. Unfortunately, the complementary input configuration may contain an undesirable "dead-zone" in the input common mode range. In this "dead-zone", the DC bias level is too high for the PMOS input, but not high enough for an NMOS input. The designer must ensure that there is sufficient overlap of $V_{cm(in)}$ where both the PMOS and NMOS differential pairs are active.

For example, using a typical modern process where Vtn=0.5V, and Vtp=-0.7V, and the current sources are biased to have a Veff=0.2V, equation (3.3) gives us;

$$V_{cm(\min N)} = 0.7V \leftarrow LimitedbyNMOSdiffpair$$
$$V_{cm(\max P)} = Vdd - 0.9V \leftarrow LimitedbyPMOSdiffpair$$

With a 1V supply, this would leave a "dead-zone" between 0.1V and 0.7V. Clearly, the complementary input stage is also not ideal for ultra-low supply voltages.

In the following sections some more recent Opamp design techniques will be

presented. These circuits are much more suitable to sub 1V supply environments.

3.2. Floating Gate CMOS (FGCMOS) Opamps

Floating gate transistors have mainly been used in EPROM and EEPROM circuits

[6]. Shown in figure 6, the FGCMOS transistor is AC coupled at the gate. The

transistor's gate then has a charge placed on it, using either UV radiation, or high

voltage pulses (e.g. 20V) [6], which biases the device at the desired level. This charge

can remain constant without any need for reprogramming for over 10 years [6].

Because the transistor is now AC coupled, the input common mode voltage can be at

almost any level.

The FGCMOS "pseudodifferential" pair proposed in [7] is shown in figure 7.

Here, inputs V1 and V2 are connected to the gates of FGCMOS $M_{1a,1b,2a,2b}$.

Transistors $M_{1a,2a}$ are in a diode connected differential pair arrangement, which

mirrors half of bias current I_b to the output. Small signal inputs $V_{1, 2}$ are amplified and

converted into small signal output currents through cascode transistor pairs $M_{1b,1c}$ and

$M_{2b, 2c}$ respectively. This arrangement allows rail-to-rail input voltage and large

differential transconductance gain G_{dm}. Figure 8 shows the experimental

transconductance gain achieved for several different bias currents, in a 1.2um process,

and with a 1.6V supply. Clearly, this circuit topology is well suited to very low input

supply voltages. Unfortunately, this topology has a limited output voltage. In order

for all transistors to remain active, the drains of transistors $M_{1c, 2c}$ must remain at least

2Veff from ground. If rail-to-rail output voltage is desired, a different approach must

be used.

One such approach is the use of FGCMOS transistors in an analog inverter

configuration. An FGCMOS differential pair was implemented in [8] using basic

analog inverter building blocks, shown in figure 9. When the transistor's gates are

programmed such that the inverter is in equilibrium (i.e. Vout=Vdd/2), it can be

shown that [8]:

$$I_p = I_n = Ibec \times e^{\frac{k_i}{nU_t}\left(\frac{Vdd}{2}-Vin\right)} e^{\frac{k_i}{nU_t}\left(\frac{Vdd}{2}-Vout\right)} \qquad (3.2.1)$$

Where Ibec is the equilibrium large signal current, $k_i = C_i/C_t$, and nU_t are constants.

Vout is then [8]:

$$Vout = \left[\frac{(A+1)}{2}\right]Vdd - AVin \qquad (3.2.2)$$

, $A = \dfrac{k_i}{k_t}$, k_t= sum of all k_i

Note that for a single input inverter, the gain A=1, and as more inputs are used,

gain is decreased. For the differential amplifier shown in figure 10, the maximum

gain achievable is A=1/2. This is clearly not very useful for an Opamp in most

applications. However, some specialized applications that do not require much gain,

such as an Opamp comparator, may still find the FGCMOS differential analog

inverter quite useful for ultra-low supply applications.

Another problem faced by all FGCMOS input devices is that their input coupling

capacitors tend to take large die areas. Therefore, FGCMOS could prove to be an

expensive solution to the low voltage supply challenge. Furthermore, placing

capacitors at the input of an Opamp makes it unsuitable for very low frequency

operation.

3.3. The Bulk driven amplifier

In the past, analog designers have often taken for granted that a MOSFET

transistor is actually a four terminal device. The Bulk terminal is usually ignored and

simply connected to ground or Vdd, or tied to the source terminal. Recently, however,

it has been discovered that the Bulk terminal may be used as a small signal input in a

completely novel family of amplifiers that are very well suited to an ultra-low supply

environment.

The Bulk driven input stage, shown in figure 11, modulates the threshold voltage

to produce a transconductance gm_b given by [9]:

$$gm_b = \frac{di_D}{dv_{BS}} = \frac{\boldsymbol{g} \times gm}{2\sqrt{2\boldsymbol{f}_F - V_{BS}}} \qquad (3.3.1)$$

It can be shown that the gain of a Bulk driven amplifier can actually exceed that

of a standard common source input differential stage when [9]:

$$V_{BS} \geq 2\boldsymbol{f}_F - 0.25\boldsymbol{g}^2 \qquad (3.3.2)$$

A rail-to-rail input and output Opamp, shown in figure 12, was presented in [9]. With only a 1V supply, this Opamp has 48.8dB gain and a 1.3Mhz unity gain frequency. This design demonstrates that Bulk driven input stages are well suited for ultra-low voltage Opamps.

Unfortunately, the favourable properties of the Bulk driven input stage do not come without their drawbacks. Increasing the input common mode voltage V_{BS}, whether for the purposes of increasing the gain of the Opamp, or simply to attain rail-to-rail input common mode, comes at the price of power dissipation.

The drain current of an active MOSFET transistor is given by:

$$I_D = \frac{m_n C_{ox}}{2} \frac{W}{L} \left(Vgs - V_T\right)^2 \left(1 + \boldsymbol{l} Vds\right) \tag{3.3.3}$$

When the V_T term is expanded to account for the Body effect, the equation becomes:

$$I_D = \frac{m_n C_{ox}}{2} \frac{W}{L} \left(Vgs - V_{T0} - \boldsymbol{g}\sqrt{2\boldsymbol{f}_F - V_{BS}} + \boldsymbol{g}\sqrt{2\boldsymbol{f}_F}\right)^2 \left(1 + \boldsymbol{l} Vds\right) \tag{3.3.4}$$

Equation 3.3.4 shows that, as V_{BS} increases, the Veff term also increases, producing a larger drain current. Another drawback of this type of input stage is that as the bias voltage to the Bulk changes, the size of the depletion region between the Bulk and substrate changes. This means that the input capacitance will now be dependant on the input Bulk bias[10].

4. Conclusion

Four different approaches to designing a low voltage Opamp were presented in

this paper.

1. The **folded cascode Opamp** is useful for moderately low supply voltages, at

    the cost of some extra current, but has limited performance in sub 1V

    applications, as well as a limited $V_{cm(in)}$.

2. The **complimentary input stage** helps to increase the input common mode

    voltage range, at the price of some extra transistors and current. However, it is

    susceptible to a dead-zone, where neither NMOS nor PMOS differential pairs

    are in the active region.

3. The **FGCMOS input stage** allows a rail-to-rail input common mode voltage

    range, at the cost of limited low frequency capabilities, and large, die area

    consuming capacitors.

4. The **Bulk driven amplifier input stage** allows a rail-to-rail input common

    mode voltage range, with substantial gain, at the cost of some extra power

    dissipation and a large Bulk bias dependant input capacitor.

All four options proposed in this paper have their own performance and cost

tradeoffs, and some may be more useful for certain applications than others. As

supply voltages continue to scale down, and performance demands increase, the

decision to make these tradeoffs will become increasingly important and difficult.

Eliyahu Zamir (961339780)

5. <u>References</u>

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[10] Troy Stockstad, Member, IEEE, and Hirokazu Yoshizawa, "A 0.9 V 0.5 uA Rail-to-Rail CMOS Operational Amplifier", IEEE journal of solid state circuits, Vol. 37, No.3, March 2002.
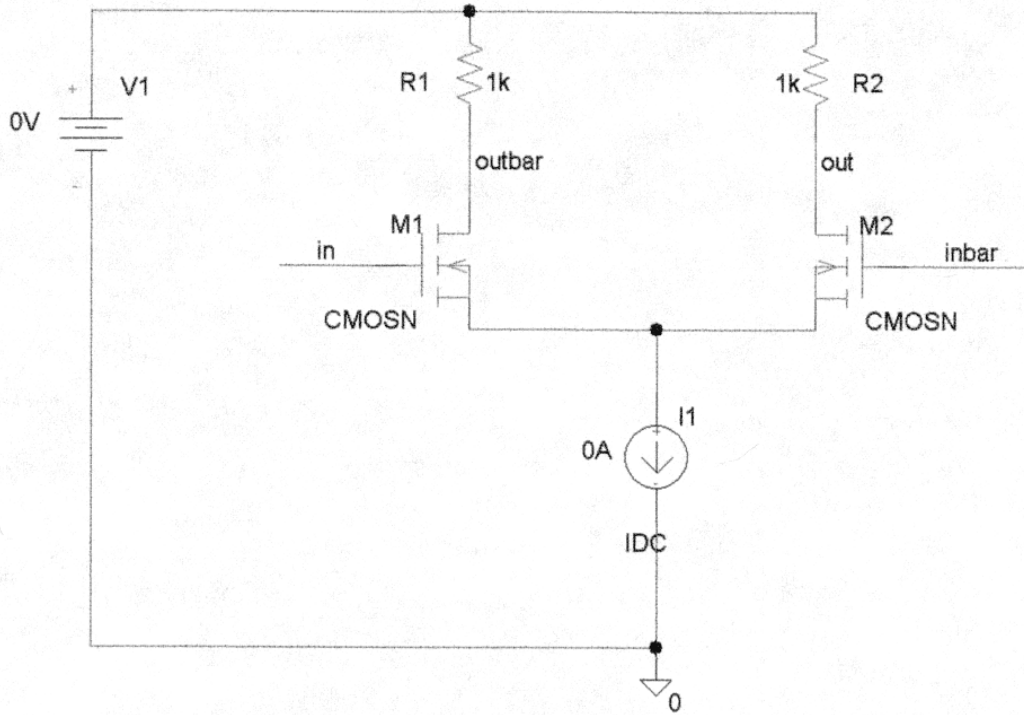
6. Figures

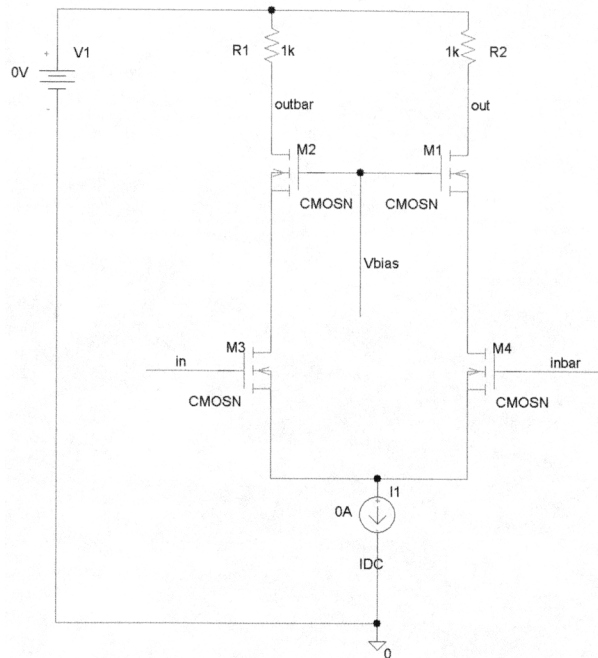**Figure 1. Standard NMOS Diffpair**
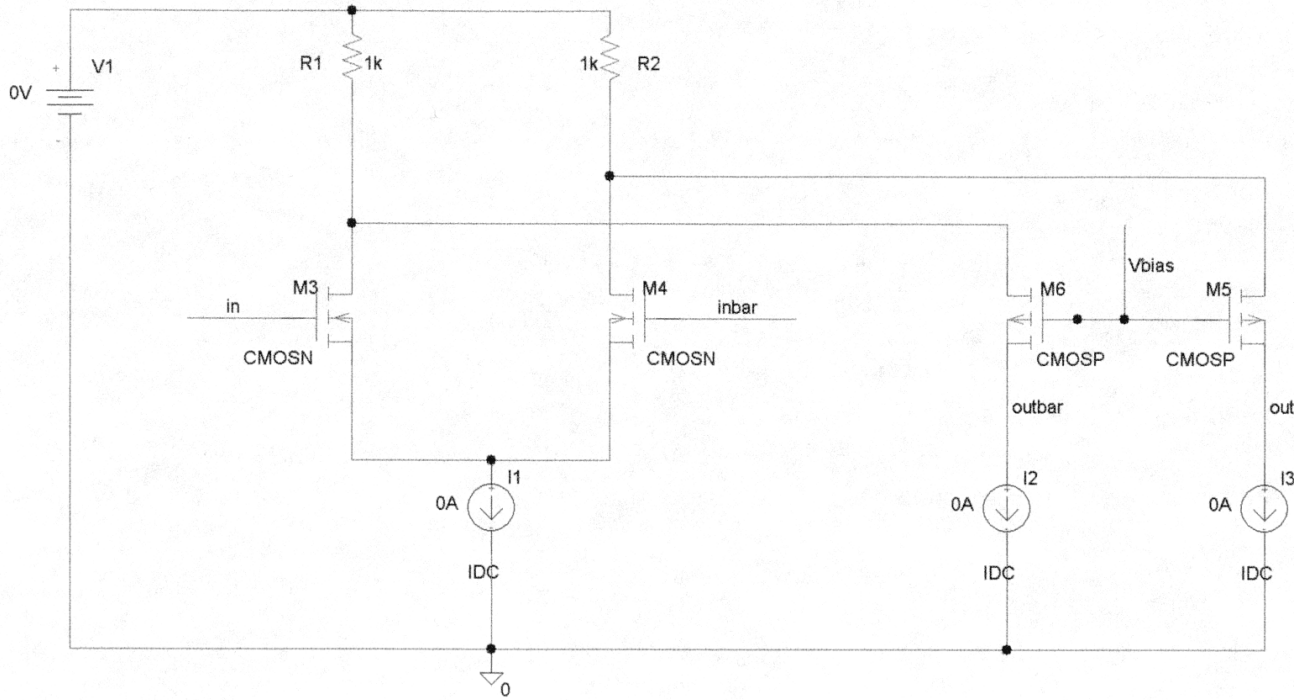

Figure 2. Cascode Differential Amplifier

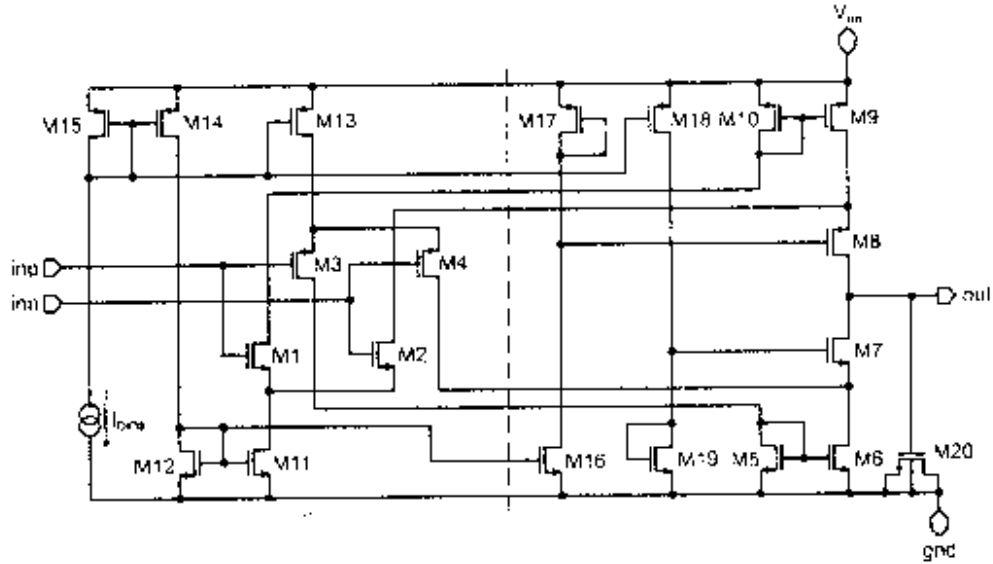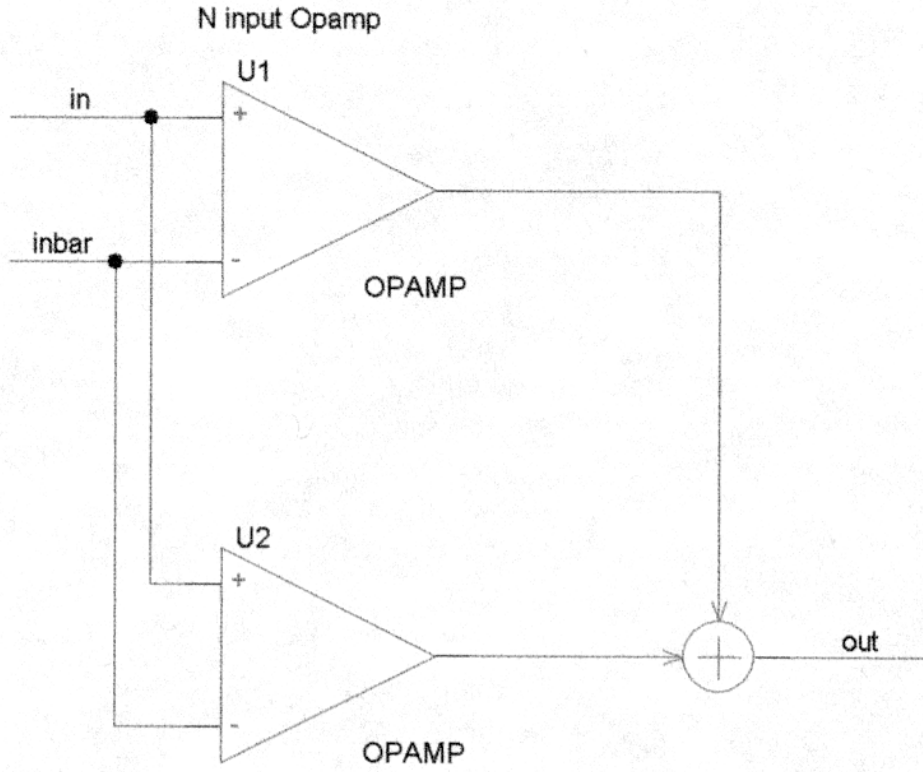**Figure 3. Folded Cascode Differential Amplifier**

Figure 4. Complimentary Differential Input Schematic [5]

N input Opamp

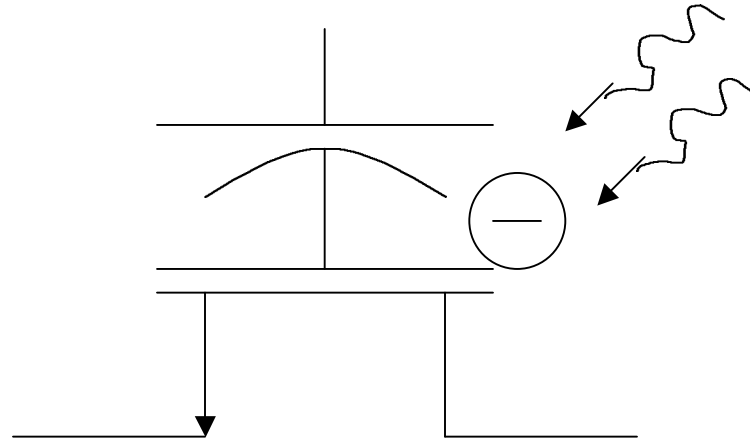**Figure 5. Complimentary input Differential pair block diagram**
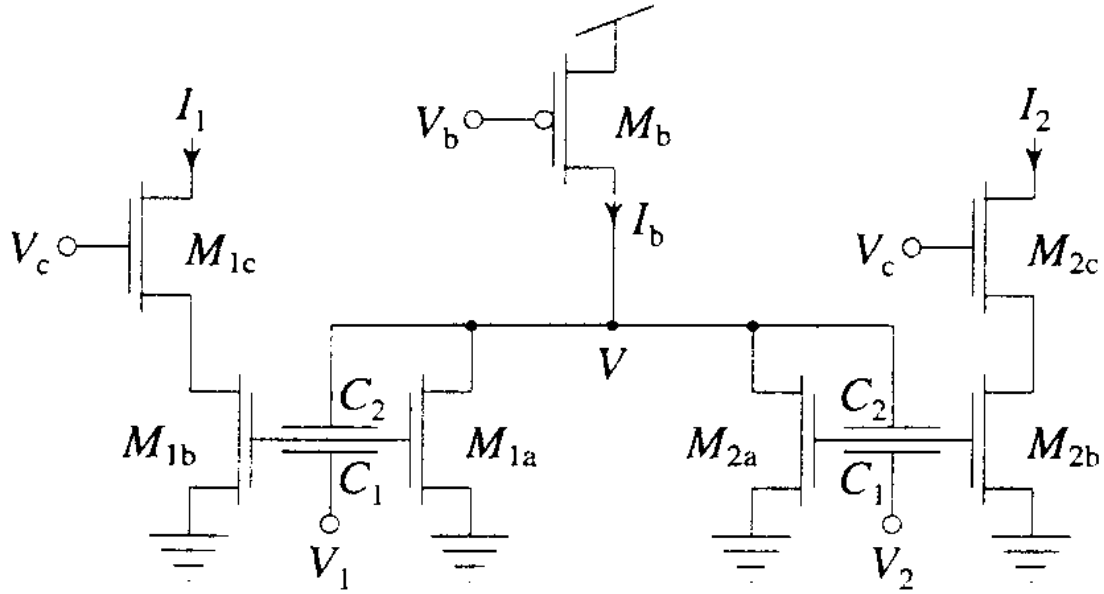
Figure 6. Programing a Floating Gate Transistor
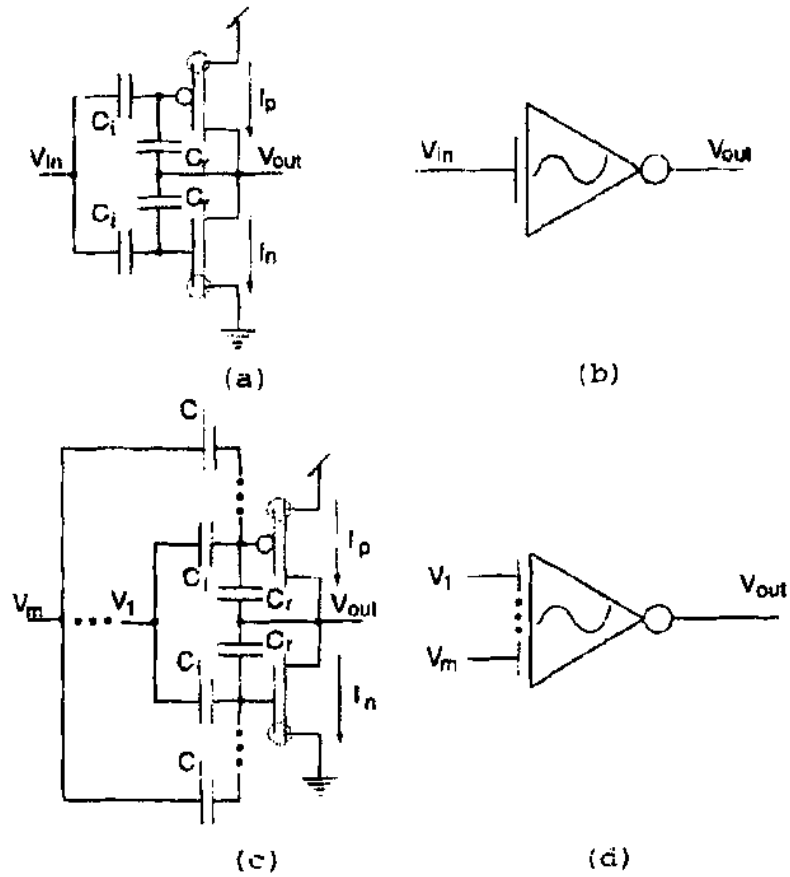
Figure 8. Floating gate Pseudodifferential Pair [7]

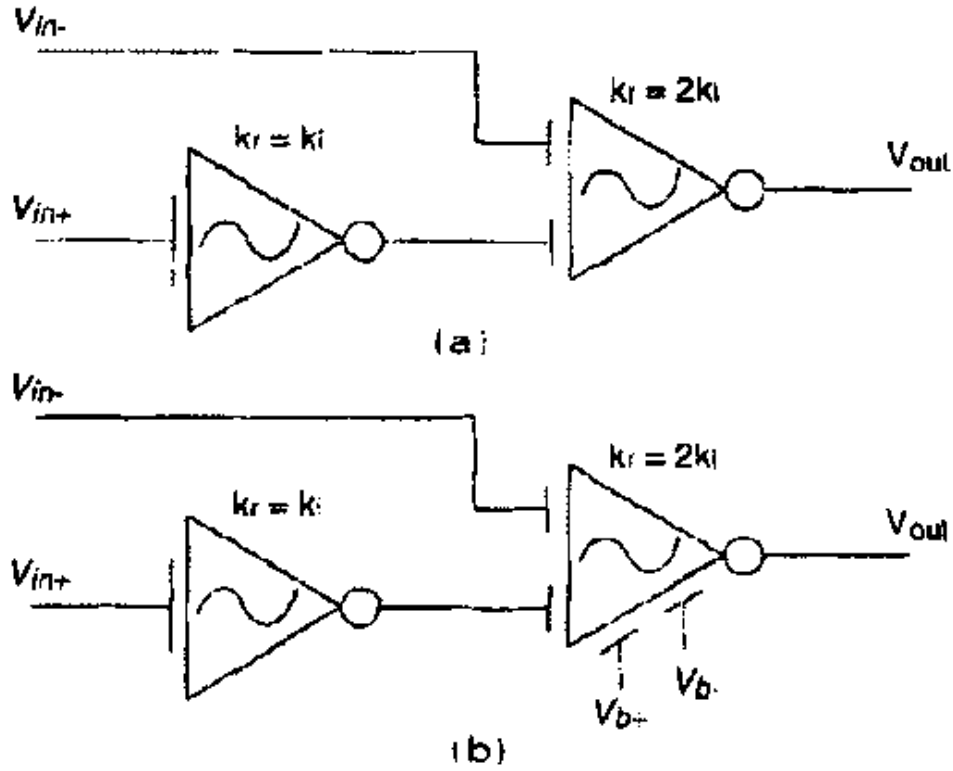**Figure 9. Floating gate Analog Inverter [7]**

Figure 10. Floating Gate Analog Inverter Differential Pair [8]

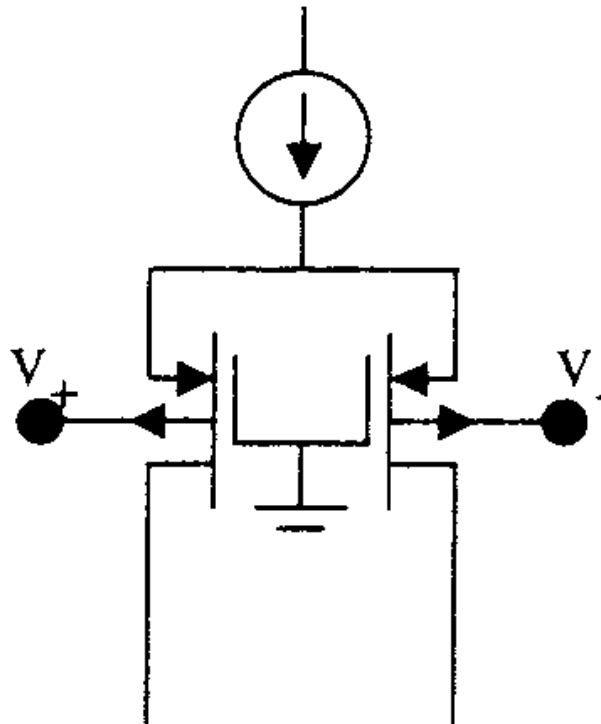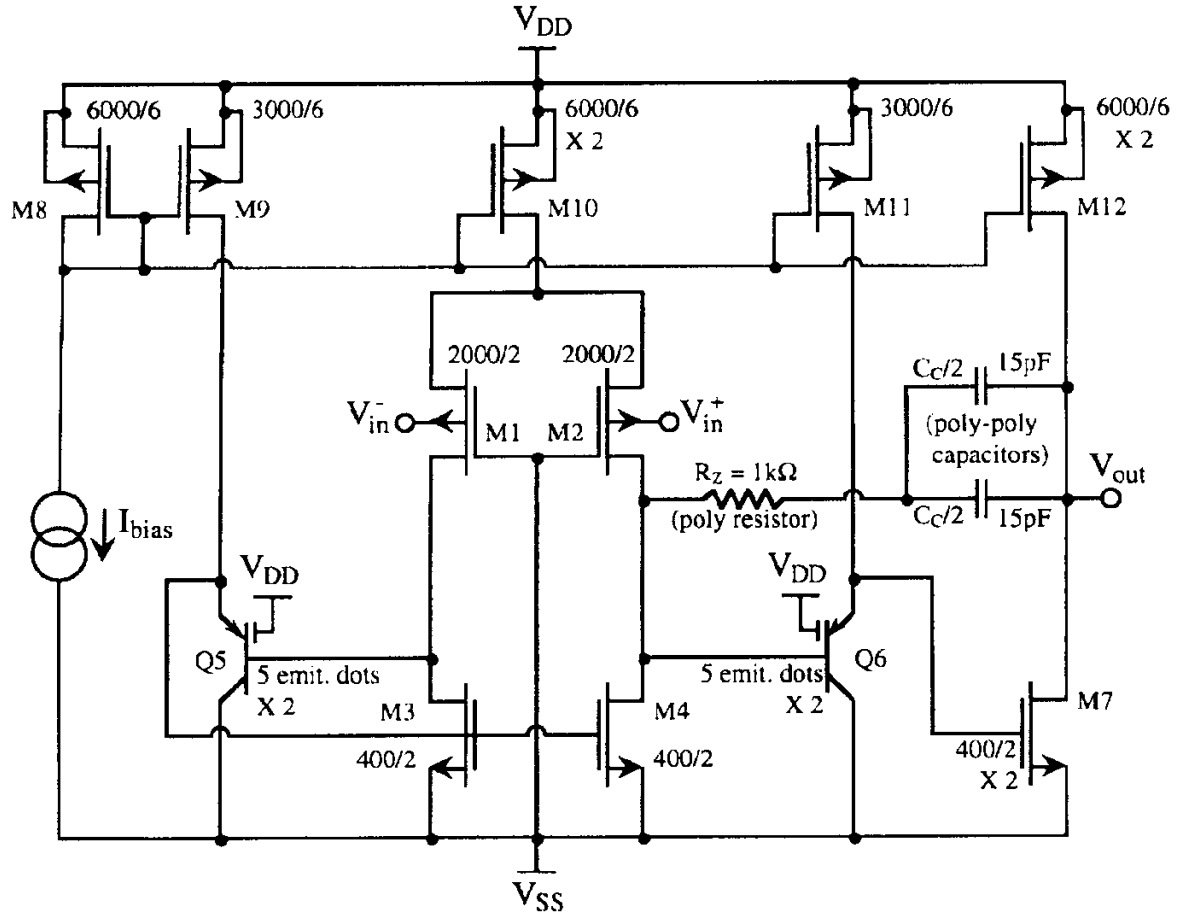**Figure 11. Bulk driven Amplifier [10]**

Figure 12. Bulk driven Opamp Schematic [10]