A Transimpedance Amplifier With DC-Coupled Differential Photodiode Current Sensing For Wireless Optical Communications

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Abstract

A transimpedance amplifier with differential dc-coupled photocurrent sensing was integrated in a standard 0.35 μm CMOS. It achieves 33KΩ transimpedance gain and a bandwidth of 255 MHz with a 2pF photodiode capacitance. This design exhibits 40dB power supply rejection ratio and an average input noise of (√(6.8pA))/√(Hz). Power dissipation is 30mW from a 3V supply.

Introduction

High-speed free-space optical receivers require a transimpedance amplifier (TIA) at their front-end to accommodate photodiodes with a wide field of view and hence a large depletion capacitance (1-10pF). Despite this significant capacitive node at the input, the desired TIA's should still provide wide bandwidth, high gain, and good sensitivity. These receivers find their application in laptop computers, personal digital assistants (PDAs), digital cameras and many other equipment supplied with a short distance infrared communication port. CMOS is the preferred technology for its low cost and ease of integration. However, building single-chip optical receivers in CMOS technology is challenging because of low supply voltages, small transistor transconductances, and large substrate noise making it difficult to achieve high bandwidth and good sensitivity. In wireless optical communications, TIAs also encounter ambient light perturbation. Intense background light can reduce output swing or even saturate the front-end preamplifiers.

Different architectures have been proposed to improve sensitivity at the input of transimpedance amplifiers. Reported designs in [1] and [2] have introduced a fully differential structure to reject common-mode substrate and power supply noise, but continue to sense the photocurrent single-endedly. To maintain symmetry at the input of the aforementioned designs, an additional capacitor or current source is attached to the other input terminal. Since common-mode rejection principally relies upon the symmetry of the signal path, such designs are prone to degraded performance as a result of poor matching and variations in the photodiode characteristics due to temperature and process. In comparison, an ac-coupled photodiode current sensing configuration in [3] and [4] suffers from the difficulty of realizing on-chip capacitors and photodiode bias fluctuation with ambient light variation.

Bandwidth improvement has been practiced by exploiting common-gate transistors at the input of transimpedance amplifiers [1], [5] and [6]. Common-gate transistors with low input impedances isolate the photodiode capacitance from the rest of the circuit and so the dominant pole at the circuit will no longer be a function of the input capacitance.

This paper presents a new transimpedance amplifier configuration with the capability of differential photodiode current sensing without any need for ac coupling capacitors by using common-gate transistors at the input. In essence, this structure benefits from numerous advantages. It provides a regulated photodiode biasing under ambient light intensity variations. It also boosts the signal power at the output by 6dB while increasing the noise power by 3dB resulting in an overall sensitivity improvement of 3dB. As well, it provides higher bandwidth by removing the dominant pole from the input terminal. It also demonstrates better common-mode noise rejection due to the balanced configuration. Finally, this design includes a dc photocurrent rejection circuit at the front of the TIA to remove any low-frequency signal caused by background light.

Preamplifier Architecture

Fig. 1 shows the simplified schematic of the proposed preamplifier structure. The circuit is composed of three sections, the photodiode bias input stage, the differential amplifier, and the dc photocurrent rejection feedback loop. Transistors M_{b3} and M_{b6} regulate the reverse bias voltage across the photodiode. A regulated cascode circuit (RGC) is employed to reduce the input impedance seen at the sources of M_{b3,6}. These transistors provide a common-gate input buffer stage to the transimpedance amplifier. Transistor M_{b4} is added to improve the symmetry of the signal path. The dc rejection feedback loop consists of an error amplifier and a differential pair made up of transistors M_{b1} and M_{b2}. Current sources I_1 and I_2 bias the cascode transistors.
In the absence of any dc photocurrent, all currents sourced by $I_1$ and $I_2$ will be drawn away from the amplifier by the differential pair $M_{b1}$ and $M_{b2}$. The presence of a dc photocurrent, $I_0$, which can be generated by the background light, results in a negative differential offset voltage at the output of the amplifier. This offset causes the error amplifier to change the differential voltage applied to the differential pair. In steady state, the bias current increases by $I_0$ for $M_{b1}$ and decreases by $I_0$ for $M_{b2}$ as illustrated in Fig. 1 to prevent differential amplifier saturation caused by dc current. In contrast, for the actual signal current $i_s$, the differential pair appears as a high impedance path. As a result, $i_s$ passes through to the amplifier where it is sensed differentially.

\[ P_1 = \frac{1}{2R_{in}C_{pd}} \]  

Fig. 1 Basic structure of the proposed optical preamplifier

![Fig. 1 Basic structure of the proposed optical preamplifier](image1)

The photodiode biasing circuit including the common-gate and RGC transistors is shown in Fig. 2. The reverse bias voltage on the photodiode is determined by the voltage differences at the sources of $M_{b3}$ and $M_{b6}$. The differential input impedance of this circuit is

\[ R_{in} = \frac{2}{g_{mb6}(1+g_{mc2}R_d)} \]  

(1)

Basically, it is the input impedance of a simple common-gate stage reduced by the factor $1 + g_{mc2}R_d$ which in turn improves the bandwidth by shifting the input pole to higher frequencies. Some design considerations which limit the minimum achievable input impedance include the allowable voltage drop across $R_d$, power consumption, and frequency response of the feedback circuit. For the differential configuration, the impedance looking into the bias circuit will be twice that given in (1). The frequency pole resulting from the depletion capacitance of the photodiode, $C_{pd}$, and the differential input impedance $2R_{in}$ is

\[ P_2 = \frac{1}{2R_{in}C_{pd}} \]  

(2)

Fig. 2 Photodiode bias input stage

![Fig. 2 Photodiode bias input stage](image2)

Fig. 4 shows the schematic diagram of the differential amplifier. The gain of the circuit is given by

\[ \frac{2A_{vd}}{1+A_{vd}} \frac{R_f2}{R_2} = 2R_f2 \quad \text{for} \ A_{vd} = 1 \]  

(3)

where $A_{vd}=g_{m1}R_f1$ is the open-loop voltage gain of differential amplifier and $g_{m1}$ is the transconductance of the input differential pair [2]. The bandwidth of this amplifier is dependent on the capacitance seen at the input terminals as well as the frequency response of the second stage. A small-signal model for the second stage of the amplifier is shown in Fig. 3 where $C_{f1}$ is the total shunt feedback capacitance bridging the drain and gate of $M_{11}$ or $M_{12}$ while $C_i$ and $C_o$ are the equivalent input and output capacitances, respectively. Because of the presence of two capacitors, $C_i$ and $C_o$, the second stage exhibits a second-order response. Shunt feedback capacitor, $C_f1$, introduces a zero at high frequencies but keeps the number of poles the same, by which it provides a degree of freedom to tune the pole locations for frequency and transient response optimization.

![Fig. 3 simplified small model for the second stage of the differential amplifier](image3)
choosing an optimum size and bias current for the transistors involved in the above equation, it is shown in [5] that the input noise current spectral density in the RGC input stage is less than that of a simple common-gate input stage. It is worth noticing that in the single-ended circuit of Fig. 5, the voltage drop across $R_d$ is controlled by the sum of gate-source voltages of $M_{c2}$ and $M_{b6}$. This poses another limitation on the $R_d$ resistance as well as $M_{c2}$ and $M_{b6}$ bias currents and sizes. In the differential RGC input, $M_{c2}$ source is virtually grounded and there is more flexibility for the circuit designer to improve noise and bandwidth performance.

**Experimental Results**

Testing and characterization of the circuit was performed utilizing an on-chip differential output buffer for driving 50Ω loads. A summary of the measured performance is given in Table 1. Fig. 6 depicts the TIA frequency response with $C_{pd}$ ranging from 0.5pF to 10pF. It can be seen that despite a 20 fold increase in $C_{pd}$, the bandwidth has only decreased by a factor of two. In Fig. 7, the output noise spectral density demonstrates a slight positive slope within the -3dB bandwidth as predicted by the given equation. Figs. 8 and 9 show output eye diagrams for 200Mbps and 400Mbps PN-sequence inputs, respectively. Fig. 10 illustrates the chip layout.

![Fig. 4 Differential amplifier circuit](image)

For noise calculation, although shot noise can dominate under intense background light, we need to analyze the circuit’s inherent thermal noise for a generalized application environment. To do so, the exact approach in [5] can be followed by considering the input half circuit of Fig. 5 where a single transistor, $M_{c31}$, represents the current source $I_2$.

![Fig. 5 Input half-circuit used for noise calculation](image)

The input equivalent noise current can be approximated by

$$
\overline{I_{n,\text{in}}} = \frac{4kT}{R_f} + \frac{4kT}{3\gamma m_{c1}} + \frac{4kT}{3\gamma m_{b2}} + \frac{8kT}{\gamma m_{c2}}\left(\frac{\omega^2}{2C_{pd}}\right)
$$

(4)

In this equation, the noise for $M_{b4}$ is cancelled because it is placed in series with $M_{b2}$ and also, junction capacitors at the input have been ignored in comparison with $C_{pd}$. As seen from this equation, noise contribution by the common-gate transistor $M_{b6}$ is removed; this is because of the existence of local feedback created by the RGC block.
Table 1: Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Vdd)</td>
<td>3.0V</td>
</tr>
<tr>
<td>Power Dissipation (excluding output buffer)</td>
<td>30mW</td>
</tr>
<tr>
<td>-3dB Bandwidth</td>
<td></td>
</tr>
<tr>
<td>Cpd=0.5pF</td>
<td>290MHz</td>
</tr>
<tr>
<td>Cpd=2pF</td>
<td>255MHz</td>
</tr>
<tr>
<td>Cpd=5pF</td>
<td>210MHz</td>
</tr>
<tr>
<td>Cpd=10pF</td>
<td>150MHz</td>
</tr>
<tr>
<td>Average Input Noise</td>
<td></td>
</tr>
<tr>
<td>Cpd=0.5pF</td>
<td>6.0pA/√Hz</td>
</tr>
<tr>
<td>Cpd=2pF</td>
<td>6.8pA/√Hz</td>
</tr>
<tr>
<td>Cpd=5pF</td>
<td>8.7pA/√Hz</td>
</tr>
<tr>
<td>Differential Transimpedance Gain</td>
<td>90.4 dBΩ</td>
</tr>
<tr>
<td>PSRR</td>
<td>40dB @ 20MHz</td>
</tr>
<tr>
<td>Max. Differential Output Swing with 50Ω Load</td>
<td>1Vpp</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35μm, CMOS</td>
</tr>
<tr>
<td>Active Area</td>
<td>300μm x 155μm</td>
</tr>
</tbody>
</table>

**Conclusion**

A fully differential transimpedance amplifier with a differential regulated cascode circuit at the input provides a gain-bandwidth of 8.4 THz-Ω with 2pF photodiode capacitance while exhibiting an input referred noise current of (6.8pA)/√Hz. Differential photodiode current sensing and its dc coupling structure provides a high PSRR of 40dB. An embedded error amplifier at this circuit, prevents the amplifier saturation caused by the background light as well as cancelling any offset at the output. This transimpedance amplifier is designed for a 3V, 0.35μm CMOS process.

**References**


