ECE-1768: Reliability of Integrated Circuits

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Prerequisite: ECE-302, or equivalent.

Text: E. A. Amerasekera and F. N. Najm, "Failure Mechanisms in Semiconductor Devices," 2nd Ed., John Wiley & Sons, 1997.

General Description: Reliability of integrated circuits has become increasingly important due to the very high levels of integration in common use today. In this course, you will learn about general reliability mathematics and modeling, reliability model development and calibration, physical causes of semiconductor device failure, model-based reliability prediction, product testing and measurement, and failure diagnosis. These topics will be covered with emphasis on how they apply to integrated circuit technology.

Topical Outline

	Topic	Reading	Assignment(s)
I. Introduction			
01.	Course introduction/overview, start probability review	1.1, 2.2	HW1
II. Review of probability theory			
02.	Random variables (RV), conditional distributions, joint statistics	2.2	HW2
03.	Sample mean, order statistics, start reliability mathematics	2.1–2.3	HW3
III. Reliability Mathematics			
04.	Reliability measures, aging trends, memoryless systems	2.3–2.5	HW4
05.	Time-to-failure distributions, start reliability testing/measurements	2.6, 5.1–5.3	HW5
IV. Reliability testing/measurements			
06.	Reliability bounds, aging trend identification	5.1–5.4	HW6
07.	Graphical estimation of failure time distributions	5.4–5.4.1.4	HW7
08.	Censored data, analytical estimation of distribution parameters	5.4.1.4–5.4.2.1	HW8
09.	Estimation of parameters from failure data	5.4.2.1	HW9
10.	Checking the fit to the failure data	5.4.2.2, 5.5	HW10
	• **Mid-Term Exam**		
VII. Industrial practice			
11.	Accelerated testing, reliability prediction	5.6, 6.1–6.3	
12.	Screening, failure analysis, built-in reliability	7.1–7.4, 8.1–8.5, 9.1–9.5	

Grading: Your course grade will be based on your performance on: (1) Ten homework assignments (30%), (2) One mid-term exam (30%), (3) One project report and presentation (30%) and (4) Attendance of the project presentations (10%). Every homework assignment is **due in one week** from the date it is handed out. There will be **no final exam**. The project report is **due on the day of your project presentation**. Additional information on the project is given below.

IMPORTANT: As part of the project, you will be required to give a 1 hour **presentation**. The six presentations will be held in the evenings 6–7PM on December 1, 2, 3, 4, 5, & 8. You are **required to attend** all six evening presentations. For every missed presentation (other than yours) you will lose 2% of your course grade. Make sure to **block off** these times/dates in your calendar as soon as possible.

IMPORTANT: There will be **no class on on Nov. 12**. In order to make up for lost time, we will have an **additional evening class** 6–8PM on Thu. Nov. 13. Make sure to **block off** this time/date in your calendar as soon as possible. The mid-term exam will be held *in class* on Nov. 26.

The Project

For the project, you will form 6 groups, and each group will prepare a **report** and give a **presentation** on one of the following 6 failure mechanisms:

1. Electro-Static Discharge (ESD) / Electrical Over Stress (EOS)
2. Gate Oxide Breakdown
3. Hot Carriers
4. Packaging Problems
5. Metal Interconnect Problems
6. Radiation-Induced Soft Errors

You are expected to survey the latest literature and present the state of the art knowledge about the specific failure mechanism. Your report should be substantial (typically, over 20 pages long) and should read as a review/tutorial paper. It should include an abstract and an introduction. Each group should submit a single report that tells a single coherent story and has a single list of references at the end. You may want to include sections on "Causes," "Effects," and "Prevention," in the style of the text by Amerasekera and Najm. In addition, feel free to discuss issues that may be relevant to the specific failure mechanism. For instance, for electromigration you may want to present *failure models* that give the MTF in terms of average current.

Make sure to always use the latest available references to get your information, as many aspects of the field are still controversial today. You should talk to the instructor about new aspects of the problems to be covered in your report and presentation, based on the latest technology developments. Make sure to check recent textbooks in the library and you may also want to use the following sources:

1. IEEE International Reliability Physics Symposium (IRPS)
2. IEEE Transactions on Electron Devices
3. International Symposium on Test and Failure Analysis (ISTFA)
4. European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)

In your report and presentation, you should plan to cover the following topics:

1. Describe the *symptoms* of the failure (so-called the *failure mode*). What do we actually observe when we say that a device has failed due to this type of failure? How does this failure manifest itself (short circuit, open circuit, silicon meltdown, etc)? It would be helpful here to show some photomicrographs of failure sites to show how a real chip may have been damaged by this type of failure.
2. What is the *root-cause* of this failure, i.e., what physical processes are believed to lead to this type of failure (e.g., electron wind due to high current density causes ion movement along grain boundaries, leading to hill or void formation, leading to electromigration).
3. How common is this type of failure? How big a problem is it? Do most chips fail due to this failure mechanism? If you can find the data, show the results of industrial studies that illustrate what percentage of chips fail due to this cause.
4. How much do we know about this failure mechanism? Is there a model for, say, the mean-time-to-failure (MTF) in terms of some electrical (I, V) or environmental (temperature, humidity) *conditions of use* of the device? If the MTF is not applicable, then show anything that can help predict the effect of the electrical and environmental conditions on the failure. Such a model would be called a *failure model*. It is usually built from some physical arguments and empirical studies.
5. How can we, during the design phase of a chip, estimate or predict its susceptibility to this type of failure? Specifically, how is the failure model useful for doing this in a CAD tool or environment? What such CAD tools exist? Give general information on some such tool(s); when/how can they be used; how do they work; etc..
6. How can we protect from this failure? Specifically, if we know of a good failure model, then how can we use it to come up with good *chip design strategies* that make the chip less susceptible to this type of failure. For instance, can we make the chip ESD-hard by proper layout? What can we do during the logic design step to ensure that the chip is not susceptible to hot-carriers, and what exactly do we mean by not susceptible?